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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

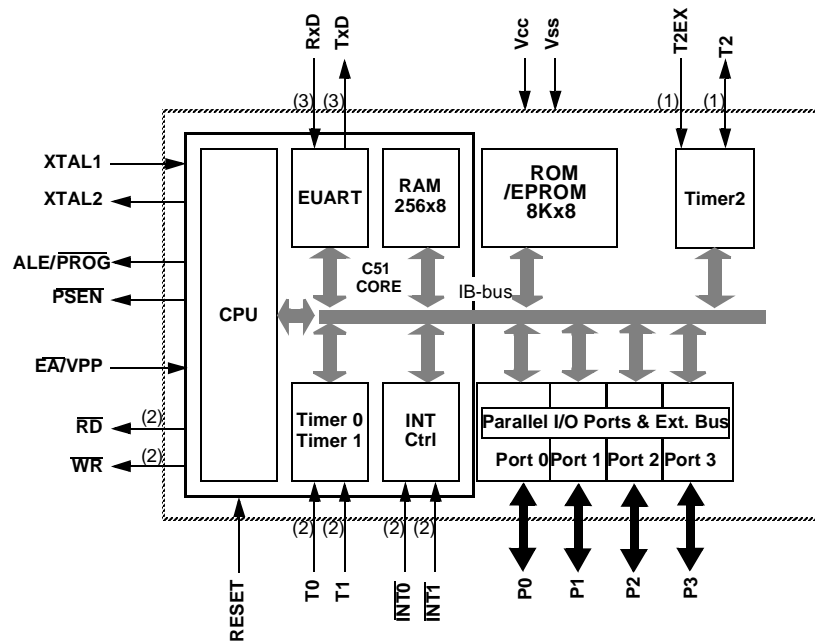
#### Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	60/30MHz
Connectivity	UART/USART
Peripherals	POR
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/ts87c52x2-vib">https://www.e-xfl.com/product-detail/microchip-technology/ts87c52x2-vib</a>

**Table 1. Memory Size**

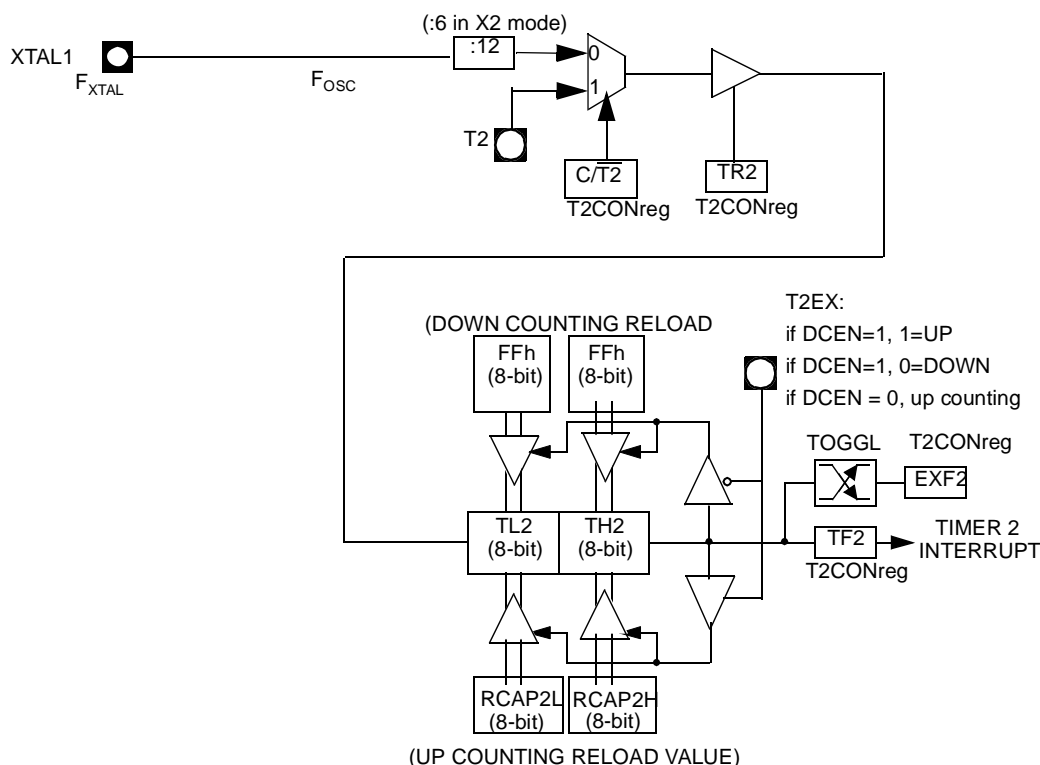
	ROM (bytes)	EPROM (bytes)	TOTAL RAM (bytes)
TS80C32X2	0	0	256
TS80C52X2	8k	0	256
TS87C52X2	0	8k	256

## Block Diagram



- Notes:
1. Alternate function of Port 1
  2. Alternate function of Port 3

Mnemonic	Pin Number			Type	Name and Function
	DIL	LCC	VQFP 1.4		
V <sub>SS</sub>	20	22	16	I	<b>Ground:</b> 0V reference
V <sub>SS1</sub>		1	39	I	Optional Ground: <b>Contact the Sales Office for ground connection.</b>
V <sub>CC</sub>	40	44	38	I	<b>Power Supply:</b> This is the power supply voltage for normal, idle and power-down operation
P0.0-P0.7	39-32	43-36	37-30	I/O	<b>Port 0:</b> Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. Port 0 pins must be polarized to V <sub>CC</sub> or V <sub>SS</sub> in order to prevent any parasitic current consumption. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-up when emitting 1s. Port 0 also inputs the code bytes during EPROM programming. External pull-ups are required during program verification during which P0 outputs the code bytes.
P1.0-P1.7	1-8	2-9	40-44 1-3	I/O	<b>Port 1:</b> Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. Port 1 also receives the low-order address byte during memory programming and verification.  Alternate functions for Port 1 include:
	1	2	40	I/O	<b>T2 (P1.0):</b> Timer/Counter 2 external count input/Clockout
	2	3	41	I	<b>T2EX (P1.1):</b> Timer/Counter 2 Reload/Capture/Direction Control
P2.0-P2.7	21-28	24-31	18-25	I/O	<b>Port 2:</b> Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX atDPTR). In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX atRi), port 2 emits the contents of the P2 SFR. Some Port 2 pins receive the high order address bits during EPROM programming and verification: P2.0 to P2.4
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	<b>Port 3:</b> Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Port 3 also serves the special features of the 80C51 family, as listed below.
	10	11	5	I	<b>RXD (P3.0):</b> Serial input port
	11	13	7	O	<b>TXD (P3.1):</b> Serial output port
	12	14	8	I	<b>INT0 (P3.2):</b> External interrupt 0

**Figure 4. Auto-reload Mode Up/Down Counter (DCEN = 1)**


### Programmable Clock-output

In the clock-out mode, timer 2 operates as a 50%-duty-cycle, programmable clock generator (See Figure 5). The input clock increments TL2 at frequency  $F_{OSC}/2$ . The timer repeatedly counts to overflow from a loaded value. At overflow, the contents of RCAP2H and RCAP2L registers are loaded into TH2 and TL2. In this mode, timer 2 overflows do not generate interrupts. The formula gives the clock-out frequency as a function of the system oscillator frequency and the value in the RCAP2H and RCAP2L registers :

$$Clock - OutFrequency = \frac{F_{osc}}{4 \times (65536 - RCAP2H/RCAP2L)}$$

For a 16 MHz system clock, timer 2 has a programmable frequency range of 61 Hz ( $F_{OSC}/2^{16}$ ) to 4 MHz ( $F_{OSC}/4$ ). The generated clock signal is brought out to T2 pin (P1.0).

Timer 2 is programmed for the clock-out mode as follows:

- Set T2OE bit in T2MOD register.
- Clear  $C/\overline{T}2$  bit in T2CON register.
- Determine the 16-bit reload value from the formula and enter it in RCAP2H/RCAP2L registers.
- Enter a 16-bit initial value in timer registers TH2/TL2. It can be the same as the reload value or a different one depending on the application.
- To start the timer, set TR2 run control bit in T2CON register.

It is possible to use timer 2 as a baud rate generator and a clock generator simultaneously. For this configuration, the baud rates and clock frequencies are not independent since both functions use the values in the RCAP2H and RCAP2L registers.

**Table 6.** T2MOD Register  
T2MOD - Timer 2 Mode Control Register (C9h)

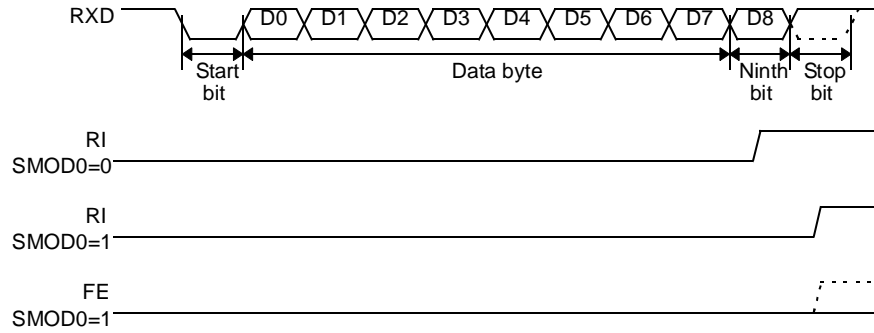
7	6	5	4	3	2	1	0
-	-	-	-	-	-	T2OE	DCEN

Bit Number	Bit Mnemonic	Description
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
4	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
3	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
2	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
1	T2OE	<b>Timer 2 Output Enable bit</b> Clear to program P1.0/T2 as clock input or I/O port. Set to program P1.0/T2 as clock output.
0	DCEN	<b>Down Counter Enable bit</b> Clear to disable timer 2 as up/down counter. Set to enable timer 2 as up/down counter.

Reset Value = XXXX XX00b  
Not bit addressable

**Figure 8. UART Timings in Modes 2 and 3**



### Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

**Note:** The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).

### Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed.

To address a device by its individual address, the SADEN mask byte must be 1111 1111b.

For example:

```
SADDR0101 0110b
SADEN1111 1100b
Given0101 01XXb
```

The following is an example of how to use given addresses to address different slaves:

```
Slave A:SADDR1111 0001b
SADEN1111 1010b
Given1111 0X0Xb
```

```
Slave B:SADDR1111 0011b
SADEN1111 1001b
Given1111 0XX1b
```

```
Slave C:SADDR1111 0010b
SADEN1111 1101b
Given1111 00X1b
```

The SADEN byte is selected so that each slave may be addressed separately.

For slave A, bit 0 (the LSB) is a don't-care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g.

1111 0000b).

For slave A, bit 1 is a 1; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves B and C, but not slave A, the master must send an address with bits 0 and 1 both set (e.g. 1111 0011b).

To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e.g. 1111 0001b).

## Broadcast Address

A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-care bits, e.g.:

```
SADDR 0101 0110b
SADEN 1111 1100b
Broadcast =SADDR OR SADEN1111 111Xb
```

The use of don't-care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh. The following is an example of using broadcast addresses:

```
Slave A:SADDR1111 0001b
      SADEN1111 1010b
Broadcast1111 1X11b,
```

```
Slave B:SADDR1111 0011b
      SADEN1111 1001b
Broadcast1111 1X11b,
```

```
Slave C:SADDR=1111 0010b
      SADEN1111 1101b
Broadcast1111 1111b
```

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send an address FFh. To communicate with slaves A and B, but not slave C, the master can send an address FBh.

## Reset Addresses

On reset, the SADDR and SADEN registers are initialized to 00h, i.e. the given and broadcast addresses are XXXX XXXXb (all don't-care bits). This ensures that the serial port will reply to any address, and so, that it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.

**Table 7. SADEN Register**  
SADEN - Slave Address Mask Register (B9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

Not bit addressable

**Table 8. SADDR Register**  
SADDR - Slave Address Register (A9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

Not bit addressable



**Table 10.** PCON Register  
PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL

Bit Number	Bit Mnemonic	Description
7	SMOD1	<b>Serial port Mode bit 1</b> Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	<b>Serial port Mode bit 0</b> Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
4	POF	<b>Power-off Flag</b> Clear to recognize next reset type. Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	<b>General purpose Flag</b> Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	<b>General purpose Flag</b> Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	<b>Power-down mode bit</b> Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	<b>Idle mode bit</b> Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b

Not bit addressable

Power-off flag reset value will be 1 only after a power on (cold reset). A warm reset doesn't affect the value of this bit.



are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

**Table 12.** IE Register  
IE - Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	-	ET2	ES	ET1	EX1	ET0	EX0

Bit Number	Bit Mnemonic	Description
7	EA	<b>Enable All interrupt bit</b> Clear to disable all interrupts. Set to enable all interrupts. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its own interrupt enable bit.
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
5	ET2	<b>Timer 2 overflow interrupt Enable bit</b> Clear to disable timer 2 overflow interrupt. Set to enable timer 2 overflow interrupt.
4	ES	<b>Serial port Enable bit</b> Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	<b>Timer 1 overflow interrupt Enable bit</b> Clear to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.
2	EX1	<b>External interrupt 1 Enable bit</b> Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	<b>Timer 0 overflow interrupt Enable bit</b> Clear to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.
0	EX0	<b>External interrupt 0 Enable bit</b> Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0X00 0000b

Bit addressable

**Table 13.** IP Register  
IP - Interrupt Priority Register (B8h)

7	6	5	4	3	2	1	0
-	-	PT2	PS	PT1	PX1	PT0	PX0

Bit Number	Bit Mnemonic	Description
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
5	PT2	<b>Timer 2 overflow interrupt Priority bit</b> Refer to PT2H for priority level.
4	PS	<b>Serial port Priority bit</b> Refer to PSH for priority level.
3	PT1	<b>Timer 1 overflow interrupt Priority bit</b> Refer to PT1H for priority level.
2	PX1	<b>External interrupt 1 Priority bit</b> Refer to PX1H for priority level.
1	PT0	<b>Timer 0 overflow interrupt Priority bit</b> Refer to PT0H for priority level.
0	PX0	<b>External interrupt 0 Priority bit</b> Refer to PX0H for priority level.

Reset Value = XX00 0000b  
Bit addressable

**Table 14.** IPH Register  
IPH - Interrupt Priority High Register (B7h)

7	6	5	4	3	2	1	0
-	-	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Bit Number	Bit Mnemonic	Description															
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.															
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.															
5	PT2H	<b>Timer 2 overflow interrupt Priority High bit</b> <table> <tr> <th>PT2H</th><th>PT2</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PT2H	PT2	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PT2H	PT2	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															
4	PSH	<b>Serial port Priority High bit</b> <table> <tr> <th>PSH</th><th>PS</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PSH	PS	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PSH	PS	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															
3	PT1H	<b>Timer 1 overflow interrupt Priority High bit</b> <table> <tr> <th>PT1H</th><th>PT1</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PT1H	PT1	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PT1H	PT1	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															
2	PX1H	<b>External interrupt 1 Priority High bit</b> <table> <tr> <th>PX1H</th><th>PX1</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PX1H	PX1	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PX1H	PX1	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															
1	PT0H	<b>Timer 0 overflow interrupt Priority High bit</b> <table> <tr> <th>PT0H</th><th>PT0</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PT0H	PT0	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PT0H	PT0	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															
0	PX0H	<b>External interrupt 0 Priority High bit</b> <table> <tr> <th>PX0H</th><th>PX0</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PX0H	PX0	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PX0H	PX0	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															

Reset Value = XX00 0000b  
Not bit addressable

## ONCE™ Mode (ON Chip Emulation)

The ONCE mode facilitates testing and debugging of systems using TS80C52X2 without removing the circuit from the board. The ONCE mode is invoked by driving certain pins of the TS80C52X2; the following sequence must be exercised:

- Pull ALE low while the device is in reset (RST high) and  $\overline{\text{PSEN}}$  is high.
- Hold ALE low as RST is deactivated.

While the TS80C52X2 is in ONCE mode, an emulator or test CPU can be used to drive the circuit Table 26. shows the status of the port pins during ONCE mode.

Normal operation is restored when normal reset is applied.

**Table 16.** External Pin Status during ONCE Mode

ALE	PSEN	Port 0	Port 1	Port 2	Port 3	XTAL1/2
Weak pull-up	Weak pull-up	Float	Weak pull-up	Weak pull-up	Weak pull-up	Active

Control and program signals must be held at the levels indicated in Table 35.

#### Definition of terms








**Address Lines:** P1.0-P1.7, P2.0-P2.4 respectively for A0-A12

**Data Lines:** P0.0-P0.7 for D0-D7

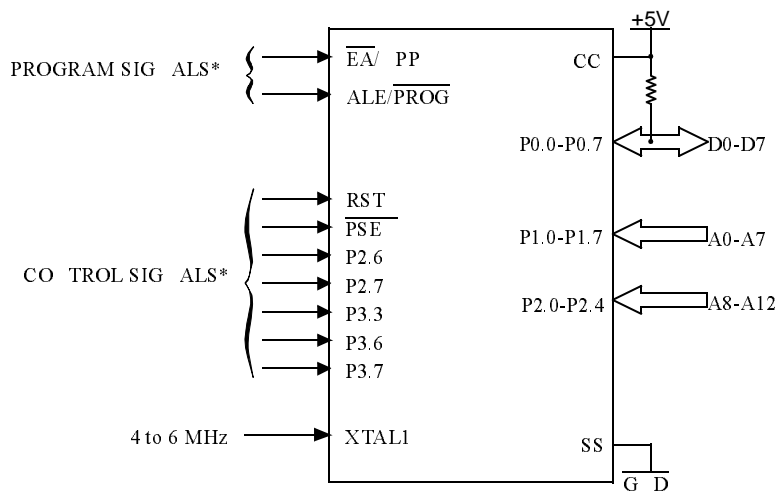
**Control Signals:** RST,  $\overline{\text{PSEN}}$ , P2.6, P2.7, P3.3, P3.6, P3.7.

**Program Signals:** ALE/ $\overline{\text{PROG}}$ ,  $\overline{\text{EA}}$ /VPP.

**Table 20.** EPROM Set-up Modes

Mode	RST	PSEN	ALE/ PROG	$\overline{\text{EA}}$ / VPP	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code data	1	0		12.75V	0	1	1	1	1
Verify Code data	1	0	1	1	0		0	1	1
Program Encryption Array Address 0-3Fh	1	0		12.75V	0	1	1	0	1
Read Signature Bytes	1	0	1	1	0		0	0	0
Program Lock bit 1	1	0		12.75V	1	1	1	1	1
Program Lock bit 2	1	0		12.75V	1	1	1	0	0
Program Lock bit 3	1	0		12.75V	1	0	1	1	0

**Figure 11.** Set-Up Modes Configuration



\* See Table 31. for proper value on these inputs

12,000  $\mu\text{W}/\text{cm}^2$  rating for 30 minutes, at a distance of about 25 mm, should be sufficient. An exposure of 1 hour is recommended with most of standard erasers.

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Å. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

## Signature Bytes

The TS80/87C52X2 has four signature bytes in location 30h, 31h, 60h and 61h. To read these bytes follow the procedure for EPROM verify but activate the control lines provided in Table 31. for Read Signature Bytes. Table 35. shows the content of the signature byte for the TS80/87C52X2.

**Table 21.** Signature Bytes Content

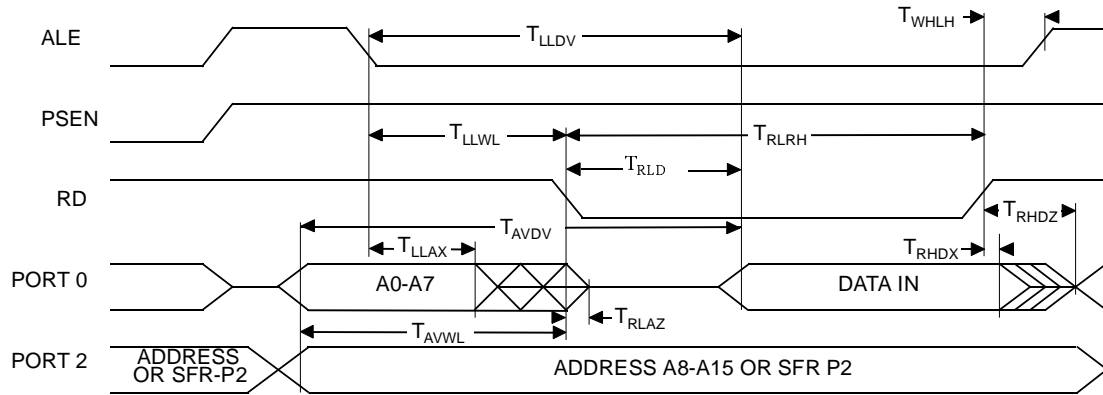
Location	Contents	Comment
30h	58h	Manufacturer Code: Atmel
31h	57h	Family Code: C51 X2
60h	2Dh	Product name: TS80C52X2
60h	ADh	Product name: TS87C52X2
60h	20h	Product name: TS80C32X2
61h	FFh	Product revision number

**Table 22.** DC Parameters in Standard Voltage (Continued)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$V_{OH}$	Output High Voltage, ports 1, 2, 3	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V V V	$I_{OH} = -10 \mu A$ $I_{OH} = -30 \mu A$ $I_{OH} = -60 \mu A$ $V_{CC} = 5V \pm 10\%$
$V_{OH1}$	Output High Voltage, port 0	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V V V	$I_{OH} = -200 \mu A$ $I_{OH} = -3.2 mA$ $I_{OH} = -7.0 mA$ $V_{CC} = 5V \pm 10\%$
$V_{OH2}$	Output High Voltage, ALE, $\overline{PSEN}$	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V V V	$I_{OH} = -100 \mu A$ $I_{OH} = -1.6 mA$ $I_{OH} = -3.5 mA$ $V_{CC} = 5V \pm 10\%$
$R_{RST}$	RST Pulldown Resistor	50	90 <sup>(5)</sup>	200	k $\Omega$	
$I_{IL}$	Logical 0 Input Current ports 1, 2 and 3			-50	$\mu A$	$V_{in} = 0.45V$
$I_{LI}$	Input Leakage Current			$\pm 10$	$\mu A$	$0.45V < V_{in} < V_{CC}$
$I_{TL}$	Logical 1 to 0 Transition Current, ports 1, 2, 3			-650	$\mu A$	$V_{in} = 2.0 V$
$C_{IO}$	Capacitance of I/O Buffer			10	pF	$F_c = 1 MHz$ $T_A = 25^\circ C$
$I_{PD}$	Power Down Current		20 <sup>(5)</sup>	50	$\mu A$	$2.0 V < V_{CC} < 5.5V^{(3)}$
$I_{CC}$ under RESET	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			1 + 0.4 Freq (MHz) at 12MHz 5.8 at 16MHz 7.4	mA	$V_{CC} = 5.5V^{(1)}$
$I_{CC}$ operating	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			3 + 0.6 Freq (MHz) at 12MHz 10.2 at 16MHz 12.6	mA	$V_{CC} = 5.5V^{(8)}$
$I_{CC}$ idle	Power Supply Current Maximum values, X1 mode: <sup>(7)</sup>			0.25+0.3 Freq (MHz) at 12MHz 3.9 at 16MHz 5.1	mA	$V_{CC} = 5.5V^{(2)}$

## External Data Memory Read Cycle

**Figure 20.** External Data Memory Read Cycle



## Serial Port Timing - Shift Register Mode

**Table 32.** Symbol Description

Symbol	Parameter
$T_{XLXL}$	Serial port clock cycle time
$T_{QVHX}$	Output data set-up to clock rising edge
$T_{XHGX}$	Output data hold after clock rising edge
$T_{XHDX}$	Input data hold after clock rising edge
$T_{XHDV}$	Clock rising edge to input data valid

**Table 33.** AC Parameters for a Fix Clock

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$T_{XLXL}$	300		200		300		300		400		ns
$T_{QVHX}$	200		117		200		200		283		ns
$T_{XHGX}$	30		13		30		30		47		ns
$T_{XHDX}$	0		0		0		0		0		ns
$T_{XHDV}$		117		34		117		117		200	ns

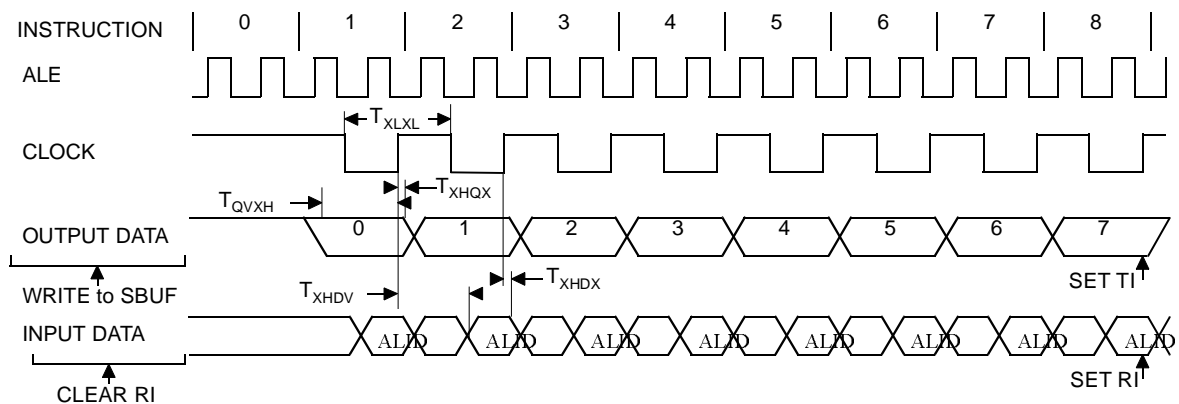


**Table 34.** AC Parameters for a Variable Clock: Derating Formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
$T_{XLXL}$	Min	12 T	6 T				ns
$T_{QVHX}$	Min	10 T - x	5 T - x	50	50	50	ns
$T_{XHGX}$	Min	2 T - x	T - x	20	20	20	ns
$T_{XHDX}$	Min	x	x	0	0	0	ns
$T_{XHDV}$	Max	10 T - x	5 T - x	133	133	133	ns

## Shift Register Timing Waveforms

**Figure 21.** Shift Register Timing Waveforms



## EPROM Programming and Verification Characteristics

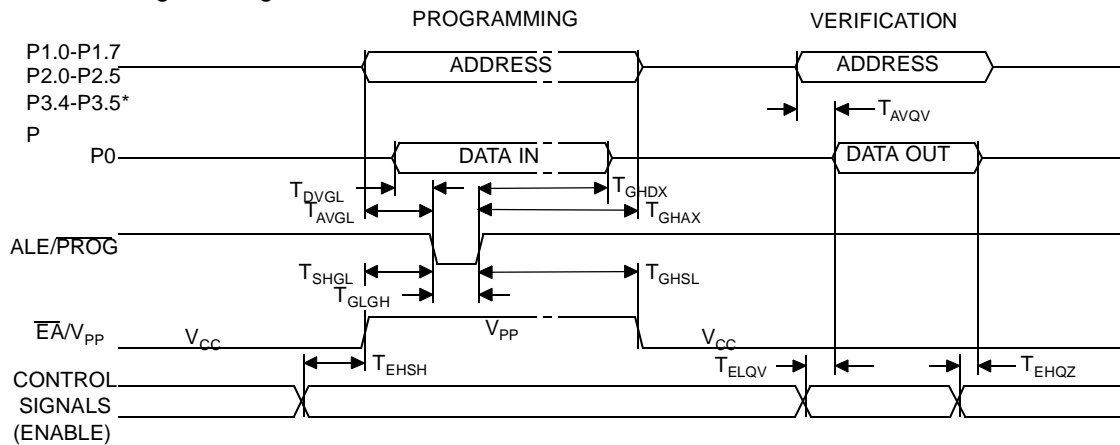
$T_A = 21^{\circ}\text{C}$  to  $27^{\circ}\text{C}$ ;  $V_{SS} = 0\text{V}$ ;  $V_{CC} = 5\text{V} \pm 10\%$  while programming.  $V_{CC}$  = operating range while verifying.

**Table 35.** EPROM Programming Parameters

Symbol	Parameter	Min	Max	Units
$V_{PP}$	Programming Supply Voltage	12.5	13	V
$I_{PP}$	Programming Supply Current		75	mA
$1/T_{CLCL}$	Oscillator Frequency	4	6	MHz
$T_{AVGL}$	Address Setup to $\overline{\text{PROG}}$ Low	$48 T_{CLCL}$		
$T_{GHAX}$	Address Hold after $\overline{\text{PROG}}$	$48 T_{CLCL}$		
$T_{DVGL}$	Data Setup to $\overline{\text{PROG}}$ Low	$48 T_{CLCL}$		
$T_{GHDX}$	Data Hold after $\overline{\text{PROG}}$	$48 T_{CLCL}$		
$T_{EHS}$	(Enable) High to $V_{PP}$	$48 T_{CLCL}$		
$T_{SHGL}$	$V_{PP}$ Setup to $\overline{\text{PROG}}$ Low	10		$\mu\text{s}$
$T_{GHSL}$	$V_{PP}$ Hold after $\overline{\text{PROG}}$	10		$\mu\text{s}$
$T_{GLGH}$	$\overline{\text{PROG}}$ Width	90	110	$\mu\text{s}$
$T_{AVQV}$	Address to Valid Data		$48 T_{CLCL}$	
$T_{ELQV}$	ENABLE Low to Data Valid		$48 T_{CLCL}$	
$T_{EHQZ}$	Data Float after ENABLE	0	$48 T_{CLCL}$	

## EPROM Programming and Verification Waveforms

**Figure 22.** EPROM Programming and Verification Waveforms



\* 8KB: up to P2.4, 16KB: up to P2.5, 32KB: up to P3.4, 64KB: up to P3.5

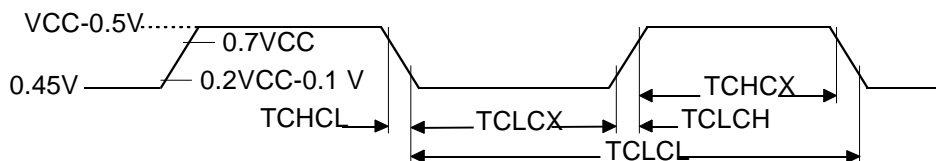
## External Clock Drive Characteristics (XTAL1)

**Table 36.** AC Parameters

Symbol	Parameter	Min	Max	Units
$T_{CLCL}$	Oscillator Period	25		ns
$T_{CHCX}$	High Time	5		ns
$T_{CLCX}$	Low Time	5		ns
$T_{CLCH}$	Rise Time		5	ns
$T_{CHCL}$	Fall Time		5	ns
$T_{CHCX}/T_{CLCX}$	Cyclic ratio in X2 mode	40	60	%

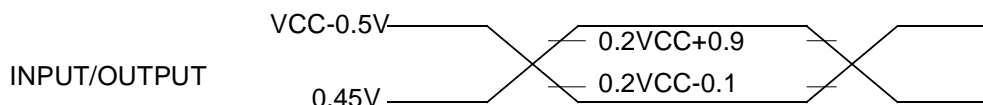
## External Clock Drive Waveforms

**Figure 23.** External Clock Drive Waveforms



## AC Testing Input/Output Waveforms

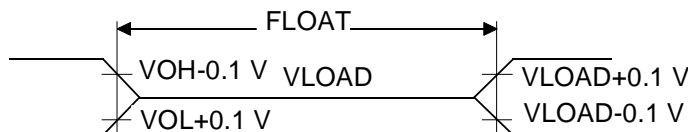
**Figure 24.** AC Testing Input/Output Waveforms



AC inputs during testing are driven at  $V_{CC} - 0.5$  for a logic “1” and 0.45V for a logic “0”. Timing measurement are made at  $V_{IH}$  min for a logic “1” and  $V_{IL}$  max for a logic “0”.

## Float Waveforms

**Figure 25.** Float Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded  $V_{OH}/V_{OL}$  level occurs.  $I_{OL}/I_{OH} \geq \pm 20mA$ .



**Table 37. Possible Ordering Entries (Continued)**

Part Number <sup>(3)</sup>	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
AT80C32X2-RLTUL	ROMLess	2.7 to 5.5V	Industrial & Green	30 MHz <sup>(1)</sup>	VQFP44	Tray
AT80C32X2-3CSUV	ROMLess	5V ±10%	Industrial & Green	60 MHz <sup>(3)</sup>	PDIL40	Stick
AT80C32X2-SLSUV	ROMLess	5V ±10%	Industrial & Green	60 MHz <sup>(3)</sup>	PLCC44	Stick
AT80C32X2-RLTUV	ROMLess	5V ±10%	Industrial & Green	60 MHz <sup>(3)</sup>	VQFP44	Tray
TS80C52X2zzz-MCA	8K ROM	2.7 to 5.5V	Commercial	40 MHz <sup>(1)</sup>	PDIL40	Stick
TS80C52X2zzz-MCB	8K ROM	2.7 to 5.5V	Commercial	40 MHz <sup>(1)</sup>	PLCC44	Stick
TS80C52X2zzz-MCC	8K ROM	2.7 to 5.5V	Commercial	40 MHz <sup>(1)</sup>	PQFP44	Tray
TS80C52X2zzz-MCE	8K ROM	2.7 to 5.5V	Commercial	40 MHz <sup>(1)</sup>	VQFP44	Tray
TS80C52X2zzz-LCA	8K ROM	2.7 to 5.5V	Commercial	30 MHz <sup>(1)</sup>	PDIL40	Stick
TS80C52X2zzz-LCB	8K ROM	2.7 to 5.5V	Commercial	30 MHz <sup>(1)</sup>	PLCC44	Stick
TS80C52X2zzz-LCC	8K ROM	2.7 to 5.5V	Commercial	30 MHz <sup>(1)</sup>	PQFP44	Tray
TS80C52X2zzz-LCE	8K ROM	2.7 to 5.5V	Commercial	30 MHz <sup>(1)</sup>	VQFP44	Tray
TS80C52X2zzz-VCA	8K ROM	5V ±10%	Commercial	60 MHz <sup>(3)</sup>	PDIL40	Stick
TS80C52X2zzz-VCB	8K ROM	5V ±10%	Commercial	60 MHz <sup>(3)</sup>	PLCC44	Stick
TS80C52X2zzz-VCC	8K ROM	5V ±10%	Commercial	60 MHz <sup>(3)</sup>	PQFP44	Tray
TS80C52X2zzz-VCE	8K ROM	5V ±10%	Commercial	60 MHz <sup>(3)</sup>	VQFP44	Tray
TS80C52X2zzz-MIA	8K ROM	5V ±10%	Industrial	40 MHz <sup>(1)</sup>	PDIL40	Stick
TS80C52X2zzz-MIB	8K ROM	5V ±10%	Industrial	40 MHz <sup>(1)</sup>	PLCC44	Stick
TS80C52X2zzz-MIC	8K ROM	5V ±10%	Industrial	40 MHz <sup>(1)</sup>	PQFP44	Tray
TS80C52X2zzz-MIE	8K ROM	5V ±10%	Industrial	40 MHz <sup>(1)</sup>	VQFP44	Tray
TS80C52X2zzz-LIA	8K ROM	2.7 to 5.5V	Industrial	30 MHz <sup>(1)</sup>	PDIL40	Stick
TS80C52X2zzz-LIB	8K ROM	2.7 to 5.5V	Industrial	30 MHz <sup>(1)</sup>	PLCC44	Stick
TS80C52X2zzz-LIC	8K ROM	2.7 to 5.5V	Industrial	30 MHz <sup>(1)</sup>	PQFP44	Tray
TS80C52X2zzz-LIE	8K ROM	2.7 to 5.5V	Industrial	30 MHz <sup>(1)</sup>	VQFP44	Tray
TS80C52X2zzz-VIA	8K ROM	5V ±10%	Industrial	60 MHz <sup>(3)</sup>	PDIL40	Stick
TS80C52X2zzz-VIB	8K ROM	5V ±10%	Industrial	60 MHz <sup>(3)</sup>	PLCC44	Stick
TS80C52X2zzz-VIC	8K ROM	5V ±10%	Industrial	60 MHz <sup>(3)</sup>	PQFP44	Tray
TS80C52X2zzz-VIE	8K ROM	5V ±10%	Industrial	60 MHz <sup>(3)</sup>	VQFP44	Tray
AT80C52X2zzz-3CSUM	8K ROM	5V ±10%	Industrial & Green	40 MHz <sup>(1)</sup>	PDIL40	Stick
AT80C52X2zzz-SLSUM	8K ROM	5V ±10%	Industrial & Green	40 MHz <sup>(1)</sup>	PLCC44	Stick
AT80C52X2zzz-RLTUM	8K ROM	5V ±10%	Industrial & Green	40 MHz <sup>(1)</sup>	VQFP44	Tray