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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

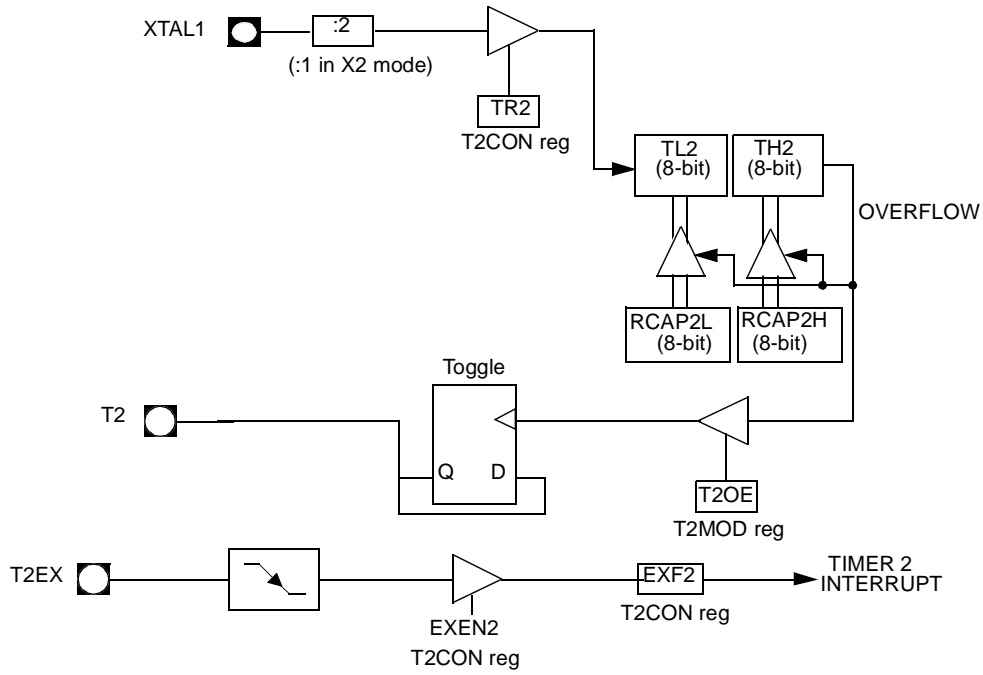
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	60/30MHz
Connectivity	UART/USART
Peripherals	POR
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-PQFP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts87c52x2-vic

Mnemonic	Pin Number			Type	Name and Function
	DIL	LCC	VQFP 1.4		
V _{SS}	20	22	16	I	Ground: 0V reference
V _{SS1}		1	39	I	Optional Ground: Contact the Sales Office for ground connection.
V _{CC}	40	44	38	I	Power Supply: This is the power supply voltage for normal, idle and power-down operation
P0.0-P0.7	39-32	43-36	37-30	I/O	Port 0: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. Port 0 pins must be polarized to V _{CC} or V _{SS} in order to prevent any parasitic current consumption. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-up when emitting 1s. Port 0 also inputs the code bytes during EPROM programming. External pull-ups are required during program verification during which P0 outputs the code bytes.
P1.0-P1.7	1-8	2-9	40-44 1-3	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. Port 1 also receives the low-order address byte during memory programming and verification. Alternate functions for Port 1 include:
	1	2	40	I/O	T2 (P1.0): Timer/Counter 2 external count input/Clockout
	2	3	41	I	T2EX (P1.1): Timer/Counter 2 Reload/Capture/Direction Control
P2.0-P2.7	21-28	24-31	18-25	I/O	Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX atDPTR). In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX atRi), port 2 emits the contents of the P2 SFR. Some Port 2 pins receive the high order address bits during EPROM programming and verification: P2.0 to P2.4
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Port 3 also serves the special features of the 80C51 family, as listed below.
	10	11	5	I	RXD (P3.0): Serial input port
	11	13	7	O	TXD (P3.1): Serial output port
	12	14	8	I	INT0 (P3.2): External interrupt 0

Figure 5. Clock-Out Mode $C/\overline{T2} = 0$



TS80C52X2 Serial I/O Port

The serial I/O port in the TS80C52X2 is compatible with the serial I/O port in the 80C52. It provides both synchronous and asynchronous communication modes. It operates as an Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates

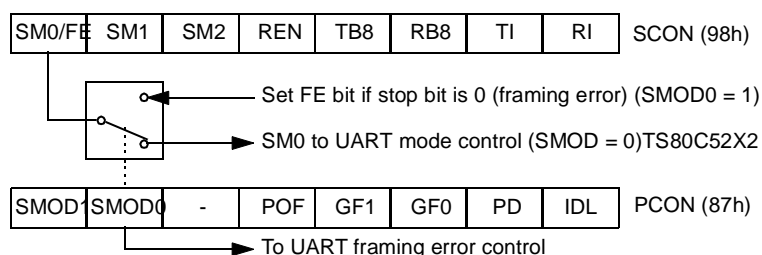
Serial I/O port includes the following enhancements:

- Framing error detection
- Automatic address recognition

Framing Error Detection

Framing bit error detection is provided for the three asynchronous modes (modes 1, 2 and 3). To enable the framing bit error detection feature, set SMOD0 bit in PCON register (See Figure 6).

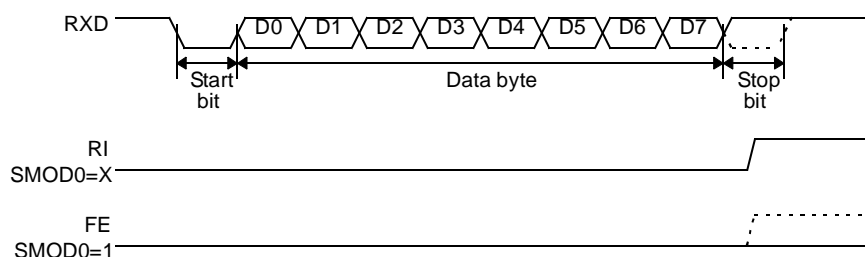
Figure 6. Framing Error Block Diagram



When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register (See Table 9.) bit is set.

Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 7. and Figure 8.).

Figure 7. UART Timings in Mode 1



1111 0000b).

For slave A, bit 1 is a 1; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves B and C, but not slave A, the master must send an address with bits 0 and 1 both set (e.g. 1111 0011b).

To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e.g. 1111 0001b).

Broadcast Address

A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-care bits, e.g.:

```
SADDR 0101 0110b
SADEN 1111 1100b
Broadcast =SADDR OR SADEN1111 111Xb
```

The use of don't-care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh. The following is an example of using broadcast addresses:

```
Slave A:SADDR1111 0001b
      SADEN1111 1010b
Broadcast1111 1X11b,
```

```
Slave B:SADDR1111 0011b
      SADEN1111 1001b
Broadcast1111 1X11b,
```

```
Slave C:SADDR=1111 0010b
      SADEN1111 1101b
Broadcast1111 1111b
```

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send an address FFh. To communicate with slaves A and B, but not slave C, the master can send an address FBh.

Reset Addresses

On reset, the SADDR and SADEN registers are initialized to 00h, i.e. the given and broadcast addresses are XXXX XXXXb (all don't-care bits). This ensures that the serial port will reply to any address, and so, that it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.

Table 7. SADEN Register
SADEN - Slave Address Mask Register (B9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

Not bit addressable

Table 8. SADDR Register
SADDR - Slave Address Register (A9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

Not bit addressable



Table 10. PCON Register
PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL

Bit Number	Bit Mnemonic	Description
7	SMOD1	Serial port Mode bit 1 Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	Serial port Mode bit 0 Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	POF	Power-off Flag Clear to recognize next reset type. Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	Power-down mode bit Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	Idle mode bit Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b

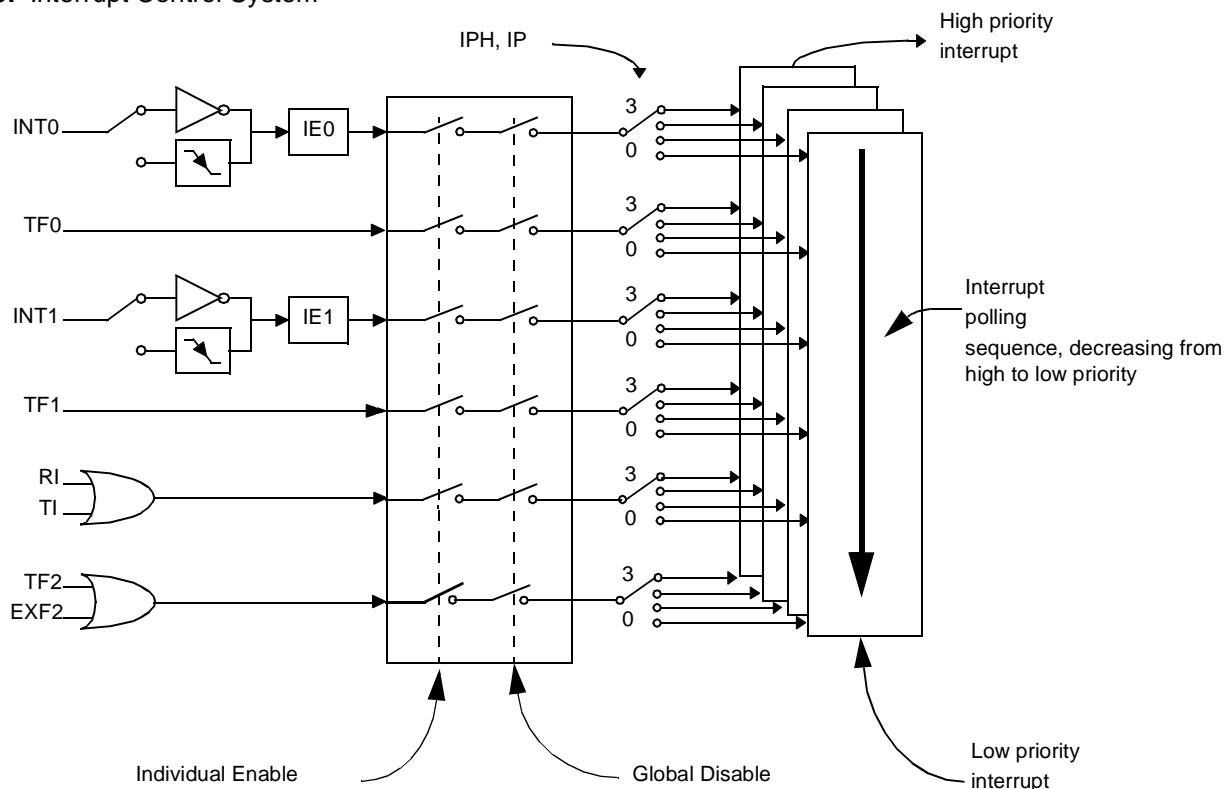
Not bit addressable

Power-off flag reset value will be 1 only after a power on (cold reset). A warm reset doesn't affect the value of this bit.

Interrupt System

The TS80C52X2 has a total of 6 interrupt vectors: two external interrupts ($\overline{\text{INT0}}$ and $\overline{\text{INT1}}$), three timer interrupts (timers 0, 1 and 2) and the serial port interrupt. These interrupts are shown in Figure 9.

Figure 9. Interrupt Control System



Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 12.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 13.) and in the Interrupt Priority High register (See Table 14.). shows the bit values and priority levels associated with each combination.

Table 11. Priority Level Bit Values

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level

are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

Table 12. IE Register
IE - Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	-	ET2	ES	ET1	EX1	ET0	EX0

Bit Number	Bit Mnemonic	Description
7	EA	Enable All interrupt bit Clear to disable all interrupts. Set to enable all interrupts. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its own interrupt enable bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	ET2	Timer 2 overflow interrupt Enable bit Clear to disable timer 2 overflow interrupt. Set to enable timer 2 overflow interrupt.
4	ES	Serial port Enable bit Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	Timer 1 overflow interrupt Enable bit Clear to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.
2	EX1	External interrupt 1 Enable bit Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	Timer 0 overflow interrupt Enable bit Clear to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.
0	EX0	External interrupt 0 Enable bit Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0X00 0000b

Bit addressable

Table 13. IP Register
IP - Interrupt Priority Register (B8h)

7	6	5	4	3	2	1	0
-	-	PT2	PS	PT1	PX1	PT0	PX0

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	PT2	Timer 2 overflow interrupt Priority bit Refer to PT2H for priority level.
4	PS	Serial port Priority bit Refer to PSH for priority level.
3	PT1	Timer 1 overflow interrupt Priority bit Refer to PT1H for priority level.
2	PX1	External interrupt 1 Priority bit Refer to PX1H for priority level.
1	PT0	Timer 0 overflow interrupt Priority bit Refer to PT0H for priority level.
0	PX0	External interrupt 0 Priority bit Refer to PX0H for priority level.

Reset Value = XX00 0000b
Bit addressable

Table 14. IPH Register
IPH - Interrupt Priority High Register (B7h)

7	6	5	4	3	2	1	0
-	-	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Bit Number	Bit Mnemonic	Description															
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.															
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.															
5	PT2H	Timer 2 overflow interrupt Priority High bit <table> <tr> <th>PT2H</th><th>PT2</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PT2H	PT2	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PT2H	PT2	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															
4	PSH	Serial port Priority High bit <table> <tr> <th>PSH</th><th>PS</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PSH	PS	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PSH	PS	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															
3	PT1H	Timer 1 overflow interrupt Priority High bit <table> <tr> <th>PT1H</th><th>PT1</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PT1H	PT1	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PT1H	PT1	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															
2	PX1H	External interrupt 1 Priority High bit <table> <tr> <th>PX1H</th><th>PX1</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PX1H	PX1	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PX1H	PX1	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															
1	PT0H	Timer 0 overflow interrupt Priority High bit <table> <tr> <th>PT0H</th><th>PT0</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PT0H	PT0	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PT0H	PT0	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															
0	PX0H	External interrupt 0 Priority High bit <table> <tr> <th>PX0H</th><th>PX0</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PX0H	PX0	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PX0H	PX0	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															

Reset Value = XX00 0000b
Not bit addressable

Idle mode

An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits GF0 and GF1 can be used to give an indication if an interrupt occurred during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

Power-down Mode

To save maximum power, a power-down mode can be invoked by software (Refer to Table 10., PCON register).

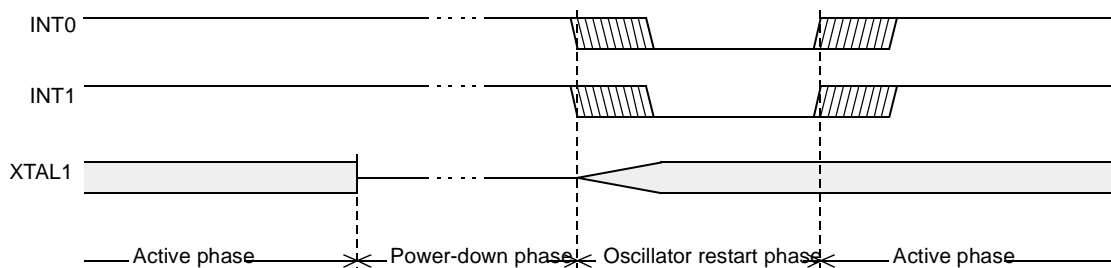
In power-down mode, the oscillator is stopped and the instruction that invoked power-down mode is the last instruction executed. The internal RAM and SFRs retain their value until the power-down mode is terminated. V_{CC} can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from power-down. To properly terminate power-down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

Only external interrupts $\overline{INT0}$ and $\overline{INT1}$ are useful to exit from power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input.

Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 10. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and power down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed.

Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put TS80C52X2 into power-down mode.

Figure 10. Power-down Exit Waveform



ONCE™ Mode (ON Chip Emulation)

The ONCE mode facilitates testing and debugging of systems using TS80C52X2 without removing the circuit from the board. The ONCE mode is invoked by driving certain pins of the TS80C52X2; the following sequence must be exercised:

- Pull ALE low while the device is in reset (RST high) and $\overline{\text{PSEN}}$ is high.
- Hold ALE low as RST is deactivated.

While the TS80C52X2 is in ONCE mode, an emulator or test CPU can be used to drive the circuit Table 26. shows the status of the port pins during ONCE mode.

Normal operation is restored when normal reset is applied.

Table 16. External Pin Status during ONCE Mode

ALE	PSEN	Port 0	Port 1	Port 2	Port 3	XTAL1/2
Weak pull-up	Weak pull-up	Float	Weak pull-up	Weak pull-up	Weak pull-up	Active

DC Parameters for Low Voltage

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$; $V_{SS} = 0\text{ V}$; $V_{CC} = 2.7\text{ V}$ to 5.5 V ; $F = 0$ to 30 MHz .
 $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$; $V_{SS} = 0\text{ V}$; $V_{CC} = 2.7\text{ V}$ to 5.5 V ; $F = 0$ to 30 MHz .

Table 23. DC Parameters for Low Voltage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		$0.2 V_{CC} - 0.1$	V	
V_{IH}	Input High Voltage except XTAL1, RST	$0.2 V_{CC} + 0.9$		$V_{CC} + 0.5$	V	
V_{IH1}	Input High Voltage, XTAL1, RST	$0.7 V_{CC}$		$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage, ports 1, 2, 3 ⁽⁶⁾			0.45	V	$I_{OL} = 0.8\text{ mA}$ ⁽⁴⁾
V_{OL1}	Output Low Voltage, port 0, ALE, $\overline{\text{PSEN}}$ ⁽⁶⁾			0.45	V	$I_{OL} = 1.6\text{ mA}$ ⁽⁴⁾
V_{OH}	Output High Voltage, ports 1, 2, 3	$0.9 V_{CC}$			V	$I_{OH} = -10\text{ }\mu\text{A}$
V_{OH1}	Output High Voltage, port 0, ALE, $\overline{\text{PSEN}}$	$0.9 V_{CC}$			V	$I_{OH} = -40\text{ }\mu\text{A}$
I_{IL}	Logical 0 Input Current ports 1, 2 and 3			-50	μA	$V_{in} = 0.45\text{ V}$
I_{LI}	Input Leakage Current			± 10	μA	$0.45\text{ V} < V_{in} < V_{CC}$
I_{TL}	Logical 1 to 0 Transition Current, ports 1, 2, 3			-650	μA	$V_{in} = 2.0\text{ V}$
R_{RST}	RST Pulldown Resistor	50	90 ⁽⁵⁾	200	$k\Omega$	
CIO	Capacitance of I/O Buffer			10	pF	$F_c = 1\text{ MHz}$ $T_A = 25^\circ\text{C}$
I_{PD}	Power Down Current		20 ⁽⁵⁾ 10 ⁽⁵⁾	50 30	μA	$V_{CC} = 2.0\text{ V}$ to 5.5 V ⁽³⁾ $V_{CC} = 2.0\text{ V}$ to 3.3 V ⁽³⁾
I_{CC} under RESET	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			1 + 0.2 Freq (MHz) at 12MHz 3.4 at 16MHz 4.2	mA	$V_{CC} = 3.3\text{ V}$ ⁽¹⁾
I_{CC} operating	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			1 + 0.3 Freq (MHz) at 12MHz 4.6 at 16MHz 5.8	mA	$V_{CC} = 3.3\text{ V}$ ⁽⁸⁾
I_{CC} idle	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			0.15 Freq (MHz) + 0.2 at 12MHz 2 at 16MHz 2.6	mA	$V_{CC} = 3.3\text{ V}$ ⁽²⁾

- Notes:
- I_{CC} under reset is measured with all output pins disconnected; XTAL1 driven with T_{CLCH} , $T_{CHCL} = 5\text{ ns}$ (see Figure 17.), $V_{IL} = V_{SS} + 0.5\text{ V}$, $V_{IH} = V_{CC} - 0.5\text{ V}$; XTAL2 N.C.; $\overline{\text{EA}} = \text{RST} = \text{Port 0} = V_{CC}$. I_{CC} would be slightly higher if a crystal oscillator used..
 - Idle I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH} , $T_{CHCL} = 5\text{ ns}$, $V_{IL} = V_{SS} + 0.5\text{ V}$, $V_{IH} = V_{CC} - 0.5\text{ V}$; XTAL2 N.C.; Port 0 = V_{CC} ; $\overline{\text{EA}} = \text{RST} = V_{SS}$ (see Figure 15.).
 - Power Down I_{CC} is measured with all output pins disconnected; $\overline{\text{EA}} = V_{SS}$, PORT 0 = V_{CC} ; XTAL2 NC.; RST = V_{SS} (see Figure 16.).
 - Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi V_{OL} peak 0.6V. A Schmitt Trigger use is not necessary.
 - Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
 - Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port:

Port 0: 26 mA

Ports 1, 2 and 3: 15 mA

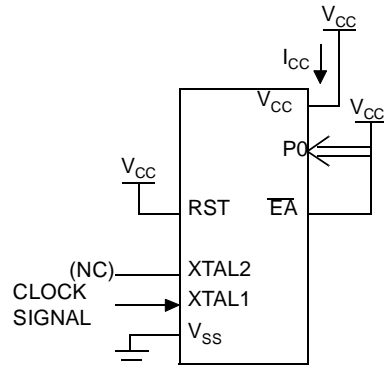
Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

7. For other values, please contact your sales office.

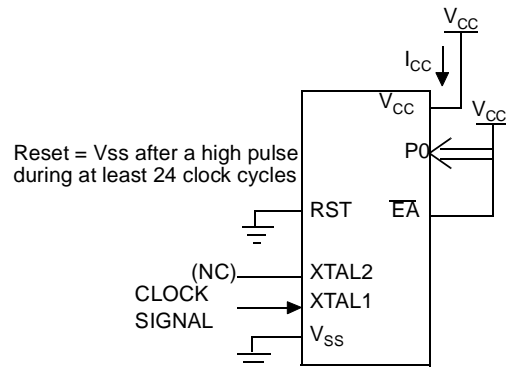
8. Operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH} , $T_{CHCL} = 5$ ns (see Figure 17.), $V_{IL} = V_{SS} + 0.5V$, $V_{IH} = V_{CC} - 0.5V$; XTAL2 N.C.; $\overline{EA} = \text{Port 0} = V_{CC}$; RST = V_{SS} . The internal ROM runs the code 80 FE (label: SJMP label). I_{CC} would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.

Figure 13. I_{CC} Test Condition, under reset



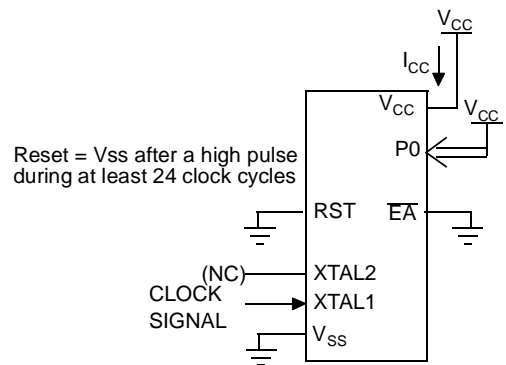
All other pins are disconnected.

Figure 14. Operating I_{CC} Test Condition



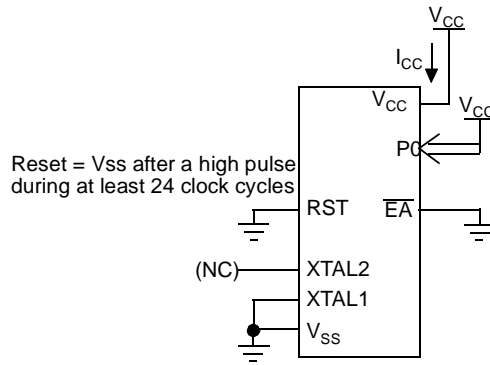
All other pins are disconnected.

Figure 15. I_{CC} Test Condition, Idle Mode



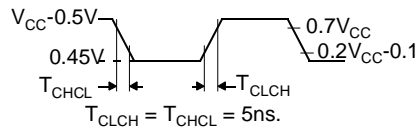
All other pins are disconnected.

Figure 16. I_{CC} Test Condition, Power-down Mode



All other pins are disconnected.

Figure 17. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes



AC Parameters

Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a "T" (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example: T_{AVLL} = Time for Address Valid to ALE Low.

T_{LLPL} = Time for ALE Low to PSEN Low.

$T_A = 0$ to $+70^\circ\text{C}$ (commercial temperature range); $V_{SS} = 0\text{ V}$; $V_{CC} = 5\text{ V} \pm 10\%$; -M and -V ranges.

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (industrial temperature range); $V_{SS} = 0\text{ V}$; $V_{CC} = 5\text{ V} \pm 10\%$; -M and -V ranges.

$T_A = 0$ to $+70^\circ\text{C}$ (commercial temperature range); $V_{SS} = 0\text{ V}$; $2.7\text{ V} < V_{CC} < 5.5\text{ V}$; -L range.

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (industrial temperature range); $V_{SS} = 0\text{ V}$; $2.7\text{ V} < V_{CC} < 5.5\text{ V}$; -L range.

Table 24. gives the maximum applicable load capacitance for Port 0, Port 1, 2 and 3, and ALE and PSEN signals. Timings will be guaranteed if these capacitances are respected. Higher capacitance values can be used, but timings will then be degraded.

Table 24. Load Capacitance versus speed range, in pF

	-M	-V	-L
Port 0	100	50	100
Port 1, 2, 3	80	50	80
ALE / PSEN	100	30	100

Table 5., Table 29. and Table 32. give the description of each AC symbols.

Table 27., Table 30. and Table 33. give for each range the AC parameter.

Table 27. AC Parameters for Fix Clock

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T	25		33		25		50		33		ns
T _{LHLL}	40		25		42		35		52		ns
T _{AVLL}	10		4		12		5		13		ns
T _{LLAX}	10		4		12		5		13		ns
T _{LLIV}		70		45		78		65		98	ns
T _{LLPL}	15		9		17		10		18		ns
T _{PLPH}	55		35		60		50		75		ns
T _{PLIV}		35		25		50		30		55	ns
T _{PXIX}	0		0		0		0		0		ns
T _{PXIZ}		18		12		20		10		18	ns
T _{AVIV}		85		53		95		80		122	ns
T _{PLAZ}		10		10		10		10		10	ns

Table 28. AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
T _{LHLL}	Min	2 T - x	T - x	10	8	15	ns
T _{AVLL}	Min	T - x	0.5 T - x	15	13	20	ns
T _{LLAX}	Min	T - x	0.5 T - x	15	13	20	ns
T _{LLIV}	Max	4 T - x	2 T - x	30	22	35	ns
T _{LLPL}	Min	T - x	0.5 T - x	10	8	15	ns
T _{PLPH}	Min	3 T - x	1.5 T - x	20	15	25	ns
T _{PLIV}	Max	3 T - x	1.5 T - x	40	25	45	ns
T _{PXIX}	Min	x	x	0	0	0	ns
T _{PXIZ}	Max	T - x	0.5 T - x	7	5	15	ns
T _{AVIV}	Max	5 T - x	2.5 T - x	40	30	45	ns
T _{PLAZ}	Max	x	x	10	10	10	ns

Table 31. AC Parameters for a Variable Clock: Derating Formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
T_{RLRH}	Min	$6 T - x$	$3 T - x$	20	15	25	ns
T_{WLWH}	Min	$6 T - x$	$3 T - x$	20	15	25	ns
T_{RLDV}	Max	$5 T - x$	$2.5 T - x$	25	23	30	ns
T_{RHDX}	Min	x	x	0	0	0	ns
T_{RHDZ}	Max	$2 T - x$	$T - x$	20	15	25	ns
T_{LLDV}	Max	$8 T - x$	$4 T - x$	40	35	45	ns
T_{AVDV}	Max	$9 T - x$	$4.5 T - x$	60	50	65	ns
T_{LLWL}	Min	$3 T - x$	$1.5 T - x$	25	20	30	ns
T_{LLWL}	Max	$3 T + x$	$1.5 T + x$	25	20	30	ns
T_{AVWL}	Min	$4 T - x$	$2 T - x$	25	20	30	ns
T_{QVWX}	Min	$T - x$	$0.5 T - x$	15	10	20	ns
T_{QVWH}	Min	$7 T - x$	$3.5 T - x$	15	10	20	ns
T_{WHQX}	Min	$T - x$	$0.5 T - x$	10	8	15	ns
T_{RLAZ}	Max	x	x	0	0	0	ns
T_{WHLH}	Min	$T - x$	$0.5 T - x$	15	10	20	ns
T_{WHLH}	Max	$T + x$	$0.5 T + x$	15	10	20	ns

External Data Memory Write Cycle

Figure 19. External Data Memory Write Cycle

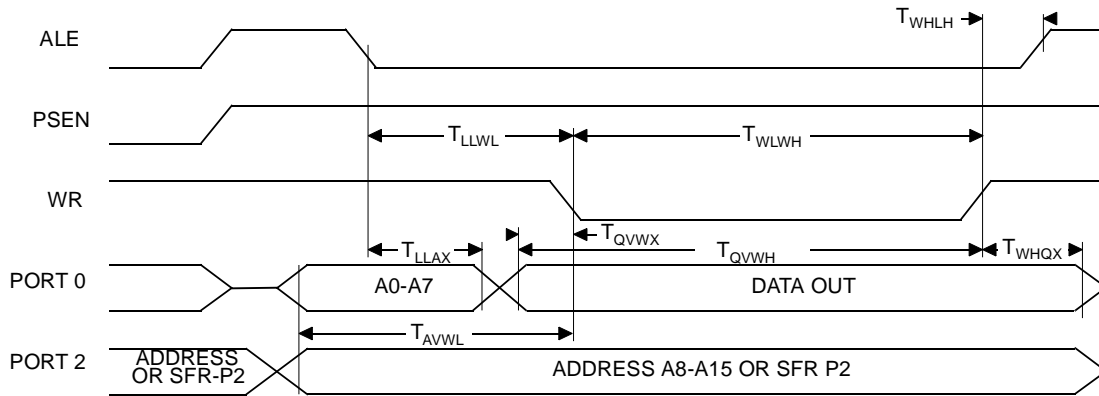


Table 34. AC Parameters for a Variable Clock: Derating Formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
T_{XLXL}	Min	12 T	6 T				ns
T_{QVHX}	Min	10 T - x	5 T - x	50	50	50	ns
T_{XHGX}	Min	2 T - x	T - x	20	20	20	ns
T_{XHDX}	Min	x	x	0	0	0	ns
T_{XHDV}	Max	10 T - x	5 T - x	133	133	133	ns

Shift Register Timing Waveforms

Figure 21. Shift Register Timing Waveforms

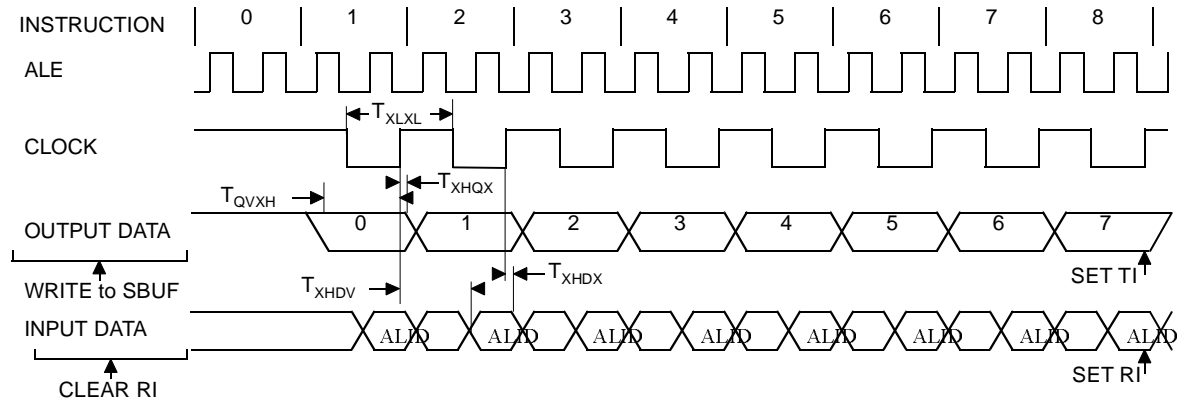


Table 37. Possible Ordering Entries (Continued)

Part Number ⁽³⁾	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
AT80C52X2zzz-3CSUL	8K ROM	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	PDIL40	Stick
AT80C52X2zzz-SLSUL	8K ROM	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	PLCC44	Stick
AT80C52X2zzz-RLTUL	8K ROM	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	VQFP44	Tray
AT80C52X2zzz-3CSUV	8K ROM	5V ±10%	Industrial & Green	60 MHz ⁽³⁾	PDIL40	Stick
AT80C52X2zzz-SLSUV	8K ROM	5V ±10%	Industrial & Green	60 MHz ⁽³⁾	PLCC44	Stick
AT80C52X2zzz-RLTUV	8K ROM	5V ±10%	Industrial & Green	60 MHz ⁽³⁾	VQFP44	Tray
TS87C52X2-MCA	8K OTP	5V ±10%	Commercial	40 MHz ⁽¹⁾	PDIL40	Stick
TS87C52X2-MCB	8K OTP	5V ±10%	Commercial	40 MHz ⁽¹⁾	PLCC44	Stick
TS87C52X2-MCC	8K OTP	5V ±10%	Commercial	40 MHz ⁽¹⁾	PQFP44	Tray
TS87C52X2-MCE	8K OTP	5V ±10%	Commercial	40 MHz ⁽¹⁾	VQFP44	Tray
TS87C52X2-LCA	8K OTP	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PDIL40	Stick
TS87C52X2-LCB	8K OTP	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PLC44	Stick
TS87C52X2-LCC	8K OTP	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PQFP44	Tray
TS87C52X2-LCE	8K OTP	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	VQFP44	Tray
TS87C52X2-VCA	8K OTP	5V ±10%	Commercial	60 MHz ⁽³⁾	PDIL40	Stick
TS87C52X2-VCB	8K OTP	5V ±10%	Commercial	60 MHz ⁽³⁾	PLCC44	Stick
TS87C52X2-VCC	8K OTP	5V ±10%	Commercial	60 MHz ⁽³⁾	PQFP44	Tray
TS87C52X2-VCE	8K OTP	5V ±10%	Commercial	60 MHz ⁽³⁾	VQFP44	Tray
TS87C52X2-MIA	8K OTP	5V ±10%	Industrial	40 MHz ⁽¹⁾	PDIL40	Stick
TS87C52X2-MIB	8K OTP	5V ±10%	Industrial	40 MHz ⁽¹⁾	PLCC44	Stick
TS87C52X2-MIC	8K OTP	5V ±10%	Industrial	40 MHz ⁽¹⁾	PQFP44	Tray
TS87C52X2-MIE	8K OTP	5V ±10%	Industrial	40 MHz ⁽¹⁾	VQFP44	Tray
TS87C52X2-LIA	8K OTP	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PDIL40	Stick
TS87C52X2-LIB	8K OTP	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PLCC44	Stick
TS87C52X2-LIC	8K OTP	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PQFP44	Tray
TS87C52X2-LIE	8K OTP	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	VQFP44	Tray
TS87C52X2-VIA	8K OTP	5V ±10%	Industrial	60 MHz ⁽³⁾	PDIL40	Stick
TS87C52X2-VIB	8K OTP	5V ±10%	Industrial	60 MHz ⁽³⁾	PLCC44	Stick
TS87C52X2-VIC	8K OTP	5V ±10%	Industrial	60 MHz ⁽³⁾	PQFP44	Tray
TS87C52X2-VIE	8K OTP	5V ±10%	Industrial	60 MHz ⁽³⁾	VQFP44	Tray

Table 37. Possible Ordering Entries (Continued)

Part Number ⁽³⁾	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
AT87C52X2-3CSUM	8K OTP	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	PDIL40	Stick
AT87C52X2-SLSUM	8K OTP	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	PLCC44	Stick
AT87C52X2-RLTUM	8K OTP	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	VQFP44	Tray
AT87C52X2-3CSUL	8K OTP	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	PDIL40	Stick
AT87C52X2-SLSUL	8K OTP	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	PLCC44	Stick
AT87C52X2-RLTUL	8K OTP	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	VQFP44	Tray
AT87C52X2-3CSUV	8K OTP	5V ±10%	Industrial & Green	60 MHz ⁽³⁾	PDIL40	Stick
AT87C52X2-SLSUV	8K OTP	5V ±10%	Industrial & Green	60 MHz ⁽³⁾	PLCC44	Stick
AT87C52X2-RLTUV	8K OTP	5V ±10%	Industrial & Green	60 MHz ⁽³⁾	VQFP44	Tray

- Notes:
1. 20 MHz in X2 Mode.
 2. Tape and Reel available for SL, PQFP and RL packages
 3. 30 MHz in X2 Mode.



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