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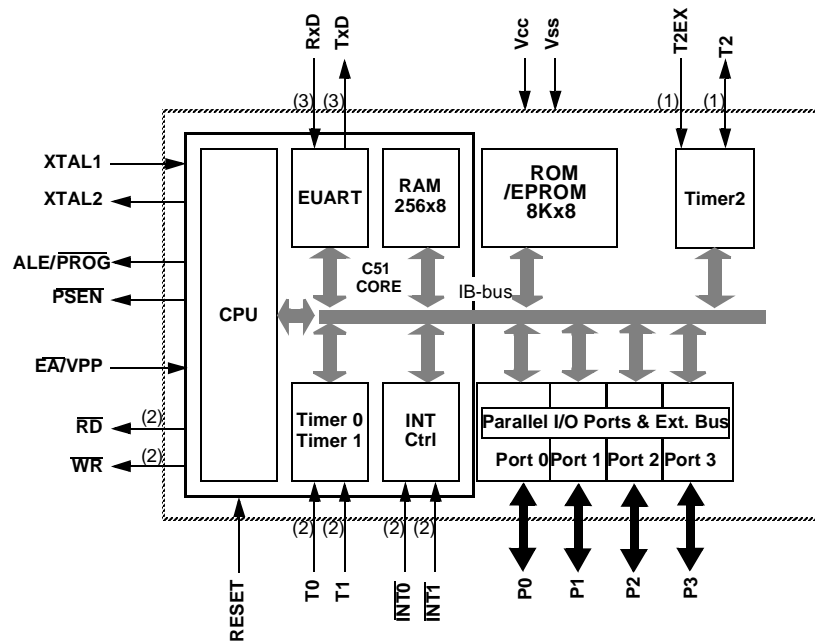
Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	60/30MHz
Connectivity	UART/USART
Peripherals	POR
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-VQFP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts87c52x2-vie

Table 1. Memory Size

	ROM (bytes)	EPROM (bytes)	TOTAL RAM (bytes)
TS80C32X2	0	0	256
TS80C52X2	8k	0	256
TS87C52X2	0	8k	256

Block Diagram



- Notes:
1. Alternate function of Port 1
 2. Alternate function of Port 3

Table 2. All SFRs with their address and their reset value

	Bit Addressable	Non Bit Addressable							
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h									FFh
F0h	B 0000 0000								F7h
E8h									EFh
E0h	ACC 0000 0000								E7h
D8 h									DFh
D0 h	PSW 0000 0000								D7h
C8 h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			CFh
C0 h									C7h
B8h	IP XX00 0000	SADEN 0000 0000							BFh
B0h	P3 1111 1111							IPH XX00 0000	B7h
A8h	IE 0X00 0000	SADDR 0000 0000							AFh
A0h	P2 1111 1111		AUXR1 XXXX XXX0						A7h
98h	SCON 0000 0000	SBUF XXXX XXXX							9Fh
90h	P1 1111 1111								97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XXXXXXXX0	CKCON XXXX XXX0	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Reserved 

Mnemonic	Pin Number			Type	Name and Function
	DIL	LCC	VQFP 1.4		
V _{SS}	20	22	16	I	Ground: 0V reference
V _{SS1}		1	39	I	Optional Ground: Contact the Sales Office for ground connection.
V _{CC}	40	44	38	I	Power Supply: This is the power supply voltage for normal, idle and power-down operation
P0.0-P0.7	39-32	43-36	37-30	I/O	<p>Port 0: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. Port 0 pins must be polarized to V_{CC} or V_{SS} in order to prevent any parasitic current consumption. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-up when emitting 1s. Port 0 also inputs the code bytes during EPROM programming. External pull-ups are required during program verification during which P0 outputs the code bytes.</p>
P1.0-P1.7	1-8	2-9	40-44 1-3	I/O	
					<p>Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. Port 1 also receives the low-order address byte during memory programming and verification.</p> <p>Alternate functions for Port 1 include:</p>
	1	2	40	I/O	T2 (P1.0): Timer/Counter 2 external count input/Clockout
	2	3	41	I	T2EX (P1.1): Timer/Counter 2 Reload/Capture/Direction Control
P2.0-P2.7	21-28	24-31	18-25	I/O	<p>Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX atDPTR). In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX atRi), port 2 emits the contents of the P2 SFR. Some Port 2 pins receive the high order address bits during EPROM programming and verification: P2.0 to P2.4</p>
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	
					<p>Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Port 3 also serves the special features of the 80C51 family, as listed below.</p>
	10	11	5	I	RXD (P3.0): Serial input port
	11	13	7	O	TXD (P3.1): Serial output port
	12	14	8	I	INT0 (P3.2): External interrupt 0

Mnemonic	Pin Number			Type	Name and Function
	DIL	LCC	VQFP 1.4		
	13	15	9	I	INT1 (P3.3): External interrupt 1
	14	16	10	I	T0 (P3.4): Timer 0 external input
	15	17	11	I	T1 (P3.5): Timer 1 external input
	16	18	12	O	WR (P3.6): External data memory write strobe
	17	19	13	O	RD (P3.7): External data memory read strobe
Reset	9	10	4	I	Reset: A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC} .
ALE/PROG	30	33	27	O (I)	Address Latch Enable/Program Pulse: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input (\overline{PROG}) during EPROM programming. ALE can be disabled by setting SFR's AUXR.0 bit. With this bit set, ALE will be inactive during internal fetches.
PSEN	29	32	26	O	Program Store Enable: The read strobe to external program memory. When executing code from the external program memory, \overline{PSEN} is activated twice each machine cycle, except that two \overline{PSEN} activations are skipped during each access to external data memory. \overline{PSEN} is not activated during fetches from internal program memory.
\overline{EA}/V_{PP}	31	35	29	I	External Access Enable/Programming Supply Voltage: \overline{EA} must be externally held low to enable the device to fetch code from external program memory locations 0000H and 3FFFH (RB) or 7FFFH (RC), or FFFFH (RD). If \overline{EA} is held high, the device executes from internal program memory unless the program counter contains an address greater than 3FFFH (RB) or 7FFFH (RC). \overline{EA} must be held low for ROMless devices. This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming. If security level 1 is programmed, \overline{EA} will be internally latched on Reset.
XTAL1	19	21	15	I	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	Crystal 2: Output from the inverting oscillator amplifier

TS80C52X2 Enhanced Features

In comparison to the original 80C52, the TS80C52X2 implements some new features, which are:

- The X2 option
- The Dual Data Pointer
- The 4 level interrupt priority system
- The power-off flag
- The ONCE mode
- The ALE disabling
- Some enhanced features are also located in the UART and the Timer 2

X2 Feature

The TS80C52X2 core needs only 6 clock periods per machine cycle. This feature called "X2" provides the following advantages:

- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power
- Save power consumption while keeping same CPU power (oscillator power saving)
- Save power consumption by dividing dynamically operating frequency by 2 in operating and idle modes
- Increase CPU power by 2 while keeping same crystal frequency

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

Description

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 1. shows the clock generation block diagram. X2 bit is validated on XTAL1÷2 rising edge to avoid glitches when switching from X2 to STD mode. Figure 2 shows the mode switching waveforms.

Figure 1. Clock Generation Diagram

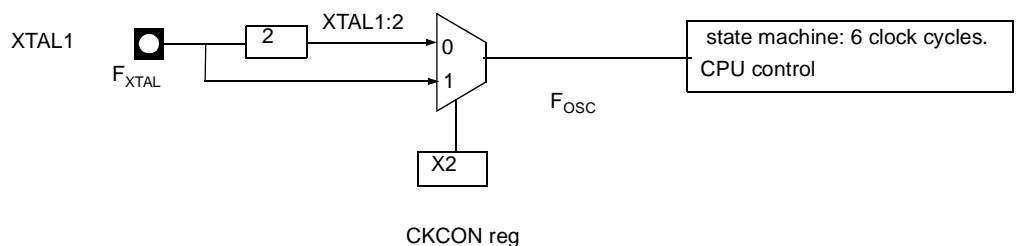


Table 5. T2CON Register
T2CON - Timer 2 Control Register (C8h)

7	6	5	4	3	2	1	0
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#
Bit Number	Bit Mnemonic	Description					
7	TF2	Timer 2 overflow Flag Must be cleared by software. Set by hardware on timer 2 overflow, if RCLK = 0 and TCLK = 0.					
6	EXF2	Timer 2 External Flag Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. When set, causes the CPU to vector to timer 2 interrupt routine when timer 2 interrupt is enabled. Must be cleared by software. EXF2 doesn't cause an interrupt in Up/down counter mode (DCEN = 1)					
5	RCLK	Receive Clock bit Clear to use timer 1 overflow as receive clock for serial port in mode 1 or 3. Set to use timer 2 overflow as receive clock for serial port in mode 1 or 3.					
4	TCLK	Transmit Clock bit Clear to use timer 1 overflow as transmit clock for serial port in mode 1 or 3. Set to use timer 2 overflow as transmit clock for serial port in mode 1 or 3.					
3	EXEN2	Timer 2 External Enable bit Clear to ignore events on T2EX pin for timer 2 operation. Set to cause a capture or reload when a negative transition on T2EX pin is detected, if timer 2 is not used to clock the serial port.					
2	TR2	Timer 2 Run control bit Clear to turn off timer 2. Set to turn on timer 2.					
1	C/T2#	Timer/Counter 2 select bit Clear for timer operation (input from internal clock system: F _{OSC}). Set for counter operation (input from T2 input pin, falling edge trigger). Must be 0 for clock out mode.					
0	CP/RL2#	Timer 2 Capture/Reload bit If RCLK=1 or TCLK=1, CP/RL2# is ignored and timer is forced to Auto-reload on timer 2 overflow. Clear to Auto-reload on timer 2 overflows or negative transitions on T2EX pin if EXEN2=1. Set to capture on negative transitions on T2EX pin if EXEN2=1.					

Reset Value = 0000 0000b

Bit addressable

TS80C52X2 Serial I/O Port

The serial I/O port in the TS80C52X2 is compatible with the serial I/O port in the 80C52. It provides both synchronous and asynchronous communication modes. It operates as an Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates

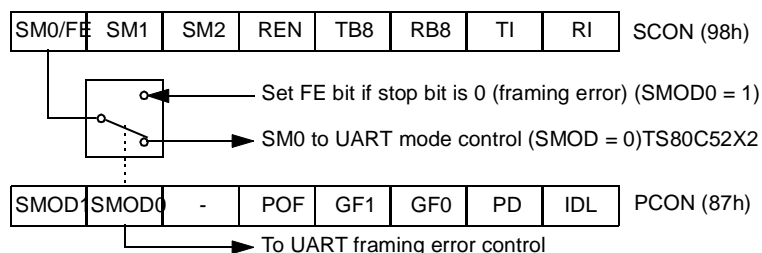
Serial I/O port includes the following enhancements:

- Framing error detection
- Automatic address recognition

Framing Error Detection

Framing bit error detection is provided for the three asynchronous modes (modes 1, 2 and 3). To enable the framing bit error detection feature, set SMOD0 bit in PCON register (See Figure 6).

Figure 6. Framing Error Block Diagram



When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register (See Table 9.) bit is set.

Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 7. and Figure 8.).

Figure 7. UART Timings in Mode 1

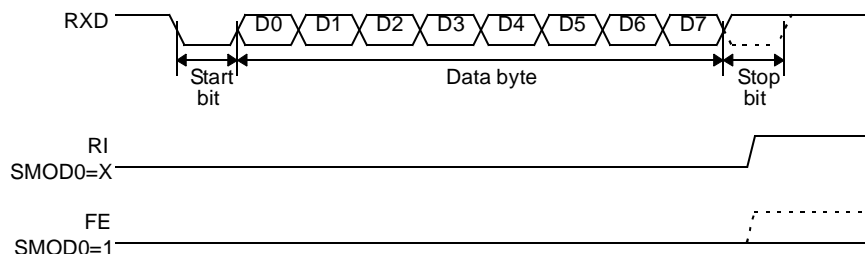
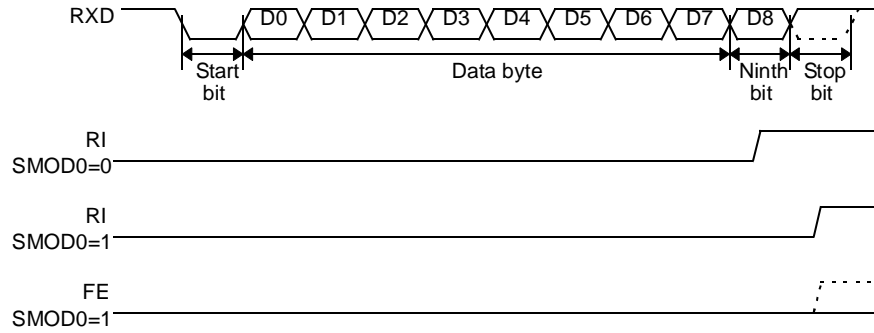


Figure 8. UART Timings in Modes 2 and 3



Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

Note: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).

Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed.

To address a device by its individual address, the SADEN mask byte must be 1111 1111b.

For example:

```
SADDR0101 0110b
SADEN1111 1100b
Given0101 01XXb
```

The following is an example of how to use given addresses to address different slaves:

```
Slave A:SADDR1111 0001b
SADEN1111 1010b
Given1111 0X0Xb
```

```
Slave B:SADDR1111 0011b
SADEN1111 1001b
Given1111 0XX1b
```

```
Slave C:SADDR1111 0010b
SADEN1111 1101b
Given1111 00X1b
```

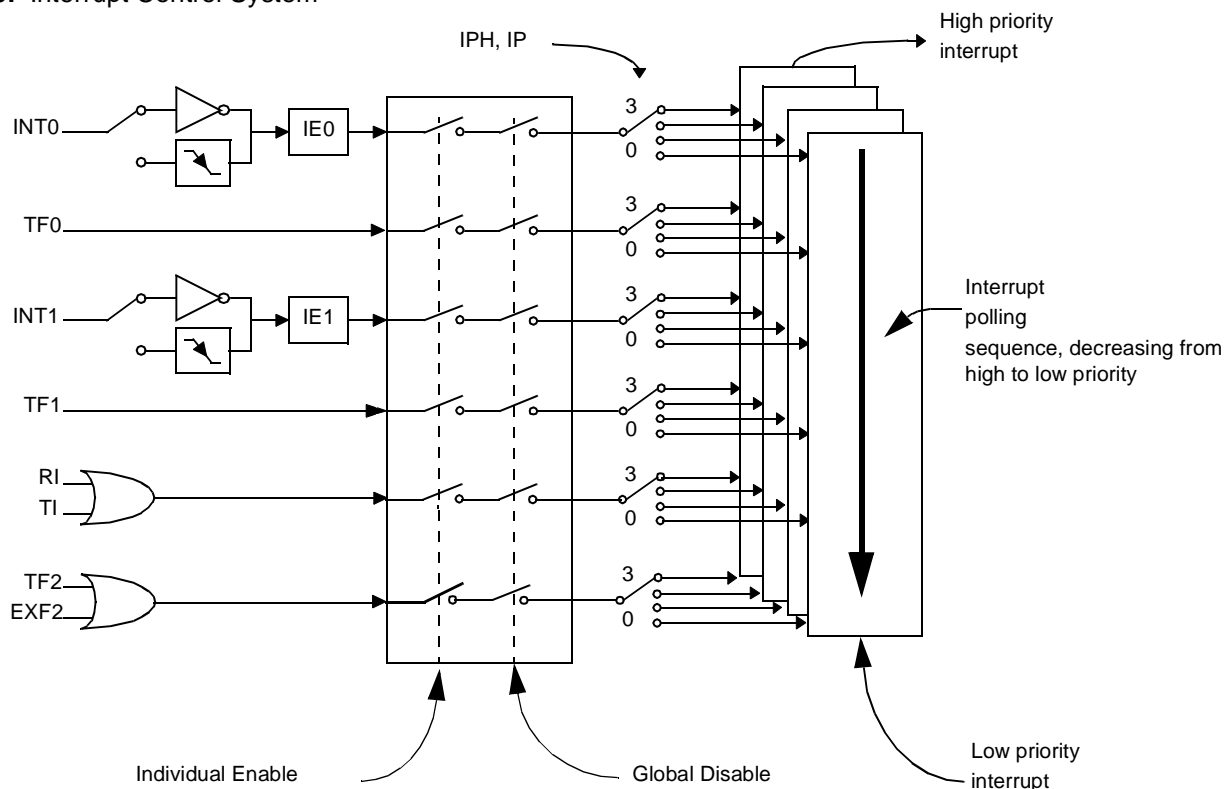
The SADEN byte is selected so that each slave may be addressed separately.

For slave A, bit 0 (the LSB) is a don't-care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g.

Interrupt System

The TS80C52X2 has a total of 6 interrupt vectors: two external interrupts ($\overline{\text{INT0}}$ and $\overline{\text{INT1}}$), three timer interrupts (timers 0, 1 and 2) and the serial port interrupt. These interrupts are shown in Figure 9.

Figure 9. Interrupt Control System



Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 12.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 13.) and in the Interrupt Priority High register (See Table 14.). shows the bit values and priority levels associated with each combination.

Table 11. Priority Level Bit Values

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level

are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

Table 12. IE Register
IE - Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	-	ET2	ES	ET1	EX1	ET0	EX0

Bit Number	Bit Mnemonic	Description
7	EA	Enable All interrupt bit Clear to disable all interrupts. Set to enable all interrupts. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its own interrupt enable bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	ET2	Timer 2 overflow interrupt Enable bit Clear to disable timer 2 overflow interrupt. Set to enable timer 2 overflow interrupt.
4	ES	Serial port Enable bit Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	Timer 1 overflow interrupt Enable bit Clear to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.
2	EX1	External interrupt 1 Enable bit Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	Timer 0 overflow interrupt Enable bit Clear to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.
0	EX0	External interrupt 0 Enable bit Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0X00 0000b

Bit addressable

Table 14. IPH Register
IPH - Interrupt Priority High Register (B7h)

7	6	5	4	3	2	1	0
-	-	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Bit Number	Bit Mnemonic	Description															
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.															
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.															
5	PT2H	Timer 2 overflow interrupt Priority High bit <table> <tr> <th>PT2H</th><th>PT2</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PT2H	PT2	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PT2H	PT2	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															
4	PSH	Serial port Priority High bit <table> <tr> <th>PSH</th><th>PS</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PSH	PS	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PSH	PS	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															
3	PT1H	Timer 1 overflow interrupt Priority High bit <table> <tr> <th>PT1H</th><th>PT1</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PT1H	PT1	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PT1H	PT1	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															
2	PX1H	External interrupt 1 Priority High bit <table> <tr> <th>PX1H</th><th>PX1</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PX1H	PX1	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PX1H	PX1	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															
1	PT0H	Timer 0 overflow interrupt Priority High bit <table> <tr> <th>PT0H</th><th>PT0</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PT0H	PT0	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PT0H	PT0	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															
0	PX0H	External interrupt 0 Priority High bit <table> <tr> <th>PX0H</th><th>PX0</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PX0H	PX0	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PX0H	PX0	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															

Reset Value = XX00 0000b
Not bit addressable

Idle mode

An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits GF0 and GF1 can be used to give an indication if an interrupt occurred during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

Power-down Mode

To save maximum power, a power-down mode can be invoked by software (Refer to Table 10., PCON register).

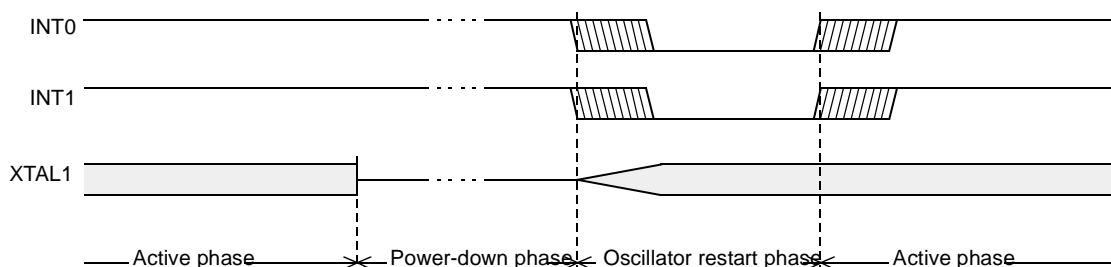
In power-down mode, the oscillator is stopped and the instruction that invoked power-down mode is the last instruction executed. The internal RAM and SFRs retain their value until the power-down mode is terminated. V_{CC} can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from power-down. To properly terminate power-down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

Only external interrupts $\overline{INT0}$ and $\overline{INT1}$ are useful to exit from power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input.

Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 10. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and power down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed.

Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put TS80C52X2 into power-down mode.

Figure 10. Power-down Exit Waveform



Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does not affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content.

Note: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.

Table 15. The State of Ports During Idle and Power-down Modes

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data ⁽¹⁾	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data ⁽¹⁾	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

Note: 1. Port 0 can force a "zero" level. A "one" will leave port floating.

Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0. As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

Table 18. AUXR Register
AUXR - Auxiliary Register (8Eh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	AO

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
1	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
0	AO	ALE Output bit Clear to restore ALE operation during internal fetches. Set to disable ALE operation during internal fetches.

Reset Value = XXXX XXX0b
Not bit addressable

Programming Algorithm

The Improved Quick Pulse algorithm is based on the Quick Pulse algorithm and decreases the number of pulses applied during byte programming from 25 to 1.

To program the TS87C52X2 the following sequence must be exercised:

- Step 1: Activate the combination of control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Input the appropriate data on the data lines.
- Step 4: Raise \overline{EA}/VPP from VCC to VPP (typical 12.75V).
- Step 5: Pulse ALE/ \overline{PROG} once.
- Step 6: Lower \overline{EA}/VPP from VPP to VCC

Repeat step 2 through 6 changing the address and data for the entire array or until the end of the object file is reached (See Figure 12.).

Verify Algorithm

Code array verify must be done after each byte or block of bytes is programmed. In either case, a complete verify of the programmed array will ensure reliable programming of the TS87C52X2.

P 2.7 is used to enable data output.

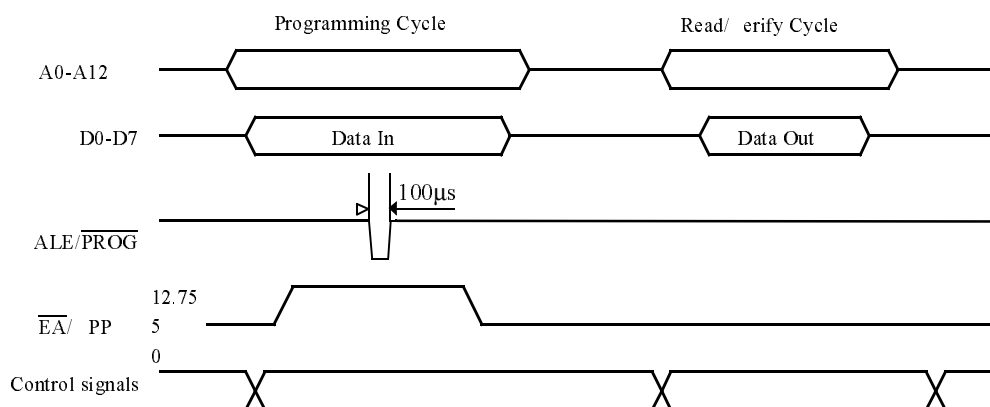
To verify the TS87C52X2 code the following sequence must be exercised:

- Step 1: Activate the combination of program and control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Read data on the data lines.

Repeat step 2 through 3 changing the address for the entire array verification (See Figure 12.).

The encryption array cannot be directly verified. Verification of the encryption array is done by observing that the code array is well encrypted.

Figure 12. Programming and Verification Signal's Waveform



EPROM Erasure (Windowed Packages Only)

Erasing the EPROM erases the code array, the encryption array and the lock bits returning the parts to full functionality.

Erasure leaves all the EPROM cells in a 1's state (FF).

Erasure Characteristics

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Å) to an integrated dose at least 15 W-sec/cm². Exposing the EPROM to an ultraviolet lamp of

Figure 16. I_{CC} Test Condition, Power-down Mode

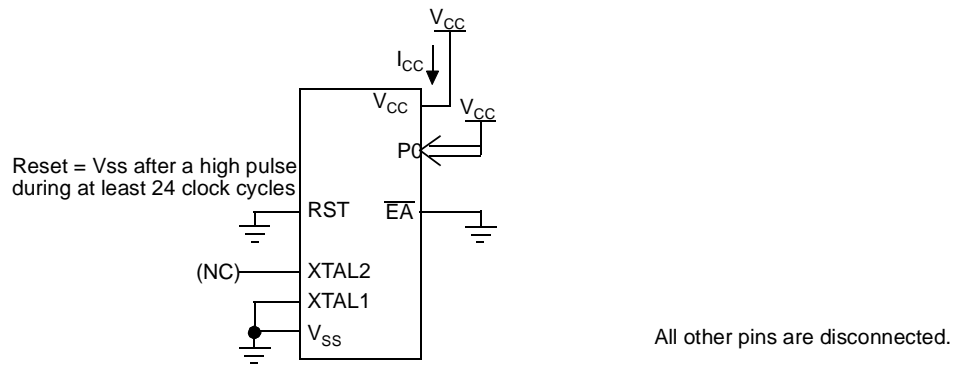
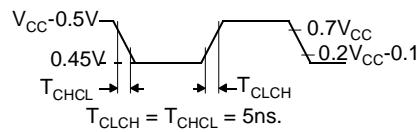


Figure 17. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes



AC Parameters

Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a “T” (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example: T_{AVLL} = Time for Address Valid to ALE Low.

T_{LLPL} = Time for ALE Low to PSEN Low.

$T_A = 0$ to $+70^{\circ}C$ (commercial temperature range); $V_{SS} = 0V$; $V_{CC} = 5V \pm 10\%$; -M and -V ranges.

$T_A = -40^{\circ}C$ to $+85^{\circ}C$ (industrial temperature range); $V_{SS} = 0V$; $V_{CC} = 5V \pm 10\%$; -M and -V ranges.

$T_A = 0$ to $+70^{\circ}C$ (commercial temperature range); $V_{SS} = 0V$; $2.7V < V_{CC} < 5.5V$; -L range.

$T_A = -40^{\circ}C$ to $+85^{\circ}C$ (industrial temperature range); $V_{SS} = 0V$; $2.7V < V_{CC} < 5.5V$; -L range.

Table 24. gives the maximum applicable load capacitance for Port 0, Port 1, 2 and 3, and ALE and PSEN signals. Timings will be guaranteed if these capacitances are respected. Higher capacitance values can be used, but timings will then be degraded.

Table 24. Load Capacitance versus speed range, in pF

	-M	-V	-L
Port 0	100	50	100
Port 1, 2, 3	80	50	80
ALE / PSEN	100	30	100

Table 5., Table 29. and Table 32. give the description of each AC symbols.

Table 27., Table 30. and Table 33. give for each range the AC parameter.

Table 27. AC Parameters for Fix Clock

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T	25		33		25		50		33		ns
T _{LHLL}	40		25		42		35		52		ns
T _{AVLL}	10		4		12		5		13		ns
T _{LLAX}	10		4		12		5		13		ns
T _{LLIV}		70		45		78		65		98	ns
T _{LLPL}	15		9		17		10		18		ns
T _{PLPH}	55		35		60		50		75		ns
T _{PLIV}		35		25		50		30		55	ns
T _{PXIX}	0		0		0		0		0		ns
T _{PXIZ}		18		12		20		10		18	ns
T _{AVIV}		85		53		95		80		122	ns
T _{PLAZ}		10		10		10		10		10	ns

Table 28. AC Parameters for a Variable Clock: derating formula

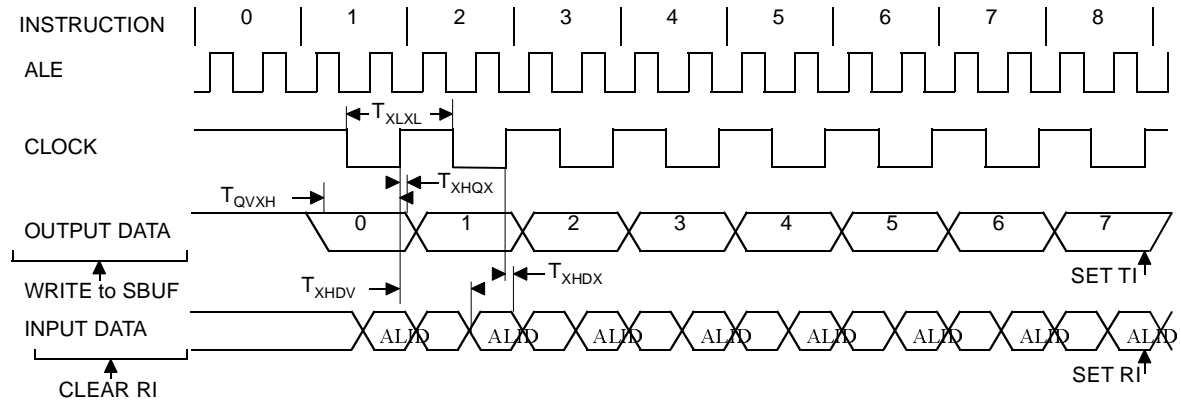
Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
T _{LHLL}	Min	2 T - x	T - x	10	8	15	ns
T _{AVLL}	Min	T - x	0.5 T - x	15	13	20	ns
T _{LLAX}	Min	T - x	0.5 T - x	15	13	20	ns
T _{LLIV}	Max	4 T - x	2 T - x	30	22	35	ns
T _{LLPL}	Min	T - x	0.5 T - x	10	8	15	ns
T _{PLPH}	Min	3 T - x	1.5 T - x	20	15	25	ns
T _{PLIV}	Max	3 T - x	1.5 T - x	40	25	45	ns
T _{PXIX}	Min	x	x	0	0	0	ns
T _{PXIZ}	Max	T - x	0.5 T - x	7	5	15	ns
T _{AVIV}	Max	5 T - x	2.5 T - x	40	30	45	ns
T _{PLAZ}	Max	x	x	10	10	10	ns

Table 34. AC Parameters for a Variable Clock: Derating Formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
T_{XLXL}	Min	12 T	6 T				ns
T_{QVHX}	Min	10 T - x	5 T - x	50	50	50	ns
T_{XHGX}	Min	2 T - x	T - x	20	20	20	ns
T_{XHDX}	Min	x	x	0	0	0	ns
T_{XHDV}	Max	10 T - x	5 T - x	133	133	133	ns

Shift Register Timing Waveforms

Figure 21. Shift Register Timing Waveforms



Ordering Information

Table 37. Possible Ordering Entries

Part Number ⁽³⁾	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
TS80C32X2-MCA	ROMLess	5V \pm 10%	Commercial	40 MHz ⁽¹⁾	PDIL40	Stick
TS80C32X2-MCB	ROMLess	5V \pm 10%	Commercial	40 MHz ⁽¹⁾	PLCC44	Stick
TS80C32X2-MCC	ROMLess	5V \pm 10%	Commercial	40 MHz ⁽¹⁾	PQFP44	Tray
TS80C32X2-MCE	ROMLess	5V \pm 10%	Commercial	40 MHz ⁽¹⁾	VQFP44	Tray
TS80C32X2-LCA	ROMLess	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PDIL40	Stick
TS80C32X2-LCB	ROMLess	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PLCC44	Stick
TS80C32X2-LCC	ROMLess	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PQFP44	Tray
TS80C32X2-LCE	ROMLess	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	VQFP44	Tray
TS80C32X2-VCA	ROMLess	5V \pm 10%	Commercial	60 MHz ⁽³⁾	PDIL40	Stick
TS80C32X2-VCB	ROMLess	5V \pm 10%	Commercial	60 MHz ⁽³⁾	PLCC44	Stick
TS80C32X2-VCC	ROMLess	5V \pm 10%	Commercial	60 MHz ⁽³⁾	PQFP44	Tray
TS80C32X2-VCE	ROMLess	5V \pm 10%	Commercial	60 MHz ⁽³⁾	VQFP44	Tray
TS80C32X2-MIA	ROMLess	5V \pm 10%	Industrial	40 MHz ⁽¹⁾	PDIL40	Stick
TS80C32X2-MIB	ROMLess	5V \pm 10%	Industrial	40 MHz ⁽¹⁾	PLCC44	Stick
TS80C32X2-MIC	ROMLess	5V \pm 10%	Industrial	40 MHz ⁽¹⁾	PQFP44	Tray
TS80C32X2-MIE	ROMLess	5V \pm 10%	Industrial	40 MHz ⁽¹⁾	VQFP44	Tray
TS80C32X2-LIA	ROMLess	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PDIL40	Stick
TS80C32X2-LIB	ROMLess	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PLCC44	Stick
TS80C32X2-LIC	ROMLess	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PQFP44	Tray
TS80C32X2-LIE	ROMLess	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	VQFP44	Tray
TS80C32X2-VIA	ROMLess	5V \pm 10%	Industrial	60 MHz ⁽³⁾	PDIL40	Stick
TS80C32X2-VIB	ROMLess	5V \pm 10%	Industrial	60 MHz ⁽³⁾	PLCC44	Stick
TS80C32X2-VIC	ROMLess	5V \pm 10%	Industrial	60 MHz ⁽³⁾	PQFP44	Tray
TS80C32X2-VIE	ROMLess	5V \pm 10%	Industrial	60 MHz ⁽³⁾	VQFP44	Tray
AT80C32X2-3CSUM	ROMLess	5V \pm 10%	Industrial & Green	40 MHz ⁽¹⁾	PDIL40	Stick
AT80C32X2-SLSUM	ROMLess	5V \pm 10%	Industrial & Green	40 MHz ⁽¹⁾	PLCC44	Stick
AT80C32X2-RLTUM	ROMLess	5V \pm 10%	Industrial & Green	40 MHz ⁽¹⁾	VQFP44	Tray
AT80C32X2-RLTUM	ROMLess	5V \pm 10%	Industrial & Green	40 MHz ⁽¹⁾	VQFP44	Tape & Reel
AT80C32X2-3CSUL	ROMLess	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	PDIL40	Stick
AT80C32X2-SLSUL	ROMLess	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	PLCC44	Stick



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