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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	EBI/EMI, I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	76
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2210fbd144-01-5

- LPC2210/01 and LPC2220 only: UART0/1 include fractional baud rate generator, auto-bauding capabilities, and handshake flow-control fully implemented in hardware.

- Vectored Interrupt Controller (VIC) with configurable priorities and vector addresses.
- Configurable external memory interface with up to four banks, each up to 16 MB and 8/16/32-bit data width.
- Up to 76 general purpose pins (5 V tolerant) capable. Up to nine edge/level sensitive external interrupt pins available.
  - LPC2210/01 and LPC2220 only: Fast GPIO ports enable port pin toggling up to 3.5 times faster than the original device. They also allow for a port pin to be read at any time regardless of its function.
- 60 MHz (LPC2210) and 75 MHz (LPC2210/01 and LPC2220) maximum CPU clock available from programmable on-chip Phase-Locked Loop (PLL) with settling time of 100 µs.
- On-chip integrated oscillator operates with external crystal in range of 1 MHz to 25 MHz and with external oscillator up to 25 MHz.
- Power saving modes include Idle and Power-down.
- Processor wake-up from Power-down mode via external interrupt.
- Individual enable/disable of peripheral functions for power optimization.
- Dual power supply:
  - CPU operating voltage range of 1.65 V to 1.95 V (1.8 V ± 0.15 V).
  - I/O power supply range of 3.0 V to 3.6 V (3.3 V ± 10 %) with 5 V tolerant I/O pads. 16/32-bit ARM7TDMI-S processor.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2210FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2210FBD144/01	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2220FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2220FET144	TFBGA144	plastic thin fine-pitch ball grid array package; 144 balls; body 12 × 12 × 0.8 mm	SOT569-2
LPC2220FET144/G	TFBGA144	plastic thin fine-pitch ball grid array package; 144 balls; body 12 × 12 × 0.8 mm	SOT569-2

Table 3. Ball allocation

Row	Column												
	1	2	3	4	5	6	7	8	9	10	11	12	13
A	P2.22/ D22	$V_{DDA(1V8)}$	P1.28/ TDI	P2.21/ D21	P2.18/ D18	P2.14/ D14	P1.29/ TCK	P2.11/ D11	P2.10/ D10	P2.7/D7	$V_{DD(3V3)}$	$V_{DD(1V8)}$	P2.4/D4
B	$V_{DD(3V3)}$	P1.27/ TDO	XTAL2	$V_{SSA(PLL)}$	P2.19/ D19	P2.15/ D15	P2.12/ D12	P0.20/ MAT1.3/ SSEL1/ EINT3	$V_{DD(3V3)}$	P2.6/D6	V_{SS}	P2.3/D3	V_{SS}
C	P0.21/ PWM5/ CAP1.3	V_{SS}	XTAL1	V_{SSA}	$\overline{\text{RESET}}$	P2.16/ D16	P2.13/ D13	P0.19/ MAT1.2/ MOSI1/ CAP1.2	P2.9/D9	P2.5/D5	P2.2/D2	P2.1/D1	$V_{DD(3V3)}$
D	P0.24	P1.19/ TRACEPKT3	P0.23	P0.22/ CAP0.0/ MAT0.0	P2.20/ D20	P2.17/ D17	V_{SS}	P0.18/ CAP1.3/ MISO1/ MAT1.3	P2.8/D8	P1.30/ TMS	V_{SS}	P1.20/ TRACESYNC	P0.17/ CAP1.2/ SCK1/ MAT1.2
E	P2.25/ D25	P2.24/ D24	P2.23/ D23	V_{SS}						P0.16/ EINT0/ MAT0.2/ CAP0.2	P0.15/ RI1/ EINT2	P2.0/D0	P3.30/ $\overline{\text{BLS1}}$
F	P2.27/ D27/ BOOT1	P1.18/ TRACEPKT2	$V_{DDA(3V3)}$	P2.26/ D26/ BOOT0						P3.31/ $\overline{\text{BLS0}}$	P1.21/ PIPESTAT0	$V_{DD(3V3)}$	V_{SS}
G	P2.29/ D29	P2.28/ D28	P2.30/ D30/AIN4	P2.31/ D31/AIN5						P0.14/ DCD1/ EINT1	P1.0/$\overline{\text{CS0}}$	P3.0/A0	P1.1/$\overline{\text{OE}}$
H	P0.25	n.c.	P0.27/ AIN0/ CAP0.1/ MAT0.1	P1.17/ TRACEPKT1						P0.13/ DTR1/ MAT1.1	P1.22/ PIPESTAT1	P3.2/A2	P3.1/A1
J	P0.28/ AIN1/ CAP0.2/ MAT0.2	V_{SS}	P3.29/ $\overline{\text{BLS2}}$/ AIN6	P3.28/ $\overline{\text{BLS3}}$/ AIN7						P3.3/A3	P1.23/ PIPESTAT2	P0.11/ CTS1/ CAP1.1	P0.12/ DSR1/ MAT1.0
K	P3.27/$\overline{\text{WE}}$	P3.26/ $\overline{\text{CS1}}$	$V_{DD(3V3)}$	P3.22/ A22	P3.20/ A20	P0.1/ RXD0/ PWM3/ EINT0	P3.14/ A14	P1.25/ EXTIN0	P3.11/ A11	$V_{DD(3V3)}$	P0.10/ RTS1/ CAP1.0	V_{SS}	P3.4/A4

Table 4. Pin description *...continued*

Symbol	Pin (LQFP)	Pin (TFBGA)	Type	Description
P1.26/RTCK	52[5]	N6[5]	I/O	**RTCK —** Returned Test Clock output. Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up. Note: LOW on this pin while $\overline{\text{RESET}}$ is LOW, enables pins P1[31:26] to operate as Debug port after reset.
P1.27/TDO	144[5]	B2[5]	O	**TDO —** Test Data out for JTAG interface.
P1.28/TDI	140[5]	A3[5]	I	**TDI —** Test Data in for JTAG interface.
P1.29/TCK	126[5]	A7[5]	I	**TCK —** Test Clock for JTAG interface. This clock must be slower than 1⁄6 of the CPU clock (CCLK) for the JTAG interface to operate.
P1.30/TMS	113[5]	D10[5]	I	**TMS —** Test Mode Select for JTAG interface.
P1.31/$\overline{\text{TRST}}$	43[5]	M4[5]	I	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface.
P2.0 to P2.31			I/O	**Port 2 —** Port 2 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 2 pins depends upon the pin function selected via the Pin Connect Block.
P2.0/D0	98[5]	E12[5]	I/O	**D0 —** External memory data line 0.
P2.1/D1	105[5]	C12[5]	I/O	**D1 —** External memory data line 1.
P2.2/D2	106[5]	C11[5]	I/O	**D2 —** External memory data line 2.
P2.3/D3	108[5]	B12[5]	I/O	**D3 —** External memory data line 3.
P2.4/D4	109[5]	A13[5]	I/O	**D4 —** External memory data line 4.
P2.5/D5	114[5]	C10[5]	I/O	**D5 —** External memory data line 5.
P2.6/D6	115[5]	B10[5]	I/O	**D6 —** External memory data line 6.
P2.7/D7	116[5]	A10[5]	I/O	**D7 —** External memory data line 7.
P2.8/D8	117[5]	D9[5]	I/O	**D8 —** External memory data line 8.
P2.9/D9	118[5]	C9[5]	I/O	**D9 —** External memory data line 9.
P2.10/D10	120[5]	A9[5]	I/O	**D10 —** External memory data line 10.
P2.11/D11	124[5]	A8[5]	I/O	**D11 —** External memory data line 11.
P2.12/D12	125[5]	B7[5]	I/O	**D12 —** External memory data line 12.
P2.13/D13	127[5]	C7[5]	I/O	**D13 —** External memory data line 13.
P2.14/D14	129[5]	A6[5]	I/O	**D14 —** External memory data line 14.
P2.15/D15	130[5]	B6[5]	I/O	**D15 —** External memory data line 15.
P2.16/D16	131[5]	C6[5]	I/O	**D16 —** External memory data line 16.
P2.17/D17	132[5]	D6[5]	I/O	**D17 —** External memory data line 17.
P2.18/D18	133[5]	A5[5]	I/O	**D18 —** External memory data line 18.
P2.19/D19	134[5]	B5[5]	I/O	**D19 —** External memory data line 19.
P2.20/D20	136[5]	D5[5]	I/O	**D20 —** External memory data line 20.
P2.21/D21	137[5]	A4[5]	I/O	**D21 —** External memory data line 21.
P2.22/D22	1[5]	A1[5]	I/O	**D22 —** External memory data line 22.
P2.23/D23	10[5]	E3[5]	I/O	**D23 —** External memory data line 23.
P2.24/D24	11[5]	E2[5]	I/O	**D24 —** External memory data line 24.
P2.25/D25	12[5]	E1[5]	I/O	**D25 —** External memory data line 25.

Table 4. Pin description *...continued*

Symbol	Pin (LQFP)	Pin (TFBGA)	Type	Description
P3.19/A19	46[5]	L5[5]	O	**A19 —** External memory address line 19.
P3.20/A20	45[5]	K5[5]	O	**A20 —** External memory address line 20.
P3.21/A21	44[5]	N4[5]	O	**A21 —** External memory address line 21.
P3.22/A22	41[5]	K4[5]	O	**A22 —** External memory address line 22.
P3.23/A23/XCLK	40[5]	N3[5]	O	**A23 —** External memory address line 23.
			O	**XCLK —** Clock output.
P3.24/$\overline{CS3}$	36[5]	M2[5]	O	**$\overline{CS3}$ —** LOW-active Chip Select 3 signal. (Bank 3 addresses range 0x8300 0000 to 0x83FF FFFF)
P3.25/$\overline{CS2}$	35[5]	M1[5]	O	**$\overline{CS2}$ —** LOW-active Chip Select 2 signal. (Bank 2 addresses range 0x8200 0000 to 0x82FF FFFF)
P3.26/$\overline{CS1}$	30[5]	K2[5]	O	**$\overline{CS1}$ —** LOW-active Chip Select 1 signal. (Bank 1 addresses range 0x8100 0000 to 0x81FF FFFF)
P3.27/$\overline{WE}$	29[5]	K1[5]	O	**$\overline{WE}$ —** LOW-active Write enable signal.
P3.28/$\overline{BLS3}$/AIN7	28[2]	J4[2]	O	**$\overline{BLS3}$ —** LOW-active Byte Lane Select signal (Bank 3).
			I	**AIN7 —** ADC, input 7. This analog input is always connected to its pin.
P3.29/$\overline{BLS2}$/AIN6	27[4]	J3[4]	O	**$\overline{BLS2}$ —** LOW-active Byte Lane Select signal (Bank 2).
			I	**AIN6 —** ADC, input 6. This analog input is always connected to its pin.
P3.30/$\overline{BLS1}$	97[4]	E13[4]	O	**$\overline{BLS1}$ —** LOW-active Byte Lane Select signal (Bank 1).
P3.31/$\overline{BLS0}$	96[4]	F10[4]	O	**$\overline{BLS0}$ —** LOW-active Byte Lane Select signal (Bank 0).
n.c.	22[5]	H2[5]		Not connected. This pin MUST NOT be pulled LOW or the device might not operate properly.
$\overline{RESET}$	135[6]	C5[6]	I	**External reset input:** A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	142[7]	C3[7]	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	141[7]	B3[7]	O	Output from the oscillator amplifier.
V_{SS}	3, 9, 26, 38, 54, 67, 79, 93, 103, 107, 111, 128	C2, E4, J2, N2, N7, L10, K12, F13, D11, B13, B11, D7	I	**Ground:** 0 V reference.
V_{SSA}	139	C4	I	**Analog ground:** 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
$V_{SSA(PLL)}$	138	B4	I	**PLL analog ground:** 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
$V_{DD(1V8)}$	37, 110	N1, A12	I	**1.8 V core power supply:** This is the power supply voltage for internal circuitry.

6.8 Pin function select register 2 (PINSEL2 - 0xE002 C014)

The PINSEL2 register controls the functions of the pins as per the settings listed in Table 9. The direction control bit in the IODIR register is effective only when the GPIO function is selected for a pin. For other functions direction is controlled automatically. Settings other than those shown in Table 9 are reserved, and should not be used.

Table 9. Pin function select register 2 (PINSEL2 - 0xE002 C014)

PINSEL2 bits	Description				Reset value
1:0	reserved				-
2	When 0, pins P1[36:26] are used as GPIO pins. When 1, P1[31:26] are used as a Debug port.				$\overline{\text{P1.26/RTCK}}$
3	When 0, pins P1[25:16] are used as GPIO pins. When 1, P1[25:16] are used as a Trace port.				$\overline{\text{P1.20/ TRACESYNC}}$
5:4	Controls the use of the data bus and strobe pins:				BOOT1:0
	Pins P2[7:0]	11	= P2[7:0]	0x or 10 = D7 to D0	
	Pin P1.0	11	= P1.0	0x or 10 = $\overline{\text{CS0}}$	
	Pin P1.1	11	= P1.1	0x or 10 = $\overline{\text{OE}}$	
	Pin P3.31	11	= P3.31	0x or 10 = $\overline{\text{BLS0}}$	
	Pins P2[15:8]	00 or 11	= P2[15:8]	01 or 10 = D15 to D8	
	Pin P3.30	00 or 11	= P3.30	01 or 10 = $\overline{\text{BLS1}}$	
	Pins P2[27:16]	0x or 11	= P2[27:16]	10 = D27 to D16	
	Pins P2[29:28]	0x or 11	= P2[29:28]	10 = D29, D28	
	Pins P2[31:30]	0x or 11	= P2[31:30] or AIN5 to AIN4	10 = D31, D30	
	Pins P3[29:28]	0x or 11	= P3[29:28] or AIN7 to AIN6	10 = $\overline{\text{BLS2}}$, $\overline{\text{BLS3}}$	
6	If bits 5:4 are not 10, controls the use of pin P3.29: 0 enables P3.29, 1 enables AIN6.				1
7	If bits 5:4 are not 10, controls the use of pin P3.28: 0 enables P3.28, 1 enables AIN7.				1
8	Controls the use of pin P3.27: 0 enables P3.27, 1 enables $\overline{\text{WE}}$.				0
10:9	reserved				-
11	Controls the use of pin P3.26: 0 enables P3.26, 1 enables $\overline{\text{CS1}}$.				0
12	reserved				-
13	If bits 27:25 are not 111, controls the use of pin P3.23/A23/XCLK: 0 enables P3.23, 1 enables XCLK.				0
15:14	Controls the use of pin P3.25: 00 enables P3.25, 01 enables $\overline{\text{CS2}}$, 10 and 11 are reserved values.				00
17:16	Controls the use of pin P3.24: 00 enables P3.24, 01 enables $\overline{\text{CS3}}$, 10 and 11 are reserved values.				00
19:18	reserved				-
20	If bits 5:4 are not 10, controls the use of pin P2[29:28]: 0 enables P2[29:28], 1 is reserved				0
21	If bits 5:4 are not 10, controls the use of pin P2.30: 0 enables P2.30, 1 enables AIN4.				1
22	If bits 5:4 are not 10, controls the use of pin P2.31: 0 enables P2.31, 1 enables AIN5.				1

Table 9. Pin function select register 2 (PINSEL2 - 0xE002 C014) *…continued*

PINSEL2 bits	Description		Reset value
23	Controls whether P3.0/A0 is a port pin (0) or an address line (1).		1 if BOOT1:0 = 00 at $\overline{\text{RESET}}$ = 0, 0 otherwise
24	Controls whether P3.1/A1 is a port pin (0) or an address line (1).		$\overline{\text{BOOT1}}$ during reset
27:25	Controls the number of pins among P3.23/A23/XCLK and P3[22:2]/A2[22:2] that are address lines:		000 if BOOT1:0 = 11 at reset, 111 otherwise
	000 = None	100 = A11 to A2 are address lines.	
	001 = A3 to A2 are address lines.	101 = A15 to A2 are address lines.	
	010 = A5 to A2 are address lines.	110 = A19 to A2 are address lines.	
	011 = A7 to A2 are address lines.	111 = A23 to A2 are address lines.	
31:28	reserved		

6.9 External memory controller

The external static memory controller is a module which provides an interface between the system bus and external (off-chip) memory devices. It provides support for up to four independently configurable memory banks (16 MB each with byte lane enable control) simultaneously. Each memory bank is capable of supporting SRAM, ROM, flash EPROM, burst ROM memory, or some external I/O devices.

Each memory bank may be 8-bit, 16-bit, or 32-bit wide.

6.10 General purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

6.10.1 Features

- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

6.11 10-bit ADC

The LPC2210/2220 each contain a single 10-bit successive approximation ADC with eight multiplexed channels.

6.11.1 Features

- Measurement range of 0 V to 3 V.
- Capable of performing more than 400000 10-bit samples per second.
- Burst conversion mode for single or multiple inputs.

- Optional conversion on transition on input pin or Timer Match signal.

6.11.2 ADC features available in LPC2210/01 and LPC2220 only

- Every analog input has a dedicated result register to reduce interrupt overhead.
- Every analog input can generate an interrupt once the conversion is completed.
- The ADC pads are 5 V tolerant when configured for digital I/O function(s).

6.12 UARTs

The LPC2210/2220 each contain two UARTs. One UART provides a full modem control handshake interface, the other provides only transmit and receive data lines.

6.12.1 Features

- 16 B receive and transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in baud rate generator.
- Standard modem interface signals included on UART1.

6.12.2 UART features available in LPC2210/01 and LPC2220 only

Compared to previous LPC2000 microcontrollers, UARTs in LPC2210/01 and LPC2220 introduce a fractional baud rate generator for both UARTs, enabling these microcontrollers to achieve standard baud rates such as 115200 Bd with any crystal frequency above 2 MHz. In addition, auto-CTS/RTS flow-control functions are fully implemented in hardware.

- Fractional baud rate generator enables standard baud rates such as 115200 Bd to be achieved with any crystal frequency above 2 MHz.
- Auto-bauding.
- Auto-CTS/RTS flow-control fully implemented in hardware.

6.13 I^2C-bus serial I/O controller

The I^2C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL), and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C-bus is a multi-master bus, and it can be controlled by more than one bus master connected to it.

The I^2C-bus implemented in LPC2210/2220 supports a bit rate up to 400 kbit/s (fast I^2C-bus).

6.13.1 Features

- Compliant with standard I^2C-bus interface.
- Easy to configure as master, slave, or master/slave.

- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus may be used for test and diagnostic purposes.

6.14 SPI serial I/O controller

The LPC2210/2220 each contain two SPIs. The SPI is a full duplex serial interface, designed to be able to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

6.14.1 Features

- Compliant with SPI specification.
- Synchronous, serial, full duplex, communication.
- Combined SPI master and slave.
- Maximum data bit rate of one eighth of the input clock rate.

6.15 SSP controller

This peripheral is available in LPC2210/01 and LPC2220 only.

6.15.1 Features

- Compatible with Motorola’s SPI, Texas Instrument’s 4-wire SSI, and National Semiconductor’s Microwire buses.
- Synchronous serial communication.
- Master or slave operation.
- 8-frame FIFOs for both transmit and receive.
- 4 bits to 16 bits per frame.

6.15.2 Description

The SSP is a controller capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. Data transfers are in principle full duplex, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master.

While the SSP and SPI1 peripherals share the same physical pins, it is not possible to have both of these two peripherals active at the same time. Application can switch on the fly from SPI1 to SSP and back.

6.16 General purpose timers

The timer/counter is designed to count cycles of the peripheral clock (PCLK) or an externally supplied clock and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. It also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt. Multiple pins can be selected to perform a single capture or match function, providing an application with ‘or’ and ‘and’, as well as ‘broadcast’ functions among them.

6.16.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Timer operation (LPC2210/2220) or external event counter (LPC2210/01 and LPC2220 only).
- Four 32-bit capture channels per timer/counter that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Four external outputs per timer/counter corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

6.16.2 Features available in LPC2210/01 and LPC2220 only

The LPC2210/01 and LPC2220 can count external events on one of the capture inputs if the external pulse lasts at least one half of the period of the PCLK. In this configuration, unused capture lines can be selected as regular timer capture inputs or used as external interrupts.

- Timer can count cycles of either the peripheral clock (PCLK) or an externally supplied clock.
- When counting cycles of an externally supplied clock, only one of the timer’s capture inputs can be selected as the timer’s clock. The rate of such a clock is limited to PCLK / 4. Duration of high/low levels on the selected capture input cannot be shorter than 1 / (2PCLK).

6.20.5 Memory mapping control

The memory mapping control alters the mapping of the interrupt vectors that appear beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the BANK0 external memory, or to the on-chip static RAM. This allows code running in different memory spaces to have control of the interrupts.

6.20.6 Power control

The LPC2210/2220 support two reduced power modes: Idle mode and Power-down mode.

In Idle mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Idle mode and may generate interrupts to cause the processor to resume execution. Idle mode eliminates power used by the processor itself, memory systems and related controllers, and internal buses.

In Power-down mode, the oscillator is shut down, and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Power-down mode, and the logic levels of chip output pins remain static. The Power-down mode can be terminated and normal operation resumed by either a reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Power-down mode reduces chip power consumption to nearly zero.

A power control for peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings.

6.20.7 APB

The APB divider determines the relationship between the processor clock (CCLK) and the clock used by peripheral devices (PCLK). The APB divider serves two purposes. The first is to provide peripherals with the desired PCLK via APB so that they can operate at the speed chosen for the ARM processor. In order to achieve this, the APB may be slowed down to $\frac{1}{2}$ to $\frac{1}{4}$ of the processor clock rate. Because the APB must work properly at power-up (and its timing cannot be altered if it does not work since the APB divider control registers reside on the APB), the default condition at reset is for the APB to run at $\frac{1}{4}$ of the processor clock rate. The second purpose of the APB divider is to allow power savings when an application does not require any peripherals to run at the full processor rate. Because the APB divider is connected to the PLL output, the PLL remains active (if it was running) during Idle mode.

6.21 Emulation and debugging

The LPC2210/2220 support emulation and debugging via a JTAG serial port. A trace port allows tracing program execution. Debugging and trace functions are multiplexed only with GPIOs on Port 1. This means that all communication, timer and interface peripherals residing on Port 0 are available during the development and debugging phase as they are when the application is run in the embedded system itself.

8. Static characteristics

Table 11. Static characteristics

T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)		[2]	1.65	1.8	1.95	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		[3]	3.0	3.3	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)			2.5	3.3	3.6	V
Standard port pins, $\overline{\text{RESET}}$, RTCK							
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	3	µA
I_{IH}	HIGH-level input current	$V_I = V_{DD(3V3)}$; no pull-down		-	-	3	µA
I_{OZ}	OFF-state output current	V_O = 0 V, $V_O = V_{DD(3V3)}$; no pull-up/down		-	-	3	µA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; T_j < 125 °C		100	-	-	mA
V_I	input voltage		[4][5][6]	0	-	5.5	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	[7]	$V_{DD(3V3)}$ − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = −4 mA	[7]	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(3V3)}$ − 0.4 V	[7]	−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[7]	4	-	-	mA
I_{OHS}	HIGH-level short circuit output current	V_{OH} = 0 V	[8]	-	-	−45	mA
I_{OLS}	LOW-level short circuit output current	$V_{OL} = V_{DD(3V3)}$	[8]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[9]	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V	[10]	−15	−50	−85	µA
		$V_{DD(3V3)} < V_I$ < 5 V	[9]	0	0	0	µA
$I_{DD(act)}$	active mode supply current	$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 25 °C; code `while(1){}` executed from on-chip RAM; no active peripherals					
		CCLK = 60 MHz (LPC2210)		-	50	70	mA
		CCLK = 75 MHz (LPC2210/01; LPC2220)		-	50	70	mA

Table 12. ADC static characteristics

$V_{DDA(3V3)}$ = 2.5 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified. ADC frequency 4.5 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		0	-	$V_{DDA(3V3)}$	V
C_{ia}	analog input capacitance		-	-	1	pF
E_D	differential linearity error	[1][2][3]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity	[1][4]	-	-	±2	LSB
E_O	offset error	[1][5]	-	-	±3	LSB
E_G	gain error	[1][6]	-	-	±0.5	%
E_T	absolute error	[1][7]	-	-	±4	LSB

[1] Conditions: V_{SSA} = 0 V, $V_{DDA(3V3)}$ = 3.3 V.

[2] The ADC is monotonic, there are no missing codes.

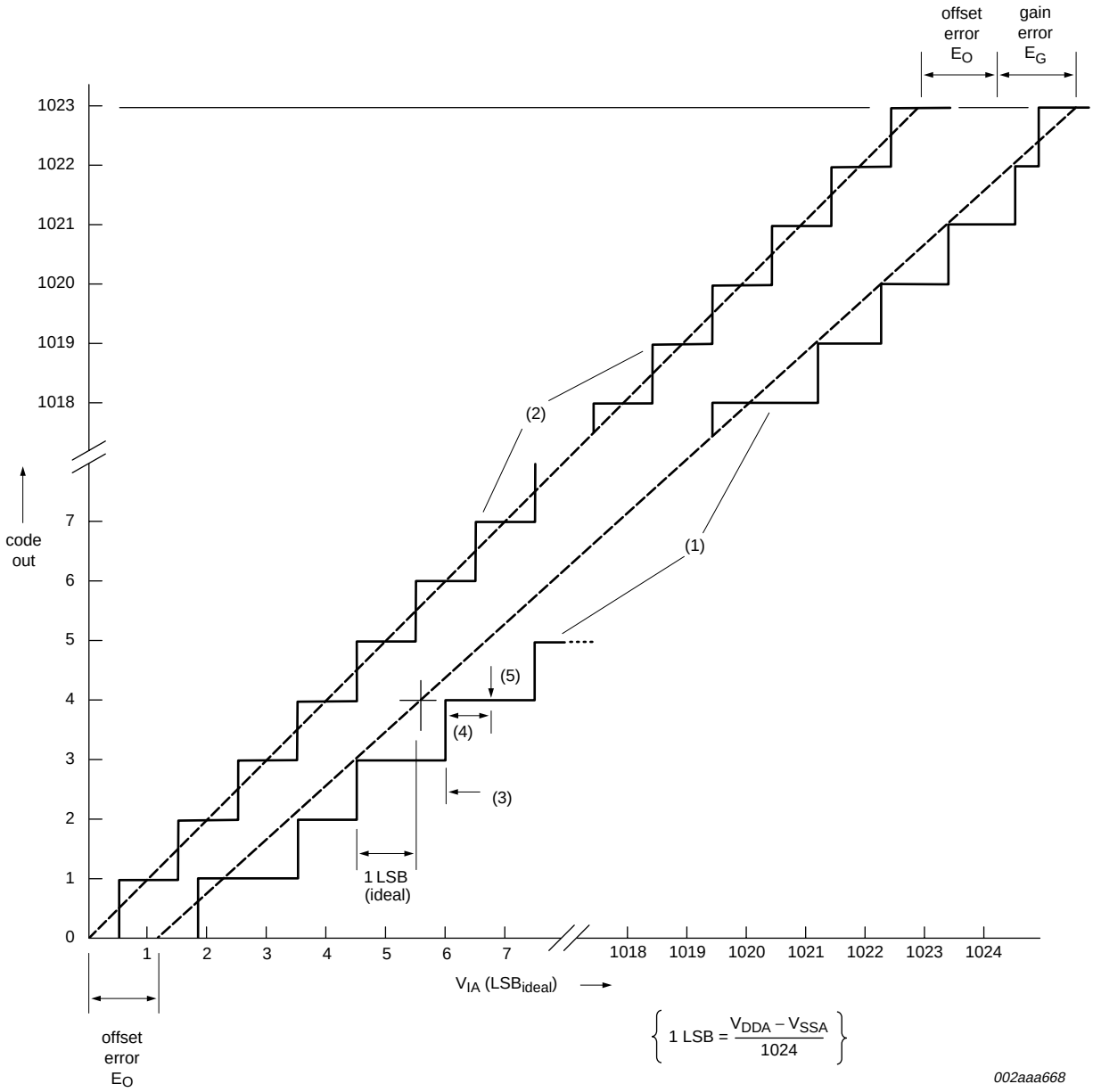
[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 5.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 5.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 5.

[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 5.

[7] The absolute voltage error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 5.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 5. ADC characteristics

9. Dynamic characteristics

Table 13. Dynamic characteristics

T_{amb} = 0 °C to +70 °C for commercial applications, −40 °C to +85 °C for industrial applications, $V_{DD(1V8)}$, $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External clock						
f_{osc}	oscillator frequency	supplied by an external oscillator (signal generator)	1	-	25	MHz
		external clock frequency supplied by an external crystal oscillator	1	-	25	MHz
		external clock frequency if on-chip PLL is used	10	-	25	MHz
		external clock frequency if on-chip bootloader is used for initial code download	10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		20	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (except P0.2 and P0.3)						
t_r	rise time		-	10	-	ns
t_f	fall time		-	10	-	ns
I^2C-bus pins (P0.2 and P0.3)						
t_f	fall time	V_{IH} to V_{IL} [2]	$20 + 0.1 \times C_b$	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Bus capacitance C_b in pF, from 10 pF to 400 pF.

Table 14. External memory interface dynamic characteristics *...continued*

C_L = 25 pF; T_{amb} = 40 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time		[2]	$(2 \times T_{cy(CCLK)}) - 5$	-	$(2 \times T_{cy(CCLK)}) + 5$	ns
t_{CHDV}	XCLK HIGH to data valid time			-	-	10	ns
t_{CHWEL}	XCLK HIGH to $\overline{WE}$ LOW time			-	-	10	ns
t_{CHBLSL}	XCLK HIGH to $\overline{BLS}$ LOW time			-	-	10	ns
t_{CHWEH}	XCLK HIGH to $\overline{WE}$ HIGH time			-	-	10	ns
t_{CHBLSH}	XCLK HIGH to $\overline{BLS}$ HIGH time			-	-	10	ns
t_{CHDNV}	XCLK HIGH to data invalid time			-	-	10	ns

[1] Except on initial access, in which case the address is set up $T_{cy(CCLK)}$ earlier.

[2] $T_{cy(CCLK)} = {}^{1}/_{CCLK}$.

[3] Latest of address valid, $\overline{CS}$ LOW, $\overline{OE}$ LOW to data valid.

[4] See the *LPC2210/20 user manual UM10114_1* for a description of the WSTn bits.

[5] Address valid to data valid.

[6] Earliest of $\overline{CS}$ HIGH, $\overline{OE}$ HIGH, address change to data invalid.

Table 15. Standard read access specifications

Access cycle	Max frequency	WST setting WST ≥ 0; round up to integer	Memory access time requirement
standard read	$f_{MAX} \leq \frac{2 + WST1}{t_{RAM} + 20\ ns}$	$WST1 \geq \frac{t_{RAM} + 20\ ns}{t_{cy(CCLK)}} - 2$	$t_{RAM} \leq t_{cy(CCLK)} \times (2 + WST1) - 20\ ns$
standard write	$f_{MAX} \leq \frac{1 + WST2}{t_{WRITE} + 5\ ns}$	$WST2 \geq \frac{t_{WRITE} - t_{CYC} + 5}{t_{cy(CCLK)}}$	$t_{WRITE} \leq t_{cy(CCLK)} \times (1 + WST2) - 5\ ns$
burst read - initial	$f_{MAX} \leq \frac{2 + WST1}{t_{INIT} + 20\ ns}$	$WST1 \geq \frac{t_{INIT} + 20\ ns}{t_{cy(CCLK)}} - 2$	$t_{INIT} \leq t_{cy(CCLK)} \times (2 + WST1) - 20\ ns$
burst read - subsequent 3×	$f_{MAX} \leq \frac{1}{t_{ROM} + 20\ ns}$	N/A	$t_{ROM} \leq t_{cy(CCLK)} - 20\ ns$

9.1 Timing

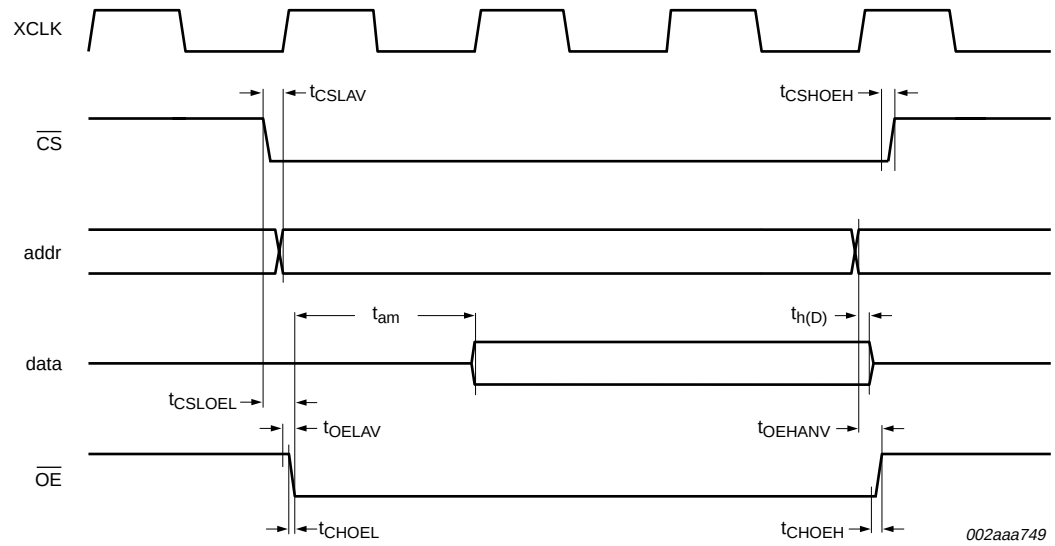


Fig 6. External memory read access

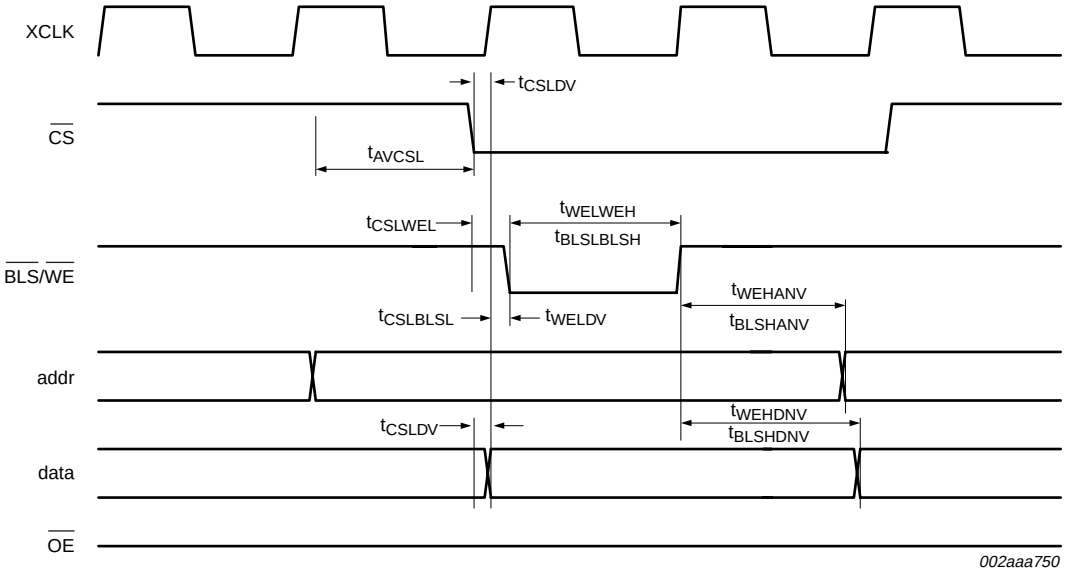
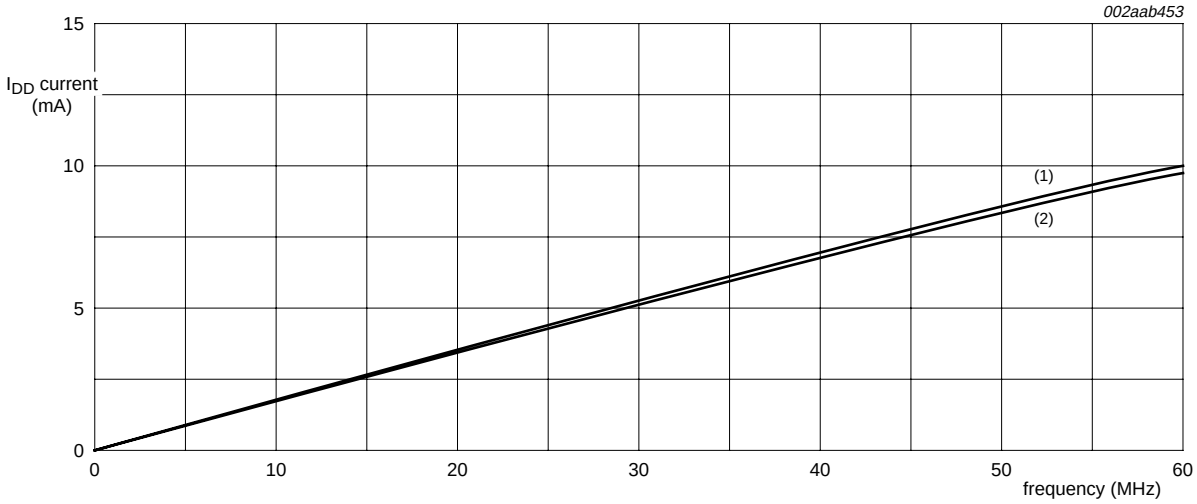


Fig 7. External memory write access

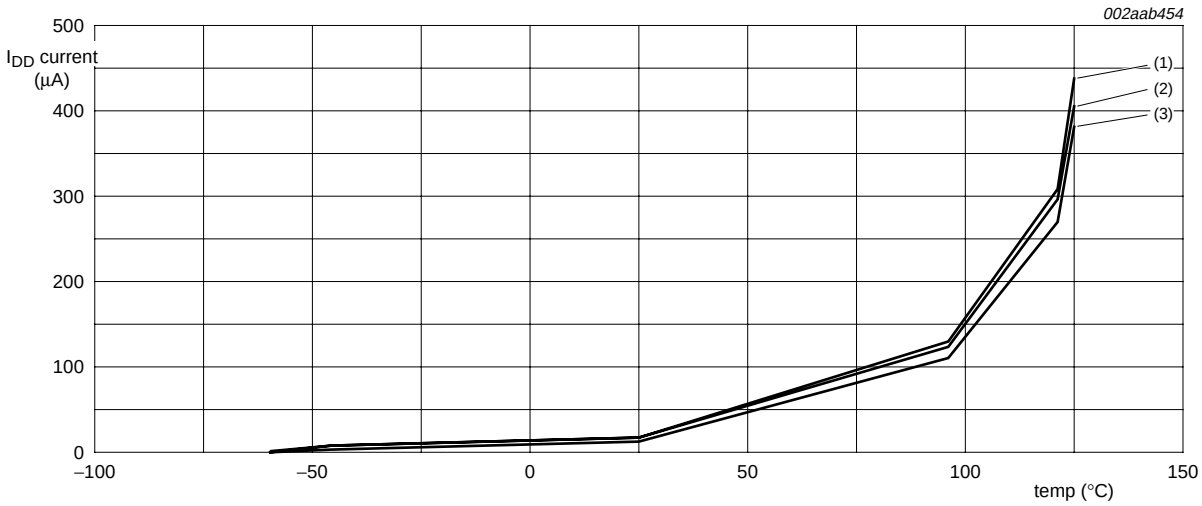


Test conditions: Idle mode entered executing code from on-chip RAM; all peripherals are enabled in PCONP register; PCLK = CCLK/4.

(1) 1.8 V core at 25 °C (typical)

(2) 1.65 V core at 25 °C (typical)

Fig 10. LPC2210 I_{DD} in Idle mode measured at different frequencies (CCLK) and temperatures



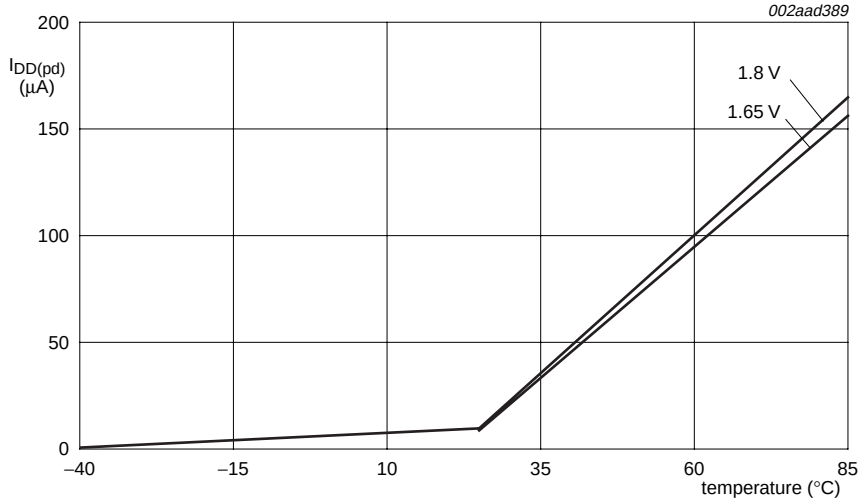
Test conditions: Power-down mode entered executing code from on-chip RAM; all peripherals are enabled in PCONP register.

(1) 1.95 V core

(2) 1.8 V core

(3) 1.65 V core

Fig 11. LPC2210 I_{DD} in Power-down mode measured at different temperatures

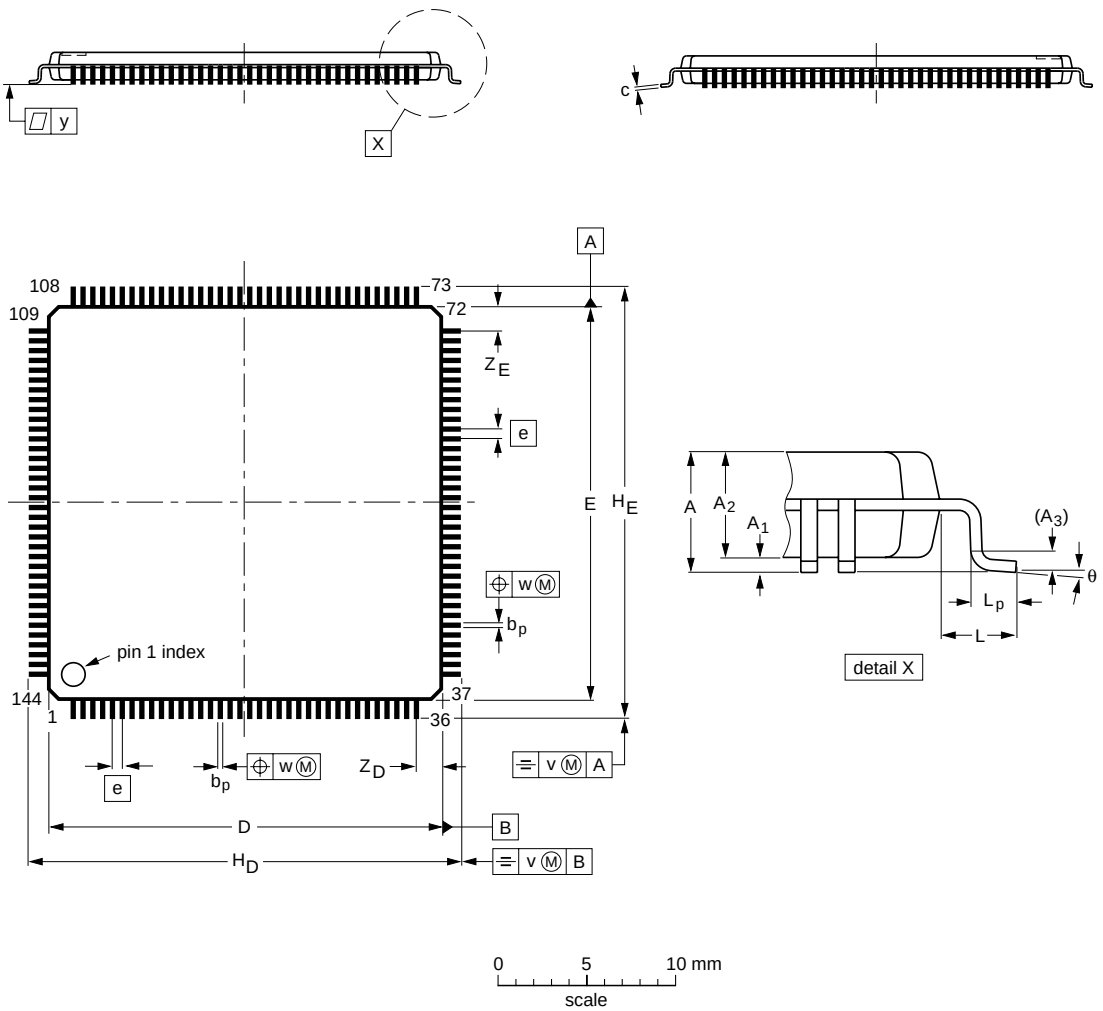


Test conditions: Power-down mode entered executing code from on-chip RAM; all peripherals are enabled in PCONP register.

Fig 14. LPC2220 and LPC2210/01 I_{DD} in Power-down mode measured at different temperatures

10. Package outline

LQFP144: plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm **SOT486-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	20.1 19.9	0.5	22.15 21.85	22.15 21.85	1	0.75 0.45	0.2	0.08	0.08	1.4 1.1	1.4 1.1	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT486-1	136E23	MS-026				~~00-03-14~~ 03-02-20

Fig 15. Package outline SOT486-1 (LQFP144)

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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