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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	EBI/EMI, I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	76
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2210fbd144-551

3.1 Ordering options

Table 2. Ordering options

Type number	RAM	Fast GPIO/ SSP/ Enhanced UART, ADC, Timer	Temperature range
LPC2210FBD144	16 kB	no	–40 °C to +85 °C
LPC2210FBD144/01	16 kB	yes	–40 °C to +85 °C
LPC2220FBD144	64 kB	yes	–40 °C to +85 °C
LPC2220FET144	64 kB	yes	–40 °C to +85 °C
LPC2220FET144/G	64 kB	yes	–40 °C to +85 °C

Table 4. Pin description *...continued*

Symbol	Pin (LQFP)	Pin (TFBGA)	Type	Description
P0.13/DTR1/ MAT1.1	85[1]	H10[1]	O	**DTR1 —** Data Terminal Ready output for UART1.
			O	**MAT1.1 —** Match output for Timer 1, channel 1.
P0.14/DCD1/ EINT1	92[2]	G10[2]	I	**DCD1 —** Data Carrier Detect input for UART1.
			I	**EINT1 —** External interrupt 1 input. Note: LOW on this pin while $\overline{\text{RESET}}$ is LOW forces on-chip bootloader to take over control of the part after reset.
P0.15/RI1/ EINT2	99[2]	E11[2]	I	**RI1 —** Ring Indicator input for UART1.
			I	**EINT2 —** External interrupt 2 input.
P0.16/EINT0/ MAT0.2/CAP0.2	100[2]	E10[2]	I	**EINT0 —** External interrupt 0 input.
			O	**MAT0.2 —** Match output for Timer 0, channel 2.
			I	**CAP0.2 —** Capture input for Timer 0, channel 2.
P0.17/CAP1.2/ SCK1/MAT1.2	101[1]	D13[1]	I	**CAP1.2 —** Capture input for Timer 1, channel 2.
			I/O	**SCK1 —** Serial Clock for SPI1/SSI/Microwire. SPI/SSI/Microwire clock output from master or input to slave.
			O	**MAT1.2 —** Match output for Timer 1, channel 2.
P0.18/CAP1.3/ MISO1/MAT1.3	121[1]	D8[1]	I	**CAP1.3 —** Capture input for Timer 1, channel 3.
			I/O	**MISO1 —** Master In Slave Out for SPI1. Data input to SPI master or data output from SPI slave.
			O	**MAT1.3 —** Match output for Timer 1, channel 3.
P0.19/MAT1.2/ MOSI1/CAP1.2	122[1]	C8[1]	O	**MAT1.2 —** Match output for Timer 1, channel 2.
			I/O	**MOSI1 —** Master Out Slave In for SPI1. Data output from SPI master or data input to SPI slave. • SPI interface: MOSI line. • SSI: DX/RX line (SPI1 as a master/slave). • Microwire: SO/SI line (SPI1 as a master/slave).
			I	**CAP1.2 —** Capture input for Timer 1, channel 2.
P0.20/MAT1.3/ SSEL1/ EINT3	123[2]	B8[2]	O	**MAT1.3 —** Match output for Timer 1, channel 3.
			I	**SSEL1 —** Slave Select for SPI1/Microwire. Used to select the SPI or Microwire interface as a slave. Frame synchronization in case of 4-wire SSI.
			I	**EINT3 —** External interrupt 3 input.
P0.21/PWM5/ CAP1.3	4[1]	C1[1]	O	**PWM5 —** Pulse Width Modulator output 5.
			I	**CAP1.3 —** Capture input for Timer 1, channel 3.
P0.22/CAP0.0/ MAT0.0	5[1]	D4[1]	I	**CAP0.0 —** Capture input for Timer 0, channel 0.
			O	**MAT0.0 —** Match output for Timer 0, channel 0.
P0.23	6[1]	D3[1]	I/O	General purpose bidirectional digital port only.
P0.24	8[1]	D1[1]	I/O	General purpose bidirectional digital port only.
P0.25	21[1]	H1[1]	I/O	General purpose bidirectional digital port only.
P0.27/AIN0/ CAP0.1/MAT0.1	23[4]	H3[4]	I	**AIN0 —** ADC, input 0. This analog input is always connected to its pin.
			I	**CAP0.1 —** Capture input for Timer 0, channel 1.
			O	**MAT0.1 —** Match output for Timer 0, channel 1.

Table 4. Pin description *...continued*

Symbol	Pin (LQFP)	Pin (TFBGA)	Type	Description
P1.26/RTCK	52[5]	N6[5]	I/O	**RTCK —** Returned Test Clock output. Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up. Note: LOW on this pin while $\overline{\text{RESET}}$ is LOW, enables pins P1[31:26] to operate as Debug port after reset.
P1.27/TDO	144[5]	B2[5]	O	**TDO —** Test Data out for JTAG interface.
P1.28/TDI	140[5]	A3[5]	I	**TDI —** Test Data in for JTAG interface.
P1.29/TCK	126[5]	A7[5]	I	**TCK —** Test Clock for JTAG interface. This clock must be slower than 1⁄6 of the CPU clock (CCLK) for the JTAG interface to operate.
P1.30/TMS	113[5]	D10[5]	I	**TMS —** Test Mode Select for JTAG interface.
P1.31/$\overline{\text{TRST}}$	43[5]	M4[5]	I	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface.
P2.0 to P2.31			I/O	**Port 2 —** Port 2 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 2 pins depends upon the pin function selected via the Pin Connect Block.
P2.0/D0	98[5]	E12[5]	I/O	**D0 —** External memory data line 0.
P2.1/D1	105[5]	C12[5]	I/O	**D1 —** External memory data line 1.
P2.2/D2	106[5]	C11[5]	I/O	**D2 —** External memory data line 2.
P2.3/D3	108[5]	B12[5]	I/O	**D3 —** External memory data line 3.
P2.4/D4	109[5]	A13[5]	I/O	**D4 —** External memory data line 4.
P2.5/D5	114[5]	C10[5]	I/O	**D5 —** External memory data line 5.
P2.6/D6	115[5]	B10[5]	I/O	**D6 —** External memory data line 6.
P2.7/D7	116[5]	A10[5]	I/O	**D7 —** External memory data line 7.
P2.8/D8	117[5]	D9[5]	I/O	**D8 —** External memory data line 8.
P2.9/D9	118[5]	C9[5]	I/O	**D9 —** External memory data line 9.
P2.10/D10	120[5]	A9[5]	I/O	**D10 —** External memory data line 10.
P2.11/D11	124[5]	A8[5]	I/O	**D11 —** External memory data line 11.
P2.12/D12	125[5]	B7[5]	I/O	**D12 —** External memory data line 12.
P2.13/D13	127[5]	C7[5]	I/O	**D13 —** External memory data line 13.
P2.14/D14	129[5]	A6[5]	I/O	**D14 —** External memory data line 14.
P2.15/D15	130[5]	B6[5]	I/O	**D15 —** External memory data line 15.
P2.16/D16	131[5]	C6[5]	I/O	**D16 —** External memory data line 16.
P2.17/D17	132[5]	D6[5]	I/O	**D17 —** External memory data line 17.
P2.18/D18	133[5]	A5[5]	I/O	**D18 —** External memory data line 18.
P2.19/D19	134[5]	B5[5]	I/O	**D19 —** External memory data line 19.
P2.20/D20	136[5]	D5[5]	I/O	**D20 —** External memory data line 20.
P2.21/D21	137[5]	A4[5]	I/O	**D21 —** External memory data line 21.
P2.22/D22	1[5]	A1[5]	I/O	**D22 —** External memory data line 22.
P2.23/D23	10[5]	E3[5]	I/O	**D23 —** External memory data line 23.
P2.24/D24	11[5]	E2[5]	I/O	**D24 —** External memory data line 24.
P2.25/D25	12[5]	E1[5]	I/O	**D25 —** External memory data line 25.

Table 4. Pin description *...continued*

Symbol	Pin (LQFP)	Pin (TFBGA)	Type	Description
P2.26/D26/ BOOT0	13[5]	F4[5]	I/O	**D26 —** External memory data line 26.
			I	**BOOT0 —** While $\overline{\text{RESET}}$ is LOW, together with BOOT1 controls booting and internal operation. Internal pull-up ensures HIGH state if pin is left unconnected.
P2.27/D27/ BOOT1	16[5]	F1[5]	I/O	**D27 —** External memory data line 27.
			I	**BOOT1 —** While $\overline{\text{RESET}}$ is LOW, together with BOOT0 controls booting and internal operation. Internal pull-up ensures HIGH state if pin is left unconnected. BOOT1:0 = 00 selects 8-bit memory on $\overline{\text{CS0}}$ for boot. BOOT1:0 = 01 selects 16-bit memory on $\overline{\text{CS0}}$ for boot. BOOT1:0 = 10 selects 32-bit memory on $\overline{\text{CS0}}$ for boot. BOOT1:0 = 11 selects 16-bit memory on $\overline{\text{CS0}}$ for boot.
P2.28/D28	17[5]	G2[5]	I/O	**D28 —** External memory data line 28.
P2.29/D29	18[5]	G1[5]	I/O	**D29 —** External memory data line 29.
P2.30/D30/ AIN4	19[2]	G3[2]	I/O	**D30 —** External memory data line 30.
			I	**AIN4 —** ADC, input 4. This analog input is always connected to its pin.
P2.31/D31/ AIN5	20[2]	G4[2]	I/O	**D31 —** External memory data line 31.
			I	**AIN5 —** ADC, input 5. This analog input is always connected to its pin.
P3.0 to P3.31			I/O	**Port 3 —** Port 3 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 3 pins depends upon the pin function selected via the Pin Connect Block.
P3.0/A0	89[5]	G12[5]	O	**A0 —** External memory address line 0.
P3.1/A1	88[5]	H13[5]	O	**A1 —** External memory address line 1.
P3.2/A2	87[5]	H12[5]	O	**A2 —** External memory address line 2.
P3.3/A3	81[5]	J10[5]	O	**A3 —** External memory address line 3.
P3.4/A4	80[5]	K13[5]	O	**A4 —** External memory address line 4.
P3.5/A5	74[5]	M13[5]	O	**A5 —** External memory address line 5.
P3.6/A6	73[5]	N13[5]	O	**A6 —** External memory address line 6.
P3.7/A7	72[5]	M12[5]	O	**A7 —** External memory address line 7.
P3.8/A8	71[5]	N12[5]	O	**A8 —** External memory address line 8.
P3.9/A9	66[5]	M10[5]	O	**A9 —** External memory address line 9.
P3.10/A10	65[5]	N10[5]	O	**A10 —** External memory address line 10.
P3.11/A11	64[5]	K9[5]	O	**A11 —** External memory address line 11.
P3.12/A12	63[5]	L9[5]	O	**A12 —** External memory address line 12.
P3.13/A13	62[5]	M9[5]	O	**A13 —** External memory address line 13.
P3.14/A14	56[5]	K7[5]	O	**A14 —** External memory address line 14.
P3.15/A15	55[5]	L7[5]	O	**A15 —** External memory address line 15.
P3.16/A16	53[5]	M7[5]	O	**A16 —** External memory address line 16.
P3.17/A17	48[5]	N5[5]	O	**A17 —** External memory address line 17.
P3.18/A18	47[5]	M5[5]	O	**A18 —** External memory address line 18.

Table 4. Pin description *...continued*

Symbol	Pin (LQFP)	Pin (TFBGA)	Type	Description
$V_{DDA(1V8)}$	143	A2	I	**Analog 1.8 V core power supply:** This is the power supply voltage for internal circuitry. This should be nominally the same voltage as $V_{DD(1V8)}$ but should be isolated to minimize noise and error.
$V_{DD(3V3)}$	2, 31, 39, 51, 57, 77, 94, 104, 112, 119	B1, K3, M3, M6, N8, K10, F12, C13, A11, B9	I	**3.3 V pad power supply:** This is the power supply voltage for the I/O ports.
$V_{DDA(3V3)}$	14	F3	I	**Analog 3.3 V pad power supply:** This should be nominally the same voltage as $V_{DD(3V3)}$ but should be isolated to minimize noise and error.

[1] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control.

[2] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. If configured for an input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns.

[3] Open drain 5 V tolerant digital I/O I^2C-bus 400 kHz specification compatible pad. It requires external pull-up to provide an output functionality.

[4] 5 V tolerant pad providing digital I/O (with TTL levels and hysteresis and 10 ns slew rate control) and analog input function. If configured for a digital input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns. When configured as an ADC input, digital section of the pad is disabled.

[5] 5 V tolerant pad with built-in pull-up resistor providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. The pull-up resistor's value ranges from 60 kΩ to 300 kΩ.

[6] 5 V tolerant pad providing digital input (with TTL levels and hysteresis) function only.

[7] Pad provides special analog functionality.

6. Functional description

6.1 Architectural overview

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on RISC principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed CISC. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set.
- A 16-bit Thumb set.

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

6.2 On-chip SRAM

On-chip SRAM may be used for code and/or data storage. The SRAM may be accessed as 8-bit, 16-bit, and 32-bit. The LPC2210 and LPC2210/01 provide 16 kB of static RAM, and the LPC2220 provides 64 kB of static RAM.

6.3 Memory map

The LPC2210/2220 memory maps incorporate several distinct regions, as shown in Figure 4.

In addition, the CPU interrupt vectors may be re-mapped to allow them to reside in either on-chip bootloader, external memory BANK0 or on-chip static RAM. This is described in Section 6.20 "System control".

Non-vectored IRQs have the lowest priority.

The VIC combines the requests from all the vectored and non-vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping there. If any of the vectored IRQs are requesting, the VIC provides the address of the highest-priority requesting IRQs service routine, otherwise it provides the address of a default routine that is shared by all the non-vectored IRQs. The default routine can read another VIC register to see what IRQs are active.

6.4.1 Interrupt sources

Table 5 lists the interrupt sources for each peripheral function. Each peripheral device has one interrupt line connected to the VIC, but may have several internal interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Table 5. Interrupt sources

Block	Flag(s)	VIC channel #
WDT	Watchdog Interrupt (WDINT)	0
-	Reserved for software interrupts only	1
ARM Core	EmbeddedICE, DbgCommRX	2
ARM Core	EmbeddedICE, DbgCommTX	3
TIMER0	Match 0 to 3 (MR0, MR1, MR2, MR3)	4
TIMER1	Match 0 to 3 (MR0, MR1, MR2, MR3)	5
UART0	RX Line Status (RLS) Transmit Holding Register Empty (THRE) RX Data Available (RDA) Character Time-out Indicator (CTI)	6
UART1	RX Line Status (RLS) Transmit Holding Register empty (THRE) RX Data Available (RDA) Character Time-out Indicator (CTI) Modem Status Interrupt (MSI)	7
PWM0	Match 0 to 6 (MR0, MR1, MR2, MR3, MR4, MR5, MR6)	8
I^2C	SI (state change)	9
SPI0	SPIF, MODF	10
SPI1 and SSP	SPIF, MODF and TXRIS, RXRIS, RTRIS, RORRIS	11
PLL	PLL Lock (PLOCK)	12
RTC	RTCCIF (Counter Increment), RTCALF (Alarm)	13
System Control	External Interrupt 0 (EINT0)	14
	External Interrupt 1 (EINT1)	15
	External Interrupt 2 (EINT2)	16
	External Interrupt 3 (EINT3)	17
A/D	ADC	18

Table 7. Pin function select register 0 (PINSEL0 - 0xE002 C000) *...continued*

PINSEL0	Pin name	Value		Function	Value after reset
31:30	P0.15	0	0	GPIO Port 0.15	0
		0	1	RI1 (UART1)	
		1	0	EINT2	
		1	1	reserved	

6.7 Pin function select register 1 (PINSEL1 - 0xE002 C004)

The PINSEL1 register controls the functions of the pins as per the settings listed in Table 8. The direction control bit in the IODIR register is effective only when the GPIO function is selected for a pin. For other functions direction is controlled automatically. Settings other than those shown in the Table 8 are reserved, and should not be used.

Table 8. Pin function select register 1 (PINSEL1 - 0xE002 C004)

PINSEL1	Pin name	Value		Function	Value after reset
1:0	P0.16	0	0	GPIO Port 0.16	0
		0	1	EINT0	
		1	0	Match 0.2 (Timer 0)	
		1	1	Capture 0.2 (Timer 0)	
3:2	P0.17	0	0	GPIO Port 0.17	0
		0	1	Capture 1.2 (Timer 1)	
		1	0	SCK (SPI1)	
		1	1	Match 1.2 (Timer 1)	
5:4	P0.18	0	0	GPIO Port 0.18	0
		0	1	Capture 1.3 (Timer 1)	
		1	0	MISO (SPI1)	
		1	1	Match 1.3 (Timer 1)	
7:6	P0.19	0	0	GPIO Port 0.19	0
		0	1	Match 1.2 (Timer 1)	
		1	0	MOSI (SPI1)	
		1	1	Capture 1.2 (Timer 1)	
9:8	P0.20	0	0	GPIO Port 0.20	0
		0	1	Match 1.3 (Timer 1)	
		1	0	SSEL (SPI1)	
		1	1	EINT3	
11:10	P0.21	0	0	GPIO Port 0.21	0
		0	1	PWM5	
		1	0	reserved	
		1	1	Capture 1.3 (Timer 1)	
13:12	P0.22	0	0	GPIO Port 0.22	0
		0	1	reserved	
		1	0	Capture 0.0 (Timer 0)	
		1	1	Match 0.0 (Timer 0)	

6.8 Pin function select register 2 (PINSEL2 - 0xE002 C014)

The PINSEL2 register controls the functions of the pins as per the settings listed in Table 9. The direction control bit in the IODIR register is effective only when the GPIO function is selected for a pin. For other functions direction is controlled automatically. Settings other than those shown in Table 9 are reserved, and should not be used.

Table 9. Pin function select register 2 (PINSEL2 - 0xE002 C014)

PINSEL2 bits	Description				Reset value
1:0	reserved				-
2	When 0, pins P1[36:26] are used as GPIO pins. When 1, P1[31:26] are used as a Debug port.				$\overline{\text{P1.26/RTCK}}$
3	When 0, pins P1[25:16] are used as GPIO pins. When 1, P1[25:16] are used as a Trace port.				$\overline{\text{P1.20/ TRACESYNC}}$
5:4	Controls the use of the data bus and strobe pins:				BOOT1:0
	Pins P2[7:0]	11	= P2[7:0]	0x or 10 = D7 to D0	
	Pin P1.0	11	= P1.0	0x or 10 = $\overline{\text{CS0}}$	
	Pin P1.1	11	= P1.1	0x or 10 = $\overline{\text{OE}}$	
	Pin P3.31	11	= P3.31	0x or 10 = $\overline{\text{BLS0}}$	
	Pins P2[15:8]	00 or 11	= P2[15:8]	01 or 10 = D15 to D8	
	Pin P3.30	00 or 11	= P3.30	01 or 10 = $\overline{\text{BLS1}}$	
	Pins P2[27:16]	0x or 11	= P2[27:16]	10 = D27 to D16	
	Pins P2[29:28]	0x or 11	= P2[29:28]	10 = D29, D28	
	Pins P2[31:30]	0x or 11	= P2[31:30] or AIN5 to AIN4	10 = D31, D30	
	Pins P3[29:28]	0x or 11	= P3[29:28] or AIN7 to AIN6	10 = $\overline{\text{BLS2}}$, $\overline{\text{BLS3}}$	
6	If bits 5:4 are not 10, controls the use of pin P3.29: 0 enables P3.29, 1 enables AIN6.				1
7	If bits 5:4 are not 10, controls the use of pin P3.28: 0 enables P3.28, 1 enables AIN7.				1
8	Controls the use of pin P3.27: 0 enables P3.27, 1 enables $\overline{\text{WE}}$.				0
10:9	reserved				-
11	Controls the use of pin P3.26: 0 enables P3.26, 1 enables $\overline{\text{CS1}}$.				0
12	reserved				-
13	If bits 27:25 are not 111, controls the use of pin P3.23/A23/XCLK: 0 enables P3.23, 1 enables XCLK.				0
15:14	Controls the use of pin P3.25: 00 enables P3.25, 01 enables $\overline{\text{CS2}}$, 10 and 11 are reserved values.				00
17:16	Controls the use of pin P3.24: 00 enables P3.24, 01 enables $\overline{\text{CS3}}$, 10 and 11 are reserved values.				00
19:18	reserved				-
20	If bits 5:4 are not 10, controls the use of pin P2[29:28]: 0 enables P2[29:28], 1 is reserved				0
21	If bits 5:4 are not 10, controls the use of pin P2.30: 0 enables P2.30, 1 enables AIN4.				1
22	If bits 5:4 are not 10, controls the use of pin P2.31: 0 enables P2.31, 1 enables AIN5.				1

Table 9. Pin function select register 2 (PINSEL2 - 0xE002 C014) *…continued*

PINSEL2 bits	Description		Reset value
23	Controls whether P3.0/A0 is a port pin (0) or an address line (1).		1 if BOOT1:0 = 00 at $\overline{\text{RESET}}$ = 0, 0 otherwise
24	Controls whether P3.1/A1 is a port pin (0) or an address line (1).		$\overline{\text{BOOT1}}$ during reset
27:25	Controls the number of pins among P3.23/A23/XCLK and P3[22:2]/A2[22:2] that are address lines:		000 if BOOT1:0 = 11 at reset, 111 otherwise
	000 = None	100 = A11 to A2 are address lines.	
	001 = A3 to A2 are address lines.	101 = A15 to A2 are address lines.	
	010 = A5 to A2 are address lines.	110 = A19 to A2 are address lines.	
	011 = A7 to A2 are address lines.	111 = A23 to A2 are address lines.	
31:28	reserved		

6.9 External memory controller

The external static memory controller is a module which provides an interface between the system bus and external (off-chip) memory devices. It provides support for up to four independently configurable memory banks (16 MB each with byte lane enable control) simultaneously. Each memory bank is capable of supporting SRAM, ROM, flash EPROM, burst ROM memory, or some external I/O devices.

Each memory bank may be 8-bit, 16-bit, or 32-bit wide.

6.10 General purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

6.10.1 Features

- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

6.11 10-bit ADC

The LPC2210/2220 each contain a single 10-bit successive approximation ADC with eight multiplexed channels.

6.11.1 Features

- Measurement range of 0 V to 3 V.
- Capable of performing more than 400000 10-bit samples per second.
- Burst conversion mode for single or multiple inputs.

6.20.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 60 MHz (LPC2210) and 10 MHz to 75 MHz (LPC2210/01 and LPC2220) with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 µs.

6.20.3 Reset and wake-up timer

Reset has two sources on the LPC2210/2220: the $\overline{\text{RESET}}$ pin and watchdog reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip reset by any source starts the wake-up timer (see wake-up timer description below), causing the internal chip reset to remain asserted until the external reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip circuitry has completed its initialization.

When the internal reset is removed, the processor begins executing at address 0, which is the reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The wake-up timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power-on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the wake-up timer.

The wake-up timer monitors the crystal oscillator as the means of checking whether it is safe to begin code execution. When power is applied to the chip, or some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of V_{DD} ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g. capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

6.20.4 External interrupt inputs

The LPC2210/2220 include up to nine edge or level sensitive external interrupt inputs as selectable pin functions. When the pins are combined, external events can be processed as four independent interrupt signals. The external interrupt inputs can optionally be used to wake up the processor from Power-down mode.

6.20.5 Memory mapping control

The memory mapping control alters the mapping of the interrupt vectors that appear beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the BANK0 external memory, or to the on-chip static RAM. This allows code running in different memory spaces to have control of the interrupts.

6.20.6 Power control

The LPC2210/2220 support two reduced power modes: Idle mode and Power-down mode.

In Idle mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Idle mode and may generate interrupts to cause the processor to resume execution. Idle mode eliminates power used by the processor itself, memory systems and related controllers, and internal buses.

In Power-down mode, the oscillator is shut down, and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Power-down mode, and the logic levels of chip output pins remain static. The Power-down mode can be terminated and normal operation resumed by either a reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Power-down mode reduces chip power consumption to nearly zero.

A power control for peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings.

6.20.7 APB

The APB divider determines the relationship between the processor clock (CCLK) and the clock used by peripheral devices (PCLK). The APB divider serves two purposes. The first is to provide peripherals with the desired PCLK via APB so that they can operate at the speed chosen for the ARM processor. In order to achieve this, the APB may be slowed down to $\frac{1}{2}$ to $\frac{1}{4}$ of the processor clock rate. Because the APB must work properly at power-up (and its timing cannot be altered if it does not work since the APB divider control registers reside on the APB), the default condition at reset is for the APB to run at $\frac{1}{4}$ of the processor clock rate. The second purpose of the APB divider is to allow power savings when an application does not require any peripherals to run at the full processor rate. Because the APB divider is connected to the PLL output, the PLL remains active (if it was running) during Idle mode.

6.21 Emulation and debugging

The LPC2210/2220 support emulation and debugging via a JTAG serial port. A trace port allows tracing program execution. Debugging and trace functions are multiplexed only with GPIOs on Port 1. This means that all communication, timer and interface peripherals residing on Port 0 are available during the development and debugging phase as they are when the application is run in the embedded system itself.

6.21.1 EmbeddedICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol converter. EmbeddedICE protocol converter converts the remote debug protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a Debug Communication Channel (DCC) function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The debug communication channel is accessed as a co-processor 14 by the program running on the ARM7TDMI-S core. The debug communication channel allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The debug communication channel data and control registers are mapped in to addresses in the EmbeddedICE logic.

The JTAG clock (TCK) must be slower than $1/6$ of the CPU clock (CCLK) for the JTAG interface to operate.

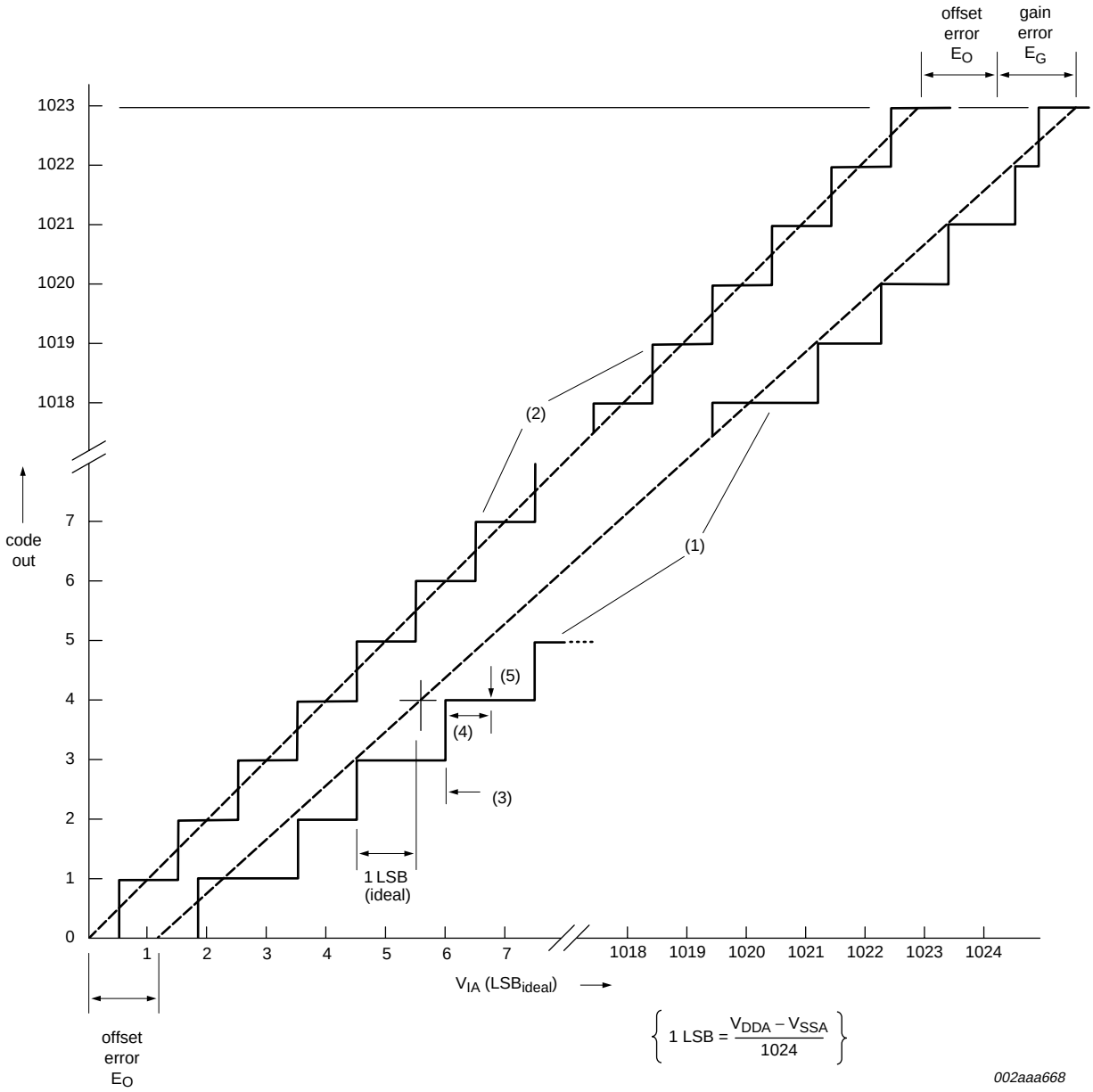
6.21.2 Embedded trace

Since the LPC2210/2220 have significant amounts of on-chip memory, it is not possible to determine how the processor core is operating simply by observing the external pins. The Embedded Trace Macrocell (ETM) provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to the trace port.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external trace port analyzer must capture the trace information under software debugger control. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code cannot be traced because of this restriction.

6.21.3 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real-time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the debug communication channel, which is present in the EmbeddedICE logic. The LPC2210/2220 contain a specific configuration of RealMonitor software programmed into the on-chip flash memory.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 5. ADC characteristics

9. Dynamic characteristics

Table 13. Dynamic characteristics

T_{amb} = 0 °C to +70 °C for commercial applications, −40 °C to +85 °C for industrial applications, $V_{DD(1V8)}$, $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External clock						
f_{osc}	oscillator frequency	supplied by an external oscillator (signal generator)	1	-	25	MHz
		external clock frequency supplied by an external crystal oscillator	1	-	25	MHz
		external clock frequency if on-chip PLL is used	10	-	25	MHz
		external clock frequency if on-chip bootloader is used for initial code download	10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		20	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (except P0.2 and P0.3)						
t_r	rise time		-	10	-	ns
t_f	fall time		-	10	-	ns
I^2C-bus pins (P0.2 and P0.3)						
t_f	fall time	V_{IH} to V_{IL} [2]	$20 + 0.1 \times C_b$	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Bus capacitance C_b in pF, from 10 pF to 400 pF.

Table 14. External memory interface dynamic characteristics

C_L = 25 pF; T_{amb} = 40 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Common to read and write cycles						
t_{CHAV}	XCLK HIGH to address valid time		-	-	10	ns
t_{CHCSL}	XCLK HIGH to $\overline{CS}$ LOW time		-	-	10	ns
t_{CHCSH}	XCLK HIGH to $\overline{CS}$ HIGH time		-	-	10	ns
t_{CHANV}	XCLK HIGH to address invalid time		-	-	10	ns
Read cycle parameters						
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	[1]	–5	-	+10	ns
t_{OELAV}	$\overline{OE}$ LOW to address valid time	[1]	–5	-	+10	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time		–5	-	+5	ns
t_{am}	memory access time	[2][3] [4]	$(T_{cy(CCLK)} \times (2 + WST1)) + (-20)$	-	-	ns
$t_{am(ibr)}$	memory access time (initial burst-ROM)	[2][3] [4]	$(T_{cy(CCLK)} \times (2 + WST1)) + (-20)$	-	-	ns
$t_{am(sbr)}$	memory access time (subsequent burst-ROM)	[2][5]	$T_{cy(CCLK)} + (-20)$	-	-	ns
$t_{h(D)}$	data hold time	[6]	0	-	-	ns
t_{CSHOEH}	$\overline{CS}$ HIGH to $\overline{OE}$ HIGH time		–5	-	+5	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid time		–5	-	+5	ns
t_{CHOEL}	XCLK HIGH to $\overline{OE}$ LOW time		–5	-	+5	ns
t_{CHOEH}	XCLK HIGH to $\overline{OE}$ HIGH time		–5	-	+5	ns
Write cycle parameters						
t_{AVCSL}	address valid to $\overline{CS}$ LOW time	[1]	$T_{cy(CCLK)} - 10$	-	-	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time		–5	-	+5	ns
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time		–5	-	+5	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time		–5	-	+5	ns
t_{WELDV}	$\overline{WE}$ LOW to data valid time		–5	-	+5	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time		–5	-	+5	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	[2][4]	$T_{cy(CCLK)} \times (1 + WST2) - 5$	-	$T_{cy(CCLK)} \times (1 + WST2) + 5$	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	[2][4]	$T_{cy(CCLK)} \times (1 + WST2) - 5$	-	$T_{cy(CCLK)} \times (1 + WST2) + 5$	ns
t_{WEHANV}	$\overline{WE}$ HIGH to address invalid time	[2]	$T_{cy(CCLK)} - 5$	-	$T_{cy(CCLK)} + 5$	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time	[2]	$(2 \times T_{cy(CCLK)}) - 5$	-	$(2 \times T_{cy(CCLK)}) + 5$	ns
$t_{BLSHANV}$	$\overline{BLS}$ HIGH to address invalid time	[2]	$T_{cy(CCLK)} - 5$	-	$T_{cy(CCLK)} + 5$	ns

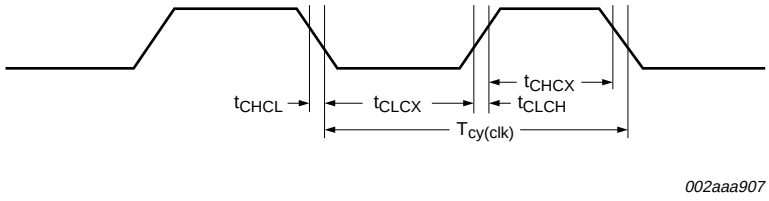
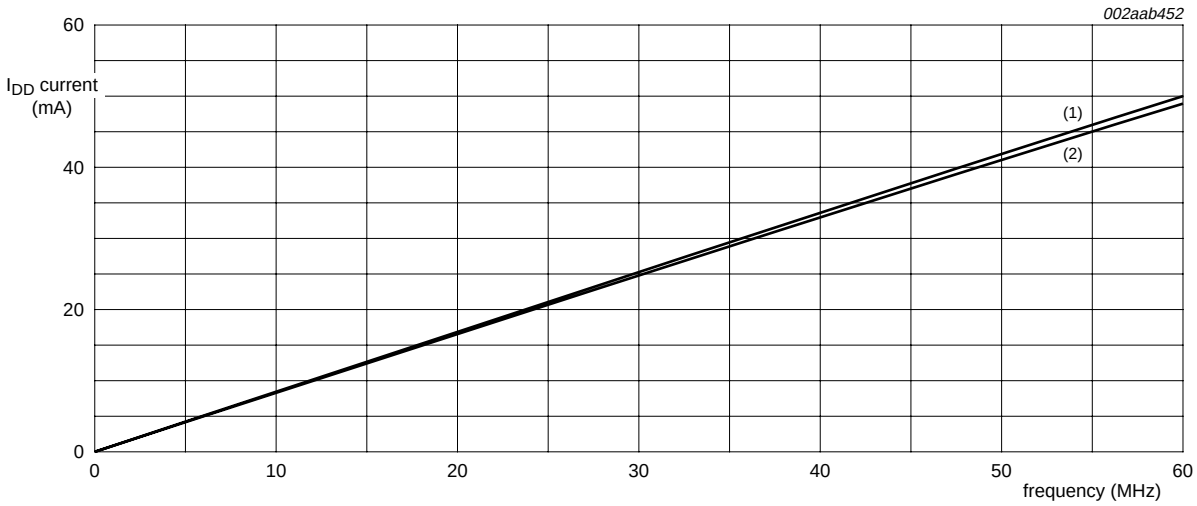


Fig 8. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

9.2 LPC2210 power consumption measurements

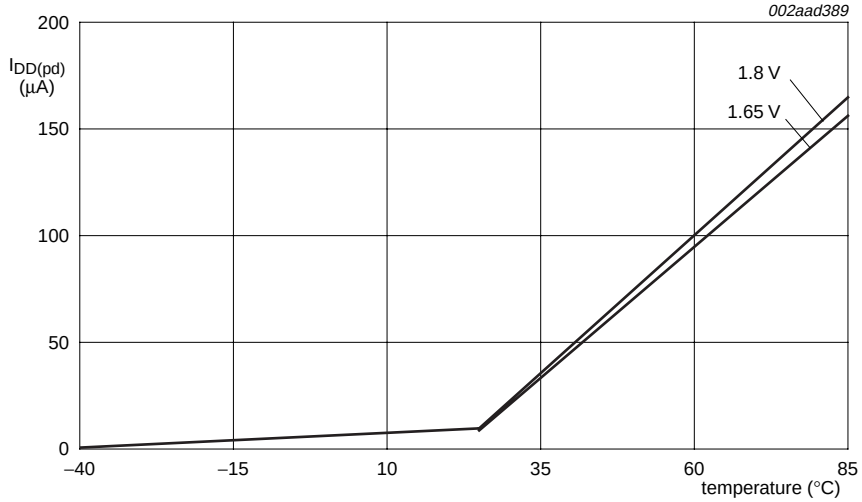


Test conditions: code executed from on-chip RAM; all peripherals are enabled in PCONP register; PCLK = CCLK/4.

(1) 1.8 V core at 25 °C (typical)

(2) 1.65 V core at 25 °C (typical)

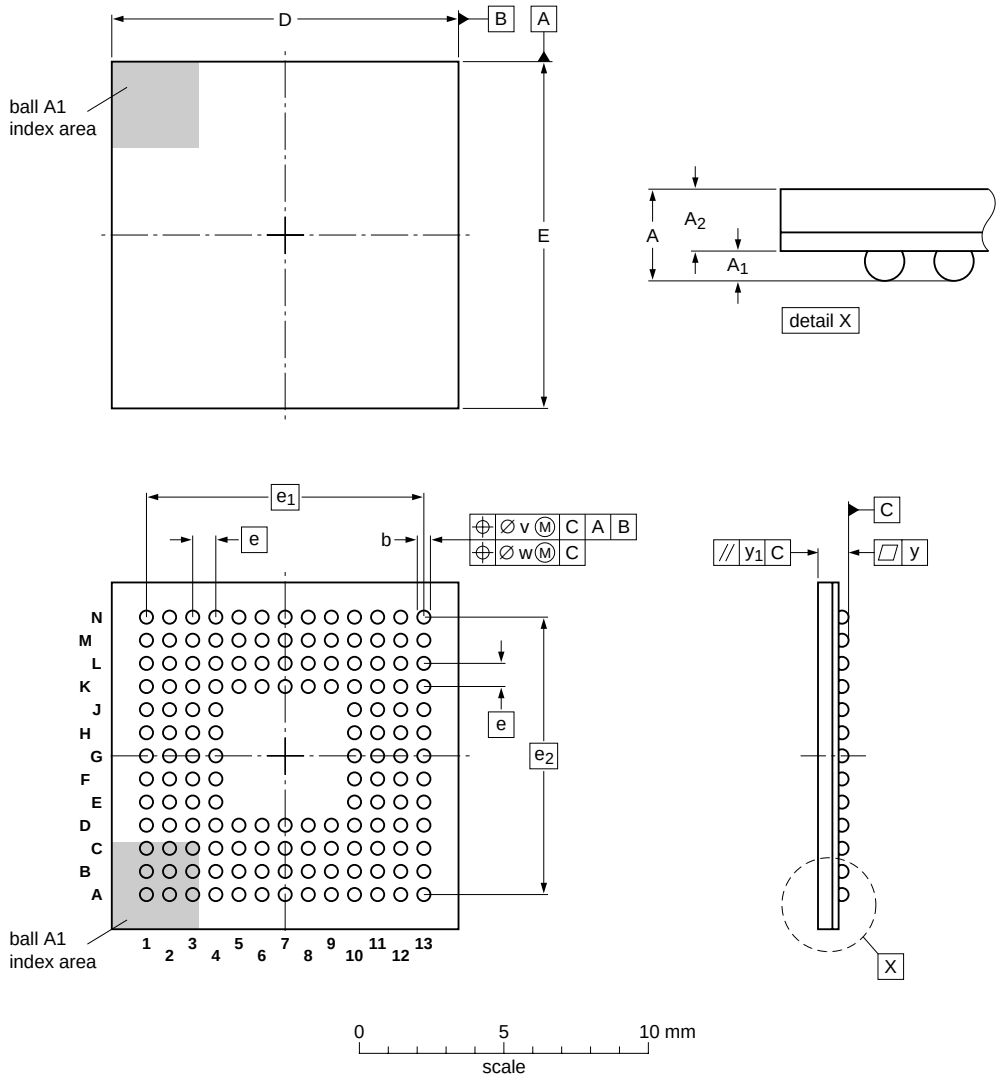
Fig 9. LPC2210 I_{DD} in Active mode measured at different frequencies (CCLK) and temperatures



Test conditions: Power-down mode entered executing code from on-chip RAM; all peripherals are enabled in PCONP register.

Fig 14. LPC2220 and LPC2210/01 I_{DD} in Power-down mode measured at different temperatures

TFBGA144: plastic thin fine-pitch ball grid array package; 144 balls **SOT569-2**



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	1.20	0.40	0.80	0.50	12.1	12.1	0.8	9.6	9.6	0.15	0.05	0.1	0.08
	nom	1.05	0.35	0.70	0.45	12.0	12.0							
	min	0.95	0.30	0.65	0.40	11.9	11.9							

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT569-2						~~08-01-29~~ 08-03-14

Fig 16. Package outline SOT569-2 (TFBGA144)

15. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

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