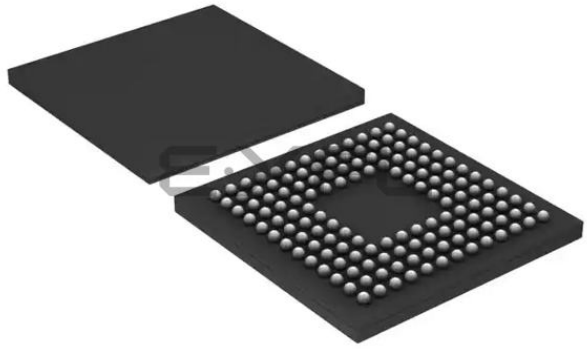

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	75MHz
Connectivity	EBI/EMI, I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	76
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TFBGA
Supplier Device Package	144-TFBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2220fet144-g-51

- LPC2210/01 and LPC2220 only: UART0/1 include fractional baud rate generator, auto-bauding capabilities, and handshake flow-control fully implemented in hardware.

- Vectored Interrupt Controller (VIC) with configurable priorities and vector addresses.
- Configurable external memory interface with up to four banks, each up to 16 MB and 8/16/32-bit data width.
- Up to 76 general purpose pins (5 V tolerant) capable. Up to nine edge/level sensitive external interrupt pins available.
  - LPC2210/01 and LPC2220 only: Fast GPIO ports enable port pin toggling up to 3.5 times faster than the original device. They also allow for a port pin to be read at any time regardless of its function.
- 60 MHz (LPC2210) and 75 MHz (LPC2210/01 and LPC2220) maximum CPU clock available from programmable on-chip Phase-Locked Loop (PLL) with settling time of 100 µs.
- On-chip integrated oscillator operates with external crystal in range of 1 MHz to 25 MHz and with external oscillator up to 25 MHz.
- Power saving modes include Idle and Power-down.
- Processor wake-up from Power-down mode via external interrupt.
- Individual enable/disable of peripheral functions for power optimization.
- Dual power supply:
  - CPU operating voltage range of 1.65 V to 1.95 V (1.8 V ± 0.15 V).
  - I/O power supply range of 3.0 V to 3.6 V (3.3 V ± 10 %) with 5 V tolerant I/O pads. 16/32-bit ARM7TDMI-S processor.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2210FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2210FBD144/01	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2220FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2220FET144	TFBGA144	plastic thin fine-pitch ball grid array package; 144 balls; body 12 × 12 × 0.8 mm	SOT569-2
LPC2220FET144/G	TFBGA144	plastic thin fine-pitch ball grid array package; 144 balls; body 12 × 12 × 0.8 mm	SOT569-2

3.1 Ordering options

Table 2. Ordering options

Type number	RAM	Fast GPIO/ SSP/ Enhanced UART, ADC, Timer	Temperature range
LPC2210FBD144	16 kB	no	–40 °C to +85 °C
LPC2210FBD144/01	16 kB	yes	–40 °C to +85 °C
LPC2220FBD144	64 kB	yes	–40 °C to +85 °C
LPC2220FET144	64 kB	yes	–40 °C to +85 °C
LPC2220FET144/G	64 kB	yes	–40 °C to +85 °C

5. Pinning information

5.1 Pinning

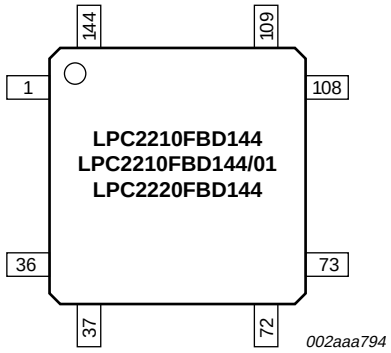

Fig 2. Pin configuration for LQFP144

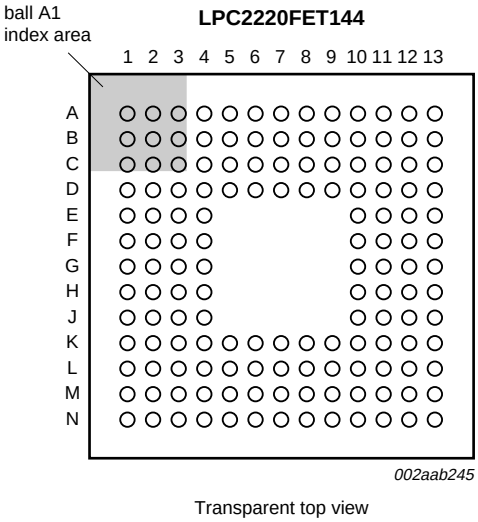

Fig 3. Ball configuration diagram for TFBGA144

5.2 Pin description

Table 4. Pin description

Symbol	Pin (LQFP)	Pin (TFBGA)	Type	Description
P0.0 to P0.31			I/O	**Port 0:** Port 0 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the Pin Connect Block. Pins 26 and 31 of port 0 are not available.
P0.0/TXD0/ PWM1	42[1]	L4[1]	O	**TXD0 —** Transmitter output for UART0.
			O	**PWM1 —** Pulse Width Modulator output 1.
P0.1/RXD0/ PWM3/EINT0	49[2]	K6[2]	I	**RXD0 —** Receiver input for UART0.
			O	**PWM3 —** Pulse Width Modulator output 3.
			I	**EINT0 —** External interrupt 0 input
P0.2/SCL/ CAP0.0	50[3]	L6[3]	I/O	**SCL —** I^2C-bus clock input/output. Open-drain output (for I^2C-bus compliance).
			I	**CAP0.0 —** Capture input for Timer 0, channel 0.
P0.3/SDA/ MAT0.0/EINT1	58[3]	M8[3]	I/O	**SDA —** I^2C-bus data input/output. Open-drain output (for I^2C-bus compliance).
			O	**MAT0.0 —** Match output for Timer 0, channel 0.
			I	**EINT1 —** External interrupt 1 input.
P0.4/SCK0/ CAP0.1	59[1]	L8[1]	I/O	**SCK0 —** Serial clock for SPI0. SPI clock output from master or input to slave.
			I	**CAP0.1 —** Capture input for Timer 0, channel 1.
P0.5/MISO0/ MAT0.1	61[1]	N9[1]	I/O	**MISO0 —** Master In Slave OUT for SPI0. Data input to SPI master or data output from SPI slave.
			O	**MAT0.1 —** Match output for Timer 0, channel 1.
P0.6/MOSI0/ CAP0.2	68[1]	N11[1]	I/O	**MOSI0 —** Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
			I	**CAP0.2 —** Capture input for Timer 0, channel 2.
P0.7/SSEL0/ PWM2/EINT2	69[2]	M11[2]	I	**SSEL0 —** Slave Select for SPI0. Selects the SPI interface as a slave.
			O	**PWM2 —** Pulse Width Modulator output 2.
			I	**EINT2 —** External interrupt 2 input.
P0.8/TXD1/ PWM4	75[1]	L12[1]	O	**TXD1 —** Transmitter output for UART1.
			O	**PWM4 —** Pulse Width Modulator output 4.
P0.9/RXD1/ PWM6/EINT3	76[2]	L13[2]	I	**RXD1 —** Receiver input for UART1.
			O	**PWM6 —** Pulse Width Modulator output 6.
			I	**EINT3 —** External interrupt 3 input.
P0.10/RTS1/ CAP1.0	78[1]	K11[1]	O	**RTS1 —** Request to Send output for UART1.
			I	**CAP1.0 —** Capture input for Timer 1, channel 0.
P0.11/CTS1/ CAP1.1	83[1]	J12[1]	I	**CTS1 —** Clear to Send input for UART1.
			I	**CAP1.1 —** Capture input for Timer 1, channel 1.
P0.12/DSR1/ MAT1.0	84[1]	J13[1]	I	**DSR1 —** Data Set Ready input for UART1.
			O	**MAT1.0 —** Match output for Timer 1, channel 0.

Table 4. Pin description *...continued*

Symbol	Pin (LQFP)	Pin (TFBGA)	Type	Description
P0.13/DTR1/ MAT1.1	85[1]	H10[1]	O	**DTR1 —** Data Terminal Ready output for UART1.
			O	**MAT1.1 —** Match output for Timer 1, channel 1.
P0.14/DCD1/ EINT1	92[2]	G10[2]	I	**DCD1 —** Data Carrier Detect input for UART1.
			I	**EINT1 —** External interrupt 1 input. Note: LOW on this pin while $\overline{\text{RESET}}$ is LOW forces on-chip bootloader to take over control of the part after reset.
P0.15/RI1/ EINT2	99[2]	E11[2]	I	**RI1 —** Ring Indicator input for UART1.
			I	**EINT2 —** External interrupt 2 input.
P0.16/EINT0/ MAT0.2/CAP0.2	100[2]	E10[2]	I	**EINT0 —** External interrupt 0 input.
			O	**MAT0.2 —** Match output for Timer 0, channel 2.
			I	**CAP0.2 —** Capture input for Timer 0, channel 2.
P0.17/CAP1.2/ SCK1/MAT1.2	101[1]	D13[1]	I	**CAP1.2 —** Capture input for Timer 1, channel 2.
			I/O	**SCK1 —** Serial Clock for SPI1/SSI/Microwire. SPI/SSI/Microwire clock output from master or input to slave.
			O	**MAT1.2 —** Match output for Timer 1, channel 2.
P0.18/CAP1.3/ MISO1/MAT1.3	121[1]	D8[1]	I	**CAP1.3 —** Capture input for Timer 1, channel 3.
			I/O	**MISO1 —** Master In Slave Out for SPI1. Data input to SPI master or data output from SPI slave.
			O	**MAT1.3 —** Match output for Timer 1, channel 3.
P0.19/MAT1.2/ MOSI1/CAP1.2	122[1]	C8[1]	O	**MAT1.2 —** Match output for Timer 1, channel 2.
			I/O	**MOSI1 —** Master Out Slave In for SPI1. Data output from SPI master or data input to SPI slave. • SPI interface: MOSI line. • SSI: DX/RX line (SPI1 as a master/slave). • Microwire: SO/SI line (SPI1 as a master/slave).
			I	**CAP1.2 —** Capture input for Timer 1, channel 2.
P0.20/MAT1.3/ SSEL1/ EINT3	123[2]	B8[2]	O	**MAT1.3 —** Match output for Timer 1, channel 3.
			I	**SSEL1 —** Slave Select for SPI1/Microwire. Used to select the SPI or Microwire interface as a slave. Frame synchronization in case of 4-wire SSI.
			I	**EINT3 —** External interrupt 3 input.
P0.21/PWM5/ CAP1.3	4[1]	C1[1]	O	**PWM5 —** Pulse Width Modulator output 5.
			I	**CAP1.3 —** Capture input for Timer 1, channel 3.
P0.22/CAP0.0/ MAT0.0	5[1]	D4[1]	I	**CAP0.0 —** Capture input for Timer 0, channel 0.
			O	**MAT0.0 —** Match output for Timer 0, channel 0.
P0.23	6[1]	D3[1]	I/O	General purpose bidirectional digital port only.
P0.24	8[1]	D1[1]	I/O	General purpose bidirectional digital port only.
P0.25	21[1]	H1[1]	I/O	General purpose bidirectional digital port only.
P0.27/AIN0/ CAP0.1/MAT0.1	23[4]	H3[4]	I	**AIN0 —** ADC, input 0. This analog input is always connected to its pin.
			I	**CAP0.1 —** Capture input for Timer 0, channel 1.
			O	**MAT0.1 —** Match output for Timer 0, channel 1.

Table 4. Pin description *...continued*

Symbol	Pin (LQFP)	Pin (TFBGA)	Type	Description
P0.28/AIN1/ CAP0.2/MAT0.2	25[4]	J1[4]	I	**AIN1 —** ADC, input 1. This analog input is always connected to its pin.
			I	**CAP0.2 —** Capture input for Timer 0, channel 2.
			O	**MAT0.2 —** Match output for Timer 0, channel 2.
P0.29/AIN2/ CAP0.3/MAT0.3	32[4]	L1[4]	I	**AIN2 —** ADC, input 2. This analog input is always connected to its pin.
			I	**CAP0.3 —** Capture input for Timer 0, Channel 3.
			O	**MAT0.3 —** Match output for Timer 0, channel 3.
P0.30/AIN3/ EINT3/CAP0.0	33[4]	L2[4]	I	**AIN3 —** ADC, input 3. This analog input is always connected to its pin.
			I	**EINT3 —** External interrupt 3 input.
			I	**CAP0.0 —** Capture input for Timer 0, channel 0.
P1.0 to P1.31			I/O	**Port 1:** Port 1 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the Pin Connect Block. Pins 0 through 15 of port 1 are not available.
P1.0/$\overline{CS0}$	91[5]	G11[5]	O	**$\overline{CS0}$ —** LOW-active Chip Select 0 signal. (Bank 0 addresses range 0x8000 0000 to 0x80FF FFFF)
P1.1/$\overline{OE}$	90[5]	G13[5]	O	**$\overline{OE}$ —** LOW-active Output Enable signal.
P1.16/ TRACEPKT0	34[5]	L3[5]	O	**TRACEPKT0 —** Trace Packet, bit 0. Standard I/O port with internal pull-up.
P1.17/ TRACEPKT1	24[5]	H4[5]	O	**TRACEPKT1 —** Trace Packet, bit 1. Standard I/O port with internal pull-up.
P1.18/ TRACEPKT2	15[5]	F2[5]	O	**TRACEPKT2 —** Trace Packet, bit 2. Standard I/O port with internal pull-up.
P1.19/ TRACEPKT3	7[5]	D2[5]	O	**TRACEPKT3 —** Trace Packet, bit 3. Standard I/O port with internal pull-up.
P1.20/ TRACESYNC	102[5]	D12[5]	O	**TRACESYNC —** Trace Synchronization. Standard I/O port with internal pull-up. Note: LOW on this pin while $\overline{RESET}$ is LOW, enables pins P1[25:16] to operate as Trace port after reset.
P1.21/ PIPESTAT0	95[5]	F11[5]	O	**PIPESTAT0 —** Pipeline Status, bit 0. Standard I/O port with internal pull-up.
P1.22/ PIPESTAT1	86[5]	H11[5]	O	**PIPESTAT1 —** Pipeline Status, bit 1. Standard I/O port with internal pull-up.
P1.23/ PIPESTAT2	82[5]	J11[5]	O	**PIPESTAT2 —** Pipeline Status, bit 2. Standard I/O port with internal pull-up.
P1.24/ TRACECLK	70[5]	L11[5]	O	**TRACECLK —** Trace Clock. Standard I/O port with internal pull-up.
P1.25/EXTIN0	60[5]	K8[5]	I	**EXTIN0 —** External Trigger Input. Standard I/O with internal pull-up.

Table 4. Pin description *...continued*

Symbol	Pin (LQFP)	Pin (TFBGA)	Type	Description
P3.19/A19	46[5]	L5[5]	O	**A19 —** External memory address line 19.
P3.20/A20	45[5]	K5[5]	O	**A20 —** External memory address line 20.
P3.21/A21	44[5]	N4[5]	O	**A21 —** External memory address line 21.
P3.22/A22	41[5]	K4[5]	O	**A22 —** External memory address line 22.
P3.23/A23/XCLK	40[5]	N3[5]	O	**A23 —** External memory address line 23.
			O	**XCLK —** Clock output.
P3.24/$\overline{CS3}$	36[5]	M2[5]	O	**$\overline{CS3}$ —** LOW-active Chip Select 3 signal. (Bank 3 addresses range 0x8300 0000 to 0x83FF FFFF)
P3.25/$\overline{CS2}$	35[5]	M1[5]	O	**$\overline{CS2}$ —** LOW-active Chip Select 2 signal. (Bank 2 addresses range 0x8200 0000 to 0x82FF FFFF)
P3.26/$\overline{CS1}$	30[5]	K2[5]	O	**$\overline{CS1}$ —** LOW-active Chip Select 1 signal. (Bank 1 addresses range 0x8100 0000 to 0x81FF FFFF)
P3.27/$\overline{WE}$	29[5]	K1[5]	O	**$\overline{WE}$ —** LOW-active Write enable signal.
P3.28/$\overline{BLS3}$/AIN7	28[2]	J4[2]	O	**$\overline{BLS3}$ —** LOW-active Byte Lane Select signal (Bank 3).
			I	**AIN7 —** ADC, input 7. This analog input is always connected to its pin.
P3.29/$\overline{BLS2}$/AIN6	27[4]	J3[4]	O	**$\overline{BLS2}$ —** LOW-active Byte Lane Select signal (Bank 2).
			I	**AIN6 —** ADC, input 6. This analog input is always connected to its pin.
P3.30/$\overline{BLS1}$	97[4]	E13[4]	O	**$\overline{BLS1}$ —** LOW-active Byte Lane Select signal (Bank 1).
P3.31/$\overline{BLS0}$	96[4]	F10[4]	O	**$\overline{BLS0}$ —** LOW-active Byte Lane Select signal (Bank 0).
n.c.	22[5]	H2[5]		Not connected. This pin MUST NOT be pulled LOW or the device might not operate properly.
$\overline{RESET}$	135[6]	C5[6]	I	**External reset input:** A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	142[7]	C3[7]	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	141[7]	B3[7]	O	Output from the oscillator amplifier.
V_{SS}	3, 9, 26, 38, 54, 67, 79, 93, 103, 107, 111, 128	C2, E4, J2, N2, N7, L10, K12, F13, D11, B13, B11, D7	I	**Ground:** 0 V reference.
V_{SSA}	139	C4	I	**Analog ground:** 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
$V_{SSA(PLL)}$	138	B4	I	**PLL analog ground:** 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
$V_{DD(1V8)}$	37, 110	N1, A12	I	**1.8 V core power supply:** This is the power supply voltage for internal circuitry.

Table 4. Pin description *...continued*

Symbol	Pin (LQFP)	Pin (TFBGA)	Type	Description
$V_{DDA(1V8)}$	143	A2	I	**Analog 1.8 V core power supply:** This is the power supply voltage for internal circuitry. This should be nominally the same voltage as $V_{DD(1V8)}$ but should be isolated to minimize noise and error.
$V_{DD(3V3)}$	2, 31, 39, 51, 57, 77, 94, 104, 112, 119	B1, K3, M3, M6, N8, K10, F12, C13, A11, B9	I	**3.3 V pad power supply:** This is the power supply voltage for the I/O ports.
$V_{DDA(3V3)}$	14	F3	I	**Analog 3.3 V pad power supply:** This should be nominally the same voltage as $V_{DD(3V3)}$ but should be isolated to minimize noise and error.

[1] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control.

[2] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. If configured for an input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns.

[3] Open drain 5 V tolerant digital I/O I^2C-bus 400 kHz specification compatible pad. It requires external pull-up to provide an output functionality.

[4] 5 V tolerant pad providing digital I/O (with TTL levels and hysteresis and 10 ns slew rate control) and analog input function. If configured for a digital input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns. When configured as an ADC input, digital section of the pad is disabled.

[5] 5 V tolerant pad with built-in pull-up resistor providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. The pull-up resistor's value ranges from 60 kΩ to 300 kΩ.

[6] 5 V tolerant pad providing digital input (with TTL levels and hysteresis) function only.

[7] Pad provides special analog functionality.

Non-vectored IRQs have the lowest priority.

The VIC combines the requests from all the vectored and non-vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping there. If any of the vectored IRQs are requesting, the VIC provides the address of the highest-priority requesting IRQs service routine, otherwise it provides the address of a default routine that is shared by all the non-vectored IRQs. The default routine can read another VIC register to see what IRQs are active.

6.4.1 Interrupt sources

Table 5 lists the interrupt sources for each peripheral function. Each peripheral device has one interrupt line connected to the VIC, but may have several internal interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Table 5. Interrupt sources

Block	Flag(s)	VIC channel #
WDT	Watchdog Interrupt (WDINT)	0
-	Reserved for software interrupts only	1
ARM Core	EmbeddedICE, DbgCommRX	2
ARM Core	EmbeddedICE, DbgCommTX	3
TIMER0	Match 0 to 3 (MR0, MR1, MR2, MR3)	4
TIMER1	Match 0 to 3 (MR0, MR1, MR2, MR3)	5
UART0	RX Line Status (RLS) Transmit Holding Register Empty (THRE) RX Data Available (RDA) Character Time-out Indicator (CTI)	6
UART1	RX Line Status (RLS) Transmit Holding Register empty (THRE) RX Data Available (RDA) Character Time-out Indicator (CTI) Modem Status Interrupt (MSI)	7
PWM0	Match 0 to 6 (MR0, MR1, MR2, MR3, MR4, MR5, MR6)	8
I^2C	SI (state change)	9
SPI0	SPIF, MODF	10
SPI1 and SSP	SPIF, MODF and TXRIS, RXRIS, RTRIS, RORRIS	11
PLL	PLL Lock (PLOCK)	12
RTC	RTCCIF (Counter Increment), RTCALF (Alarm)	13
System Control	External Interrupt 0 (EINT0)	14
	External Interrupt 1 (EINT1)	15
	External Interrupt 2 (EINT2)	16
	External Interrupt 3 (EINT3)	17
A/D	ADC	18

Table 7. Pin function select register 0 (PINSEL0 - 0xE002 C000) *...continued*

PINSEL0	Pin name	Value		Function	Value after reset
11:10	P0.5	0	0	GPIO Port 0.5	0
		0	1	MISO (SPI0)	
		1	0	Match 0.1 (Timer 0)	
		1	1	reserved	
13:12	P0.6	0	0	GPIO Port 0.6	0
		0	1	MOSI (SPI0)	
		1	0	Capture 0.2 (Timer 0)	
		1	1	reserved	
15:14	P0.7	0	0	GPIO Port 0.7	0
		0	1	SSEL (SPI0)	
		1	0	PWM2	
		1	1	EINT2	
17:16	P0.8	0	0	GPIO Port 0.8	0
		0	1	TXD1 UART1	
		1	0	PWM4	
		1	1	reserved	
19:18	P0.9	0	0	GPIO Port 0.9	0
		0	1	RXD1 (UART1)	
		1	0	PWM6	
		1	1	EINT3	
21:20	P0.10	0	0	GPIO Port 0.10	0
		0	1	RTS1 (UART1)	
		1	0	Capture 1.0 (Timer 1)	
		1	1	reserved	
23:22	P0.11	0	0	GPIO Port 0.11	0
		0	1	CTS1 (UART1)	
		1	0	Capture 1.1 (Timer 1)	
		1	1	reserved	
25:24	P0.12	0	0	GPIO Port 0.12	0
		0	1	DSR1 (UART1)	
		1	0	Match 1.0 (Timer 1)	
		1	1	reserved	
27:26	P0.13	0	0	GPIO Port 0.13	0
		0	1	DTR1 (UART1)	
		1	0	Match 1.1 (Timer 1)	
		1	1	reserved	
29:28	P0.14	0	0	GPIO Port 0.14	0
		0	1	DCD1 (UART1)	
		1	0	EINT1	
		1	1	reserved	

Table 7. Pin function select register 0 (PINSEL0 - 0xE002 C000) *...continued*

PINSEL0	Pin name	Value		Function	Value after reset
31:30	P0.15	0	0	GPIO Port 0.15	0
		0	1	RI1 (UART1)	
		1	0	EINT2	
		1	1	reserved	

6.7 Pin function select register 1 (PINSEL1 - 0xE002 C004)

The PINSEL1 register controls the functions of the pins as per the settings listed in Table 8. The direction control bit in the IODIR register is effective only when the GPIO function is selected for a pin. For other functions direction is controlled automatically. Settings other than those shown in the Table 8 are reserved, and should not be used.

Table 8. Pin function select register 1 (PINSEL1 - 0xE002 C004)

PINSEL1	Pin name	Value		Function	Value after reset
1:0	P0.16	0	0	GPIO Port 0.16	0
		0	1	EINT0	
		1	0	Match 0.2 (Timer 0)	
		1	1	Capture 0.2 (Timer 0)	
3:2	P0.17	0	0	GPIO Port 0.17	0
		0	1	Capture 1.2 (Timer 1)	
		1	0	SCK (SPI1)	
		1	1	Match 1.2 (Timer 1)	
5:4	P0.18	0	0	GPIO Port 0.18	0
		0	1	Capture 1.3 (Timer 1)	
		1	0	MISO (SPI1)	
		1	1	Match 1.3 (Timer 1)	
7:6	P0.19	0	0	GPIO Port 0.19	0
		0	1	Match 1.2 (Timer 1)	
		1	0	MOSI (SPI1)	
		1	1	Capture 1.2 (Timer 1)	
9:8	P0.20	0	0	GPIO Port 0.20	0
		0	1	Match 1.3 (Timer 1)	
		1	0	SSEL (SPI1)	
		1	1	EINT3	
11:10	P0.21	0	0	GPIO Port 0.21	0
		0	1	PWM5	
		1	0	reserved	
		1	1	Capture 1.3 (Timer 1)	
13:12	P0.22	0	0	GPIO Port 0.22	0
		0	1	reserved	
		1	0	Capture 0.0 (Timer 0)	
		1	1	Match 0.0 (Timer 0)	

- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus may be used for test and diagnostic purposes.

6.14 SPI serial I/O controller

The LPC2210/2220 each contain two SPIs. The SPI is a full duplex serial interface, designed to be able to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

6.14.1 Features

- Compliant with SPI specification.
- Synchronous, serial, full duplex, communication.
- Combined SPI master and slave.
- Maximum data bit rate of one eighth of the input clock rate.

6.15 SSP controller

This peripheral is available in LPC2210/01 and LPC2220 only.

6.15.1 Features

- Compatible with Motorola’s SPI, Texas Instrument’s 4-wire SSI, and National Semiconductor’s Microwire buses.
- Synchronous serial communication.
- Master or slave operation.
- 8-frame FIFOs for both transmit and receive.
- 4 bits to 16 bits per frame.

6.15.2 Description

The SSP is a controller capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. Data transfers are in principle full duplex, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master.

6.17 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to 'feed' (or reload) the watchdog within a predetermined amount of time.

6.17.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(PCLK)} \times 256 \times 4$) to ($T_{cy(PCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(PCLK)} \times 4$.

6.18 Real-time clock

The Real-Time Clock (RTC) is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

6.18.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra-low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Programmable reference clock divider allows adjustment of the RTC to match various crystal frequencies.

6.19 Pulse width modulator

The PWM is based on the standard timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2210/2220. The timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is also based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge

controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

6.19.1 Features

- Seven match registers allow up to six single edge controlled or three double edge controlled PWM outputs, or a mix of both types.
- The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go HIGH at the beginning of each cycle unless the output is a constant LOW. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit timer/counter with a programmable 32-bit prescaler.

6.20 System control

6.20.1 Crystal oscillator

The oscillator supports crystals in the range of 1 MHz to 25 MHz and up to 25 MHz with the external oscillator. The oscillator output frequency is called f_{osc} and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. f_{osc} and CCLK are the same value unless the PLL is running and connected. Refer to Section 6.20.2 “PLL” for additional information.

6.20.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 60 MHz (LPC2210) and 10 MHz to 75 MHz (LPC2210/01 and LPC2220) with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 µs.

6.20.3 Reset and wake-up timer

Reset has two sources on the LPC2210/2220: the $\overline{\text{RESET}}$ pin and watchdog reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip reset by any source starts the wake-up timer (see wake-up timer description below), causing the internal chip reset to remain asserted until the external reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip circuitry has completed its initialization.

When the internal reset is removed, the processor begins executing at address 0, which is the reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The wake-up timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power-on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the wake-up timer.

The wake-up timer monitors the crystal oscillator as the means of checking whether it is safe to begin code execution. When power is applied to the chip, or some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of V_{DD} ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g. capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

6.20.4 External interrupt inputs

The LPC2210/2220 include up to nine edge or level sensitive external interrupt inputs as selectable pin functions. When the pins are combined, external events can be processed as four independent interrupt signals. The external interrupt inputs can optionally be used to wake up the processor from Power-down mode.

6.21.1 EmbeddedICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol converter. EmbeddedICE protocol converter converts the remote debug protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a Debug Communication Channel (DCC) function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The debug communication channel is accessed as a co-processor 14 by the program running on the ARM7TDMI-S core. The debug communication channel allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The debug communication channel data and control registers are mapped in to addresses in the EmbeddedICE logic.

The JTAG clock (TCK) must be slower than $1/6$ of the CPU clock (CCLK) for the JTAG interface to operate.

6.21.2 Embedded trace

Since the LPC2210/2220 have significant amounts of on-chip memory, it is not possible to determine how the processor core is operating simply by observing the external pins. The Embedded Trace Macrocell (ETM) provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to the trace port.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external trace port analyzer must capture the trace information under software debugger control. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code cannot be traced because of this restriction.

6.21.3 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real-time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the debug communication channel, which is present in the EmbeddedICE logic. The LPC2210/2220 contain a specific configuration of RealMonitor software programmed into the on-chip flash memory.

9. Dynamic characteristics

Table 13. Dynamic characteristics

T_{amb} = 0 °C to +70 °C for commercial applications, −40 °C to +85 °C for industrial applications, $V_{DD(1V8)}$, $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External clock						
f_{osc}	oscillator frequency	supplied by an external oscillator (signal generator)	1	-	25	MHz
		external clock frequency supplied by an external crystal oscillator	1	-	25	MHz
		external clock frequency if on-chip PLL is used	10	-	25	MHz
		external clock frequency if on-chip bootloader is used for initial code download	10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		20	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (except P0.2 and P0.3)						
t_r	rise time		-	10	-	ns
t_f	fall time		-	10	-	ns
I^2C-bus pins (P0.2 and P0.3)						
t_f	fall time	V_{IH} to V_{IL} [2]	$20 + 0.1 \times C_b$	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Bus capacitance C_b in pF, from 10 pF to 400 pF.

Table 14. External memory interface dynamic characteristics

C_L = 25 pF; T_{amb} = 40 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Common to read and write cycles						
t_{CHAV}	XCLK HIGH to address valid time		-	-	10	ns
t_{CHCSL}	XCLK HIGH to $\overline{CS}$ LOW time		-	-	10	ns
t_{CHCSH}	XCLK HIGH to $\overline{CS}$ HIGH time		-	-	10	ns
t_{CHANV}	XCLK HIGH to address invalid time		-	-	10	ns
Read cycle parameters						
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	[1]	–5	-	+10	ns
t_{OELAV}	$\overline{OE}$ LOW to address valid time	[1]	–5	-	+10	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time		–5	-	+5	ns
t_{am}	memory access time	[2][3] [4]	$(T_{cy(CCLK)} \times (2 + WST1)) + (-20)$	-	-	ns
$t_{am(ibr)}$	memory access time (initial burst-ROM)	[2][3] [4]	$(T_{cy(CCLK)} \times (2 + WST1)) + (-20)$	-	-	ns
$t_{am(sbr)}$	memory access time (subsequent burst-ROM)	[2][5]	$T_{cy(CCLK)} + (-20)$	-	-	ns
$t_{h(D)}$	data hold time	[6]	0	-	-	ns
t_{CSHOEH}	$\overline{CS}$ HIGH to $\overline{OE}$ HIGH time		–5	-	+5	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid time		–5	-	+5	ns
t_{CHOEL}	XCLK HIGH to $\overline{OE}$ LOW time		–5	-	+5	ns
t_{CHOEH}	XCLK HIGH to $\overline{OE}$ HIGH time		–5	-	+5	ns
Write cycle parameters						
t_{AVCSL}	address valid to $\overline{CS}$ LOW time	[1]	$T_{cy(CCLK)} - 10$	-	-	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time		–5	-	+5	ns
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time		–5	-	+5	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time		–5	-	+5	ns
t_{WELDV}	$\overline{WE}$ LOW to data valid time		–5	-	+5	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time		–5	-	+5	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	[2][4]	$T_{cy(CCLK)} \times (1 + WST2) - 5$	-	$T_{cy(CCLK)} \times (1 + WST2) + 5$	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	[2][4]	$T_{cy(CCLK)} \times (1 + WST2) - 5$	-	$T_{cy(CCLK)} \times (1 + WST2) + 5$	ns
t_{WEHANV}	$\overline{WE}$ HIGH to address invalid time	[2]	$T_{cy(CCLK)} - 5$	-	$T_{cy(CCLK)} + 5$	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time	[2]	$(2 \times T_{cy(CCLK)}) - 5$	-	$(2 \times T_{cy(CCLK)}) + 5$	ns
$t_{BLSHANV}$	$\overline{BLS}$ HIGH to address invalid time	[2]	$T_{cy(CCLK)} - 5$	-	$T_{cy(CCLK)} + 5$	ns

11. Abbreviations

Table 16. Acronym list

Acronym	Description
ADC	Analog-to-Digital Converter
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
CISC	Complex Instruction Set Computer
FIFO	First In, First Out
GPIO	General Purpose Input/Output
I/O	Input/Output
JTAG	Joint Test Action Group
PWM	Pulse Width Modulator
RISC	Reduced Instruction Set Computer
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter

15. Contents

For more information, please visit: http://www.nxp.com
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