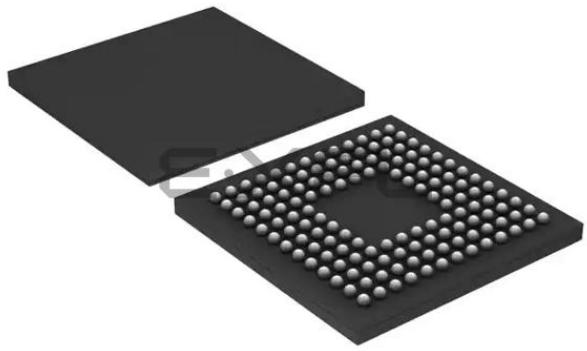

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	75MHz
Connectivity	EBI/EMI, I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	76
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TFBGA
Supplier Device Package	144-TFBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2220fet144-g-55

- LPC2210/01 and LPC2220 only: UART0/1 include fractional baud rate generator, auto-bauding capabilities, and handshake flow-control fully implemented in hardware.

- Vectored Interrupt Controller (VIC) with configurable priorities and vector addresses.
- Configurable external memory interface with up to four banks, each up to 16 MB and 8/16/32-bit data width.
- Up to 76 general purpose pins (5 V tolerant) capable. Up to nine edge/level sensitive external interrupt pins available.
  - LPC2210/01 and LPC2220 only: Fast GPIO ports enable port pin toggling up to 3.5 times faster than the original device. They also allow for a port pin to be read at any time regardless of its function.
- 60 MHz (LPC2210) and 75 MHz (LPC2210/01 and LPC2220) maximum CPU clock available from programmable on-chip Phase-Locked Loop (PLL) with settling time of 100 µs.
- On-chip integrated oscillator operates with external crystal in range of 1 MHz to 25 MHz and with external oscillator up to 25 MHz.
- Power saving modes include Idle and Power-down.
- Processor wake-up from Power-down mode via external interrupt.
- Individual enable/disable of peripheral functions for power optimization.
- Dual power supply:
  - CPU operating voltage range of 1.65 V to 1.95 V (1.8 V ± 0.15 V).
  - I/O power supply range of 3.0 V to 3.6 V (3.3 V ± 10 %) with 5 V tolerant I/O pads. 16/32-bit ARM7TDMI-S processor.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2210FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2210FBD144/01	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2220FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2220FET144	TFBGA144	plastic thin fine-pitch ball grid array package; 144 balls; body 12 × 12 × 0.8 mm	SOT569-2
LPC2220FET144/G	TFBGA144	plastic thin fine-pitch ball grid array package; 144 balls; body 12 × 12 × 0.8 mm	SOT569-2

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5. Pinning information

5.1 Pinning

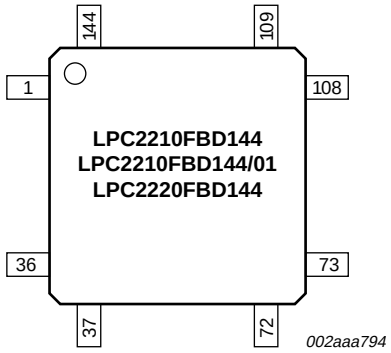

Fig 2. Pin configuration for LQFP144

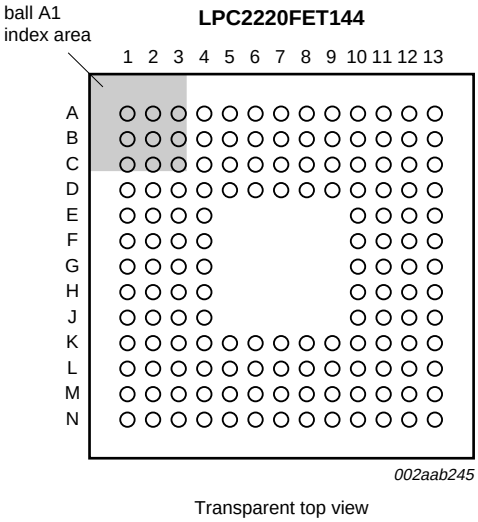

Fig 3. Ball configuration diagram for TFBGA144

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Table 3. Ball allocation

Row	Column												
	1	2	3	4	5	6	7	8	9	10	11	12	13
A	P2.22/ D22	$V_{DDA(1V8)}$	P1.28/ TDI	P2.21/ D21	P2.18/ D18	P2.14/ D14	P1.29/ TCK	P2.11/ D11	P2.10/ D10	P2.7/D7	$V_{DD(3V3)}$	$V_{DD(1V8)}$	P2.4/D4
B	$V_{DD(3V3)}$	P1.27/ TDO	XTAL2	$V_{SSA(PLL)}$	P2.19/ D19	P2.15/ D15	P2.12/ D12	P0.20/ MAT1.3/ SSEL1/ EINT3	$V_{DD(3V3)}$	P2.6/D6	V_{SS}	P2.3/D3	V_{SS}
C	P0.21/ PWM5/ CAP1.3	V_{SS}	XTAL1	V_{SSA}	$\overline{\text{RESET}}$	P2.16/ D16	P2.13/ D13	P0.19/ MAT1.2/ MOSI1/ CAP1.2	P2.9/D9	P2.5/D5	P2.2/D2	P2.1/D1	$V_{DD(3V3)}$
D	P0.24	P1.19/ TRACEPKT3	P0.23	P0.22/ CAP0.0/ MAT0.0	P2.20/ D20	P2.17/ D17	V_{SS}	P0.18/ CAP1.3/ MISO1/ MAT1.3	P2.8/D8	P1.30/ TMS	V_{SS}	P1.20/ TRACESYNC	P0.17/ CAP1.2/ SCK1/ MAT1.2
E	P2.25/ D25	P2.24/ D24	P2.23/ D23	V_{SS}						P0.16/ EINT0/ MAT0.2/ CAP0.2	P0.15/ RI1/ EINT2	P2.0/D0	P3.30/ $\overline{\text{BLS1}}$
F	P2.27/ D27/ BOOT1	P1.18/ TRACEPKT2	$V_{DDA(3V3)}$	P2.26/ D26/ BOOT0						P3.31/ $\overline{\text{BLS0}}$	P1.21/ PIPESTAT0	$V_{DD(3V3)}$	V_{SS}
G	P2.29/ D29	P2.28/ D28	P2.30/ D30/AIN4	P2.31/ D31/AIN5						P0.14/ DCD1/ EINT1	P1.0/$\overline{\text{CS0}}$	P3.0/A0	P1.1/$\overline{\text{OE}}$
H	P0.25	n.c.	P0.27/ AIN0/ CAP0.1/ MAT0.1	P1.17/ TRACEPKT1						P0.13/ DTR1/ MAT1.1	P1.22/ PIPESTAT1	P3.2/A2	P3.1/A1
J	P0.28/ AIN1/ CAP0.2/ MAT0.2	V_{SS}	P3.29/ $\overline{\text{BLS2}}$/ AIN6	P3.28/ $\overline{\text{BLS3}}$/ AIN7						P3.3/A3	P1.23/ PIPESTAT2	P0.11/ CTS1/ CAP1.1	P0.12/ DSR1/ MAT1.0
K	P3.27/$\overline{\text{WE}}$	P3.26/ $\overline{\text{CS1}}$	$V_{DD(3V3)}$	P3.22/ A22	P3.20/ A20	P0.1/ RXD0/ PWM3/ EINT0	P3.14/ A14	P1.25/ EXTIN0	P3.11/ A11	$V_{DD(3V3)}$	P0.10/ RTS1/ CAP1.0	V_{SS}	P3.4/A4

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Table 3. Ball allocation *…continued*

Row	Column												
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**
L	P0.29/ AIN2/ CAP0.3/ MAT0.3	P0.30/ AIN3/ EINT3/ CAP0.0	P1.16/ TRACEPKT0	P0.0/ TXD0/ PWM1	P3.19/ A19	P0.2/ SCL/ CAP0.0	P3.15/ A15	P0.4/ SCK0/ CAP0.1	P3.12/ A12	V_{SS}	P1.24/ TRACECLK	P0.8/ TXD1/ PWM4	P0.9/ RXD1/ PWM6/ EINT3
M	P3.25/ $\overline{CS2}$	P3.24/ $\overline{CS3}$	$V_{DD(3V3)}$	P1.31/ $\overline{TRST}$	P3.18/ A18	$V_{DD(3V3)}$	P3.16/ A16	P0.3/ SDA/ MAT0.0/ EINT1	P3.13/ A13	P3.9/A9	P0.7/ SSEL0/ PWM2/ EINT2	P3.7/A7	P3.5/A5
N	$V_{DD(1V8)}$	V_{SS}	P3.23/ A23/ XCLK	P3.21/ A21	P3.17/ A17	P1.26/ RTCK	V_{SS}	$V_{DD(3V3)}$	P0.5/ MISO0/ MAT0.1	P3.10/ A10	P0.6/ MOSI0/ CAP0.2	P3.8/A8	P3.6/A6

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5.2 Pin description

Table 4. Pin description

Symbol	Pin (LQFP)	Pin (TFBGA)	Type	Description
P0.0 to P0.31			I/O	**Port 0:** Port 0 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the Pin Connect Block. Pins 26 and 31 of port 0 are not available.
P0.0/TXD0/ PWM1	42[1]	L4[1]	O	**TXD0 —** Transmitter output for UART0.
			O	**PWM1 —** Pulse Width Modulator output 1.
P0.1/RXD0/ PWM3/EINT0	49[2]	K6[2]	I	**RXD0 —** Receiver input for UART0.
			O	**PWM3 —** Pulse Width Modulator output 3.
			I	**EINT0 —** External interrupt 0 input
P0.2/SCL/ CAP0.0	50[3]	L6[3]	I/O	**SCL —** I^2C-bus clock input/output. Open-drain output (for I^2C-bus compliance).
			I	**CAP0.0 —** Capture input for Timer 0, channel 0.
P0.3/SDA/ MAT0.0/EINT1	58[3]	M8[3]	I/O	**SDA —** I^2C-bus data input/output. Open-drain output (for I^2C-bus compliance).
			O	**MAT0.0 —** Match output for Timer 0, channel 0.
			I	**EINT1 —** External interrupt 1 input.
P0.4/SCK0/ CAP0.1	59[1]	L8[1]	I/O	**SCK0 —** Serial clock for SPI0. SPI clock output from master or input to slave.
			I	**CAP0.1 —** Capture input for Timer 0, channel 1.
P0.5/MISO0/ MAT0.1	61[1]	N9[1]	I/O	**MISO0 —** Master In Slave OUT for SPI0. Data input to SPI master or data output from SPI slave.
			O	**MAT0.1 —** Match output for Timer 0, channel 1.
P0.6/MOSI0/ CAP0.2	68[1]	N11[1]	I/O	**MOSI0 —** Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
			I	**CAP0.2 —** Capture input for Timer 0, channel 2.
P0.7/SSEL0/ PWM2/EINT2	69[2]	M11[2]	I	**SSEL0 —** Slave Select for SPI0. Selects the SPI interface as a slave.
			O	**PWM2 —** Pulse Width Modulator output 2.
			I	**EINT2 —** External interrupt 2 input.
P0.8/TXD1/ PWM4	75[1]	L12[1]	O	**TXD1 —** Transmitter output for UART1.
			O	**PWM4 —** Pulse Width Modulator output 4.
P0.9/RXD1/ PWM6/EINT3	76[2]	L13[2]	I	**RXD1 —** Receiver input for UART1.
			O	**PWM6 —** Pulse Width Modulator output 6.
			I	**EINT3 —** External interrupt 3 input.
P0.10/RTS1/ CAP1.0	78[1]	K11[1]	O	**RTS1 —** Request to Send output for UART1.
			I	**CAP1.0 —** Capture input for Timer 1, channel 0.
P0.11/CTS1/ CAP1.1	83[1]	J12[1]	I	**CTS1 —** Clear to Send input for UART1.
			I	**CAP1.1 —** Capture input for Timer 1, channel 1.
P0.12/DSR1/ MAT1.0	84[1]	J13[1]	I	**DSR1 —** Data Set Ready input for UART1.
			O	**MAT1.0 —** Match output for Timer 1, channel 0.

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Table 4. Pin description *...continued*

Symbol	Pin (LQFP)	Pin (TFBGA)	Type	Description
P0.28/AIN1/ CAP0.2/MAT0.2	25[4]	J1[4]	I	**AIN1 —** ADC, input 1. This analog input is always connected to its pin.
			I	**CAP0.2 —** Capture input for Timer 0, channel 2.
			O	**MAT0.2 —** Match output for Timer 0, channel 2.
P0.29/AIN2/ CAP0.3/MAT0.3	32[4]	L1[4]	I	**AIN2 —** ADC, input 2. This analog input is always connected to its pin.
			I	**CAP0.3 —** Capture input for Timer 0, Channel 3.
			O	**MAT0.3 —** Match output for Timer 0, channel 3.
P0.30/AIN3/ EINT3/CAP0.0	33[4]	L2[4]	I	**AIN3 —** ADC, input 3. This analog input is always connected to its pin.
			I	**EINT3 —** External interrupt 3 input.
			I	**CAP0.0 —** Capture input for Timer 0, channel 0.
P1.0 to P1.31			I/O	**Port 1:** Port 1 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the Pin Connect Block. Pins 0 through 15 of port 1 are not available.
P1.0/$\overline{CS0}$	91[5]	G11[5]	O	**$\overline{CS0}$ —** LOW-active Chip Select 0 signal. (Bank 0 addresses range 0x8000 0000 to 0x80FF FFFF)
P1.1/$\overline{OE}$	90[5]	G13[5]	O	**$\overline{OE}$ —** LOW-active Output Enable signal.
P1.16/ TRACEPKT0	34[5]	L3[5]	O	**TRACEPKT0 —** Trace Packet, bit 0. Standard I/O port with internal pull-up.
P1.17/ TRACEPKT1	24[5]	H4[5]	O	**TRACEPKT1 —** Trace Packet, bit 1. Standard I/O port with internal pull-up.
P1.18/ TRACEPKT2	15[5]	F2[5]	O	**TRACEPKT2 —** Trace Packet, bit 2. Standard I/O port with internal pull-up.
P1.19/ TRACEPKT3	7[5]	D2[5]	O	**TRACEPKT3 —** Trace Packet, bit 3. Standard I/O port with internal pull-up.
P1.20/ TRACESYNC	102[5]	D12[5]	O	**TRACESYNC —** Trace Synchronization. Standard I/O port with internal pull-up. Note: LOW on this pin while $\overline{RESET}$ is LOW, enables pins P1[25:16] to operate as Trace port after reset.
P1.21/ PIPESTAT0	95[5]	F11[5]	O	**PIPESTAT0 —** Pipeline Status, bit 0. Standard I/O port with internal pull-up.
P1.22/ PIPESTAT1	86[5]	H11[5]	O	**PIPESTAT1 —** Pipeline Status, bit 1. Standard I/O port with internal pull-up.
P1.23/ PIPESTAT2	82[5]	J11[5]	O	**PIPESTAT2 —** Pipeline Status, bit 2. Standard I/O port with internal pull-up.
P1.24/ TRACECLK	70[5]	L11[5]	O	**TRACECLK —** Trace Clock. Standard I/O port with internal pull-up.
P1.25/EXTIN0	60[5]	K8[5]	I	**EXTIN0 —** External Trigger Input. Standard I/O with internal pull-up.

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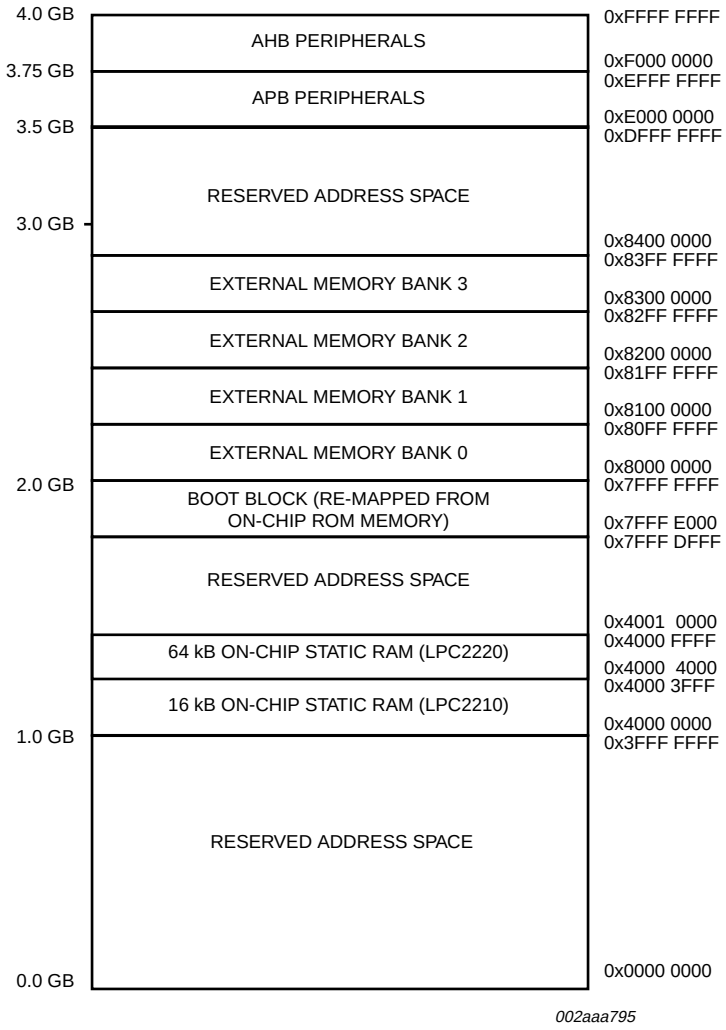

Fig 4. LPC2210/2220 memory map

6.4 Interrupt controller

The VIC accepts all of the interrupt request inputs and categorizes them as Fast Interrupt Request (FIQ), vectored Interrupt Request (IRQ), and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

FIQ has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine can simply start dealing with that device. But if more than one request is assigned to the FIQ class, the FIQ service routine can read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs have the middle priority. Sixteen of the interrupt requests can be assigned to this category. Any of the interrupt requests can be assigned to any of the 16 vectored IRQ slots, among which slot 0 has the highest priority and slot 15 has the lowest.

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Non-vectored IRQs have the lowest priority.

The VIC combines the requests from all the vectored and non-vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping there. If any of the vectored IRQs are requesting, the VIC provides the address of the highest-priority requesting IRQs service routine, otherwise it provides the address of a default routine that is shared by all the non-vectored IRQs. The default routine can read another VIC register to see what IRQs are active.

6.4.1 Interrupt sources

Table 5 lists the interrupt sources for each peripheral function. Each peripheral device has one interrupt line connected to the VIC, but may have several internal interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Table 5. Interrupt sources

Block	Flag(s)	VIC channel #
WDT	Watchdog Interrupt (WDINT)	0
-	Reserved for software interrupts only	1
ARM Core	EmbeddedICE, DbgCommRX	2
ARM Core	EmbeddedICE, DbgCommTX	3
TIMER0	Match 0 to 3 (MR0, MR1, MR2, MR3)	4
TIMER1	Match 0 to 3 (MR0, MR1, MR2, MR3)	5
UART0	RX Line Status (RLS) Transmit Holding Register Empty (THRE) RX Data Available (RDA) Character Time-out Indicator (CTI)	6
UART1	RX Line Status (RLS) Transmit Holding Register empty (THRE) RX Data Available (RDA) Character Time-out Indicator (CTI) Modem Status Interrupt (MSI)	7
PWM0	Match 0 to 6 (MR0, MR1, MR2, MR3, MR4, MR5, MR6)	8
I^2C	SI (state change)	9
SPI0	SPIF, MODF	10
SPI1 and SSP	SPIF, MODF and TXRIS, RXRIS, RTRIS, RORRIS	11
PLL	PLL Lock (PLOCK)	12
RTC	RTCCIF (Counter Increment), RTCALF (Alarm)	13
System Control	External Interrupt 0 (EINT0)	14
	External Interrupt 1 (EINT1)	15
	External Interrupt 2 (EINT2)	16
	External Interrupt 3 (EINT3)	17
A/D	ADC	18

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Table 7. Pin function select register 0 (PINSEL0 - 0xE002 C000) *...continued*

PINSEL0	Pin name	Value		Function	Value after reset
11:10	P0.5	0	0	GPIO Port 0.5	0
		0	1	MISO (SPI0)	
		1	0	Match 0.1 (Timer 0)	
		1	1	reserved	
13:12	P0.6	0	0	GPIO Port 0.6	0
		0	1	MOSI (SPI0)	
		1	0	Capture 0.2 (Timer 0)	
		1	1	reserved	
15:14	P0.7	0	0	GPIO Port 0.7	0
		0	1	SSEL (SPI0)	
		1	0	PWM2	
		1	1	EINT2	
17:16	P0.8	0	0	GPIO Port 0.8	0
		0	1	TXD1 UART1	
		1	0	PWM4	
		1	1	reserved	
19:18	P0.9	0	0	GPIO Port 0.9	0
		0	1	RXD1 (UART1)	
		1	0	PWM6	
		1	1	EINT3	
21:20	P0.10	0	0	GPIO Port 0.10	0
		0	1	RTS1 (UART1)	
		1	0	Capture 1.0 (Timer 1)	
		1	1	reserved	
23:22	P0.11	0	0	GPIO Port 0.11	0
		0	1	CTS1 (UART1)	
		1	0	Capture 1.1 (Timer 1)	
		1	1	reserved	
25:24	P0.12	0	0	GPIO Port 0.12	0
		0	1	DSR1 (UART1)	
		1	0	Match 1.0 (Timer 1)	
		1	1	reserved	
27:26	P0.13	0	0	GPIO Port 0.13	0
		0	1	DTR1 (UART1)	
		1	0	Match 1.1 (Timer 1)	
		1	1	reserved	
29:28	P0.14	0	0	GPIO Port 0.14	0
		0	1	DCD1 (UART1)	
		1	0	EINT1	
		1	1	reserved	

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Table 7. Pin function select register 0 (PINSEL0 - 0xE002 C000) *...continued*

PINSEL0	Pin name	Value		Function	Value after reset
31:30	P0.15	0	0	GPIO Port 0.15	0
		0	1	RI1 (UART1)	
		1	0	EINT2	
		1	1	reserved	

6.7 Pin function select register 1 (PINSEL1 - 0xE002 C004)

The PINSEL1 register controls the functions of the pins as per the settings listed in Table 8. The direction control bit in the IODIR register is effective only when the GPIO function is selected for a pin. For other functions direction is controlled automatically. Settings other than those shown in the Table 8 are reserved, and should not be used.

Table 8. Pin function select register 1 (PINSEL1 - 0xE002 C004)

PINSEL1	Pin name	Value		Function	Value after reset
1:0	P0.16	0	0	GPIO Port 0.16	0
		0	1	EINT0	
		1	0	Match 0.2 (Timer 0)	
		1	1	Capture 0.2 (Timer 0)	
3:2	P0.17	0	0	GPIO Port 0.17	0
		0	1	Capture 1.2 (Timer 1)	
		1	0	SCK (SPI1)	
		1	1	Match 1.2 (Timer 1)	
5:4	P0.18	0	0	GPIO Port 0.18	0
		0	1	Capture 1.3 (Timer 1)	
		1	0	MISO (SPI1)	
		1	1	Match 1.3 (Timer 1)	
7:6	P0.19	0	0	GPIO Port 0.19	0
		0	1	Match 1.2 (Timer 1)	
		1	0	MOSI (SPI1)	
		1	1	Capture 1.2 (Timer 1)	
9:8	P0.20	0	0	GPIO Port 0.20	0
		0	1	Match 1.3 (Timer 1)	
		1	0	SSEL (SPI1)	
		1	1	EINT3	
11:10	P0.21	0	0	GPIO Port 0.21	0
		0	1	PWM5	
		1	0	reserved	
		1	1	Capture 1.3 (Timer 1)	
13:12	P0.22	0	0	GPIO Port 0.22	0
		0	1	reserved	
		1	0	Capture 0.0 (Timer 0)	
		1	1	Match 0.0 (Timer 0)	

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Table 8. Pin function select register 1 (PINSEL1 - 0xE002 C004) *…continued*

PINSEL1	Pin name	Value		Function	Value after reset
15:14	P0.23	0	0	GPIO Port 0.23	0
		0	1	reserved	
		1	0	reserved	
		1	1	reserved	
17:16	P0.24	0	0	GPIO Port 0.24	0
		0	1	reserved	
		1	0	reserved	
		1	1	reserved	
19:18	P0.25	0	0	GPIO Port 0.25	0
		0	1	reserved	
		1	0	reserved	
		1	1	reserved	
21:20	P0.26	0	0	reserved	0
		0	1	reserved	
		1	0	reserved	
		1	1	reserved	
23:22	P0.27	0	0	GPIO Port 0.27	1
		0	1	AIN0 (A/D input 0)	
		1	0	Capture 0.1 (Timer 0)	
		1	1	Match 0.1 (Timer 0)	
25:24	P0.28	0	0	GPIO Port 0.28	1
		0	1	AIN1 (A/D input 1)	
		1	0	Capture 0.2 (Timer 0)	
		1	1	Match 0.2 (Timer 0)	
27:26	P0.29	0	0	GPIO Port 0.29	1
		0	1	AIN2 (A/D input 2)	
		1	0	Capture 0.3 (Timer 0)	
		1	1	Match 0.3 (Timer 0)	
29:28	P0.30	0	0	GPIO Port 0.30	1
		0	1	AIN3 (A/D input 0)	
		1	0	EINT3	
		1	1	Capture 0.0 (Timer 0)	
31:30	P0.31	0	0	reserved	0
		0	1	reserved	
		1	0	reserved	
		1	1	reserved	

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6.8 Pin function select register 2 (PINSEL2 - 0xE002 C014)

The PINSEL2 register controls the functions of the pins as per the settings listed in Table 9. The direction control bit in the IODIR register is effective only when the GPIO function is selected for a pin. For other functions direction is controlled automatically. Settings other than those shown in Table 9 are reserved, and should not be used.

Table 9. Pin function select register 2 (PINSEL2 - 0xE002 C014)

PINSEL2 bits	Description				Reset value
1:0	reserved				-
2	When 0, pins P1[36:26] are used as GPIO pins. When 1, P1[31:26] are used as a Debug port.				$\overline{\text{P1.26/RTCK}}$
3	When 0, pins P1[25:16] are used as GPIO pins. When 1, P1[25:16] are used as a Trace port.				$\overline{\text{P1.20/ TRACESYNC}}$
5:4	Controls the use of the data bus and strobe pins:				BOOT1:0
	Pins P2[7:0]	11	= P2[7:0]	0x or 10 = D7 to D0	
	Pin P1.0	11	= P1.0	0x or 10 = $\overline{\text{CS0}}$	
	Pin P1.1	11	= P1.1	0x or 10 = $\overline{\text{OE}}$	
	Pin P3.31	11	= P3.31	0x or 10 = $\overline{\text{BLS0}}$	
	Pins P2[15:8]	00 or 11	= P2[15:8]	01 or 10 = D15 to D8	
	Pin P3.30	00 or 11	= P3.30	01 or 10 = $\overline{\text{BLS1}}$	
	Pins P2[27:16]	0x or 11	= P2[27:16]	10 = D27 to D16	
	Pins P2[29:28]	0x or 11	= P2[29:28]	10 = D29, D28	
	Pins P2[31:30]	0x or 11	= P2[31:30] or AIN5 to AIN4	10 = D31, D30	
	Pins P3[29:28]	0x or 11	= P3[29:28] or AIN7 to AIN6	10 = $\overline{\text{BLS2}}$, $\overline{\text{BLS3}}$	
6	If bits 5:4 are not 10, controls the use of pin P3.29: 0 enables P3.29, 1 enables AIN6.				1
7	If bits 5:4 are not 10, controls the use of pin P3.28: 0 enables P3.28, 1 enables AIN7.				1
8	Controls the use of pin P3.27: 0 enables P3.27, 1 enables $\overline{\text{WE}}$.				0
10:9	reserved				-
11	Controls the use of pin P3.26: 0 enables P3.26, 1 enables $\overline{\text{CS1}}$.				0
12	reserved				-
13	If bits 27:25 are not 111, controls the use of pin P3.23/A23/XCLK: 0 enables P3.23, 1 enables XCLK.				0
15:14	Controls the use of pin P3.25: 00 enables P3.25, 01 enables $\overline{\text{CS2}}$, 10 and 11 are reserved values.				00
17:16	Controls the use of pin P3.24: 00 enables P3.24, 01 enables $\overline{\text{CS3}}$, 10 and 11 are reserved values.				00
19:18	reserved				-
20	If bits 5:4 are not 10, controls the use of pin P2[29:28]: 0 enables P2[29:28], 1 is reserved				0
21	If bits 5:4 are not 10, controls the use of pin P2.30: 0 enables P2.30, 1 enables AIN4.				1
22	If bits 5:4 are not 10, controls the use of pin P2.31: 0 enables P2.31, 1 enables AIN5.				1

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- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus may be used for test and diagnostic purposes.

6.14 SPI serial I/O controller

The LPC2210/2220 each contain two SPIs. The SPI is a full duplex serial interface, designed to be able to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

6.14.1 Features

- Compliant with SPI specification.
- Synchronous, serial, full duplex, communication.
- Combined SPI master and slave.
- Maximum data bit rate of one eighth of the input clock rate.

6.15 SSP controller

This peripheral is available in LPC2210/01 and LPC2220 only.

6.15.1 Features

- Compatible with Motorola’s SPI, Texas Instrument’s 4-wire SSI, and National Semiconductor’s Microwire buses.
- Synchronous serial communication.
- Master or slave operation.
- 8-frame FIFOs for both transmit and receive.
- 4 bits to 16 bits per frame.

6.15.2 Description

The SSP is a controller capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. Data transfers are in principle full duplex, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master.

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While the SSP and SPI1 peripherals share the same physical pins, it is not possible to have both of these two peripherals active at the same time. Application can switch on the fly from SPI1 to SSP and back.

6.16 General purpose timers

The timer/counter is designed to count cycles of the peripheral clock (PCLK) or an externally supplied clock and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. It also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt. Multiple pins can be selected to perform a single capture or match function, providing an application with ‘or’ and ‘and’, as well as ‘broadcast’ functions among them.

6.16.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Timer operation (LPC2210/2220) or external event counter (LPC2210/01 and LPC2220 only).
- Four 32-bit capture channels per timer/counter that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Four external outputs per timer/counter corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

6.16.2 Features available in LPC2210/01 and LPC2220 only

The LPC2210/01 and LPC2220 can count external events on one of the capture inputs if the external pulse lasts at least one half of the period of the PCLK. In this configuration, unused capture lines can be selected as regular timer capture inputs or used as external interrupts.

- Timer can count cycles of either the peripheral clock (PCLK) or an externally supplied clock.
- When counting cycles of an externally supplied clock, only one of the timer’s capture inputs can be selected as the timer’s clock. The rate of such a clock is limited to PCLK / 4. Duration of high/low levels on the selected capture input cannot be shorter than 1 / (2PCLK).

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controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

6.19.1 Features

- Seven match registers allow up to six single edge controlled or three double edge controlled PWM outputs, or a mix of both types.
- The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go HIGH at the beginning of each cycle unless the output is a constant LOW. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit timer/counter with a programmable 32-bit prescaler.

6.20 System control

6.20.1 Crystal oscillator

The oscillator supports crystals in the range of 1 MHz to 25 MHz and up to 25 MHz with the external oscillator. The oscillator output frequency is called f_{osc} and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. f_{osc} and CCLK are the same value unless the PLL is running and connected. Refer to Section 6.20.2 “PLL” for additional information.

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9. Dynamic characteristics

Table 13. Dynamic characteristics

T_{amb} = 0 °C to +70 °C for commercial applications, −40 °C to +85 °C for industrial applications, $V_{DD(1V8)}$, $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External clock						
f_{osc}	oscillator frequency	supplied by an external oscillator (signal generator)	1	-	25	MHz
		external clock frequency supplied by an external crystal oscillator	1	-	25	MHz
		external clock frequency if on-chip PLL is used	10	-	25	MHz
		external clock frequency if on-chip bootloader is used for initial code download	10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		20	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (except P0.2 and P0.3)						
t_r	rise time		-	10	-	ns
t_f	fall time		-	10	-	ns
I^2C-bus pins (P0.2 and P0.3)						
t_f	fall time	V_{IH} to V_{IL} [2]	$20 + 0.1 \times C_b$	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Bus capacitance C_b in pF, from 10 pF to 400 pF.

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Table 14. External memory interface dynamic characteristics

C_L = 25 pF; T_{amb} = 40 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Common to read and write cycles						
t_{CHAV}	XCLK HIGH to address valid time		-	-	10	ns
t_{CHCSL}	XCLK HIGH to $\overline{CS}$ LOW time		-	-	10	ns
t_{CHCSH}	XCLK HIGH to $\overline{CS}$ HIGH time		-	-	10	ns
t_{CHANV}	XCLK HIGH to address invalid time		-	-	10	ns
Read cycle parameters						
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	[1]	–5	-	+10	ns
t_{OELAV}	$\overline{OE}$ LOW to address valid time	[1]	–5	-	+10	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time		–5	-	+5	ns
t_{am}	memory access time	[2][3] [4]	$(T_{cy(CCLK)} \times (2 + WST1)) + (-20)$	-	-	ns
$t_{am(ibr)}$	memory access time (initial burst-ROM)	[2][3] [4]	$(T_{cy(CCLK)} \times (2 + WST1)) + (-20)$	-	-	ns
$t_{am(sbr)}$	memory access time (subsequent burst-ROM)	[2][5]	$T_{cy(CCLK)} + (-20)$	-	-	ns
$t_{h(D)}$	data hold time	[6]	0	-	-	ns
t_{CSHOEH}	$\overline{CS}$ HIGH to $\overline{OE}$ HIGH time		–5	-	+5	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid time		–5	-	+5	ns
t_{CHOEL}	XCLK HIGH to $\overline{OE}$ LOW time		–5	-	+5	ns
t_{CHOEH}	XCLK HIGH to $\overline{OE}$ HIGH time		–5	-	+5	ns
Write cycle parameters						
t_{AVCSL}	address valid to $\overline{CS}$ LOW time	[1]	$T_{cy(CCLK)} - 10$	-	-	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time		–5	-	+5	ns
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time		–5	-	+5	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time		–5	-	+5	ns
t_{WELDV}	$\overline{WE}$ LOW to data valid time		–5	-	+5	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time		–5	-	+5	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	[2][4]	$T_{cy(CCLK)} \times (1 + WST2) - 5$	-	$T_{cy(CCLK)} \times (1 + WST2) + 5$	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	[2][4]	$T_{cy(CCLK)} \times (1 + WST2) - 5$	-	$T_{cy(CCLK)} \times (1 + WST2) + 5$	ns
t_{WEHANV}	$\overline{WE}$ HIGH to address invalid time	[2]	$T_{cy(CCLK)} - 5$	-	$T_{cy(CCLK)} + 5$	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time	[2]	$(2 \times T_{cy(CCLK)}) - 5$	-	$(2 \times T_{cy(CCLK)}) + 5$	ns
$t_{BLSHANV}$	$\overline{BLS}$ HIGH to address invalid time	[2]	$T_{cy(CCLK)} - 5$	-	$T_{cy(CCLK)} + 5$	ns

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Table 14. External memory interface dynamic characteristics *...continued*

C_L = 25 pF; T_{amb} = 40 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time		[2]	$(2 \times T_{cy(CCLK)}) - 5$	-	$(2 \times T_{cy(CCLK)}) + 5$	ns
t_{CHDV}	XCLK HIGH to data valid time			-	-	10	ns
t_{CHWEL}	XCLK HIGH to $\overline{WE}$ LOW time			-	-	10	ns
t_{CHBLSL}	XCLK HIGH to $\overline{BLS}$ LOW time			-	-	10	ns
t_{CHWEH}	XCLK HIGH to $\overline{WE}$ HIGH time			-	-	10	ns
t_{CHBLSH}	XCLK HIGH to $\overline{BLS}$ HIGH time			-	-	10	ns
t_{CHDNV}	XCLK HIGH to data invalid time			-	-	10	ns

[1] Except on initial access, in which case the address is set up $T_{cy(CCLK)}$ earlier.

[2] $T_{cy(CCLK)} = {}^{1}/_{CCLK}$.

[3] Latest of address valid, $\overline{CS}$ LOW, $\overline{OE}$ LOW to data valid.

[4] See the *LPC2210/20 user manual UM10114_1* for a description of the WSTn bits.

[5] Address valid to data valid.

[6] Earliest of $\overline{CS}$ HIGH, $\overline{OE}$ HIGH, address change to data invalid.

Table 15. Standard read access specifications

Access cycle	Max frequency	WST setting WST ≥ 0; round up to integer	Memory access time requirement
standard read	$f_{MAX} \leq \frac{2 + WST1}{t_{RAM} + 20\ ns}$	$WST1 \geq \frac{t_{RAM} + 20\ ns}{t_{cy(CCLK)}} - 2$	$t_{RAM} \leq t_{cy(CCLK)} \times (2 + WST1) - 20\ ns$
standard write	$f_{MAX} \leq \frac{1 + WST2}{t_{WRITE} + 5\ ns}$	$WST2 \geq \frac{t_{WRITE} - t_{CYC} + 5}{t_{cy(CCLK)}}$	$t_{WRITE} \leq t_{cy(CCLK)} \times (1 + WST2) - 5\ ns$
burst read - initial	$f_{MAX} \leq \frac{2 + WST1}{t_{INIT} + 20\ ns}$	$WST1 \geq \frac{t_{INIT} + 20\ ns}{t_{cy(CCLK)}} - 2$	$t_{INIT} \leq t_{cy(CCLK)} \times (2 + WST1) - 20\ ns$
burst read - subsequent 3×	$f_{MAX} \leq \frac{1}{t_{ROM} + 20\ ns}$	N/A	$t_{ROM} \leq t_{cy(CCLK)} - 20\ ns$

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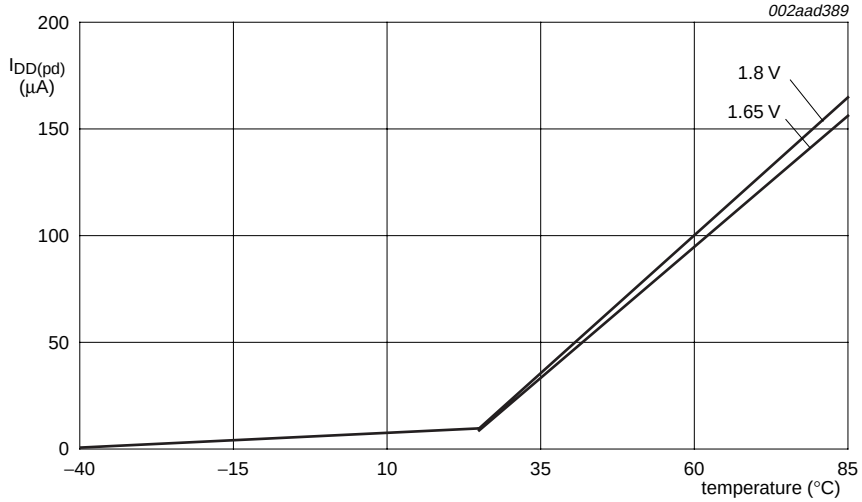

Test conditions: Power-down mode entered executing code from on-chip RAM; all peripherals are enabled in PCONP register.

Fig 14. LPC2220 and LPC2210/01 I_{DD} in Power-down mode measured at different temperatures

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15. Contents

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