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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	27
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.5К х 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21336mnfp-30

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Item	Function	Specification
Serial	UART0, UART1	Clock synchronous serial I/O/UART × 2 channel
Interface	UART2	Clock synchronous serial I/O/UART, I ² C mode (I ² C-bus), multiprocessor communication function
Synchronous	Serial	1 (shared with I ² C-bus)
Communicatio	on Unit (SSU)	
I ² C bus		1 (shared with SSU)
LIN Module		Hardware LIN: 1 (timer RA, UART0)
A/D Converte	r	10-bit resolution \times 12 channels, includes sample and hold function, with sweep mode
D/A Converte	r	8-bit resolution x 2 circuits
Comparator A	A	 2 circuits (shared with voltage monitor 1 and voltage monitor 2)
		 External reference voltage input available
Comparator E	3	2 circuits
Flash Memory	у	 Programming and erasure voltage: VCC = 2.7 to 5.5 V
		 Programming and erasure endurance: 10,000 times (data flash)
		1,000 times (program ROM)
		 Program security: ROM code protect, ID code check
		 Debug functions: On-chip debug, on-board flash rewrite function
		Background operation (BGO) function
Operating Fre	equency/Supply	f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V)
Voltage		$f(XIN) = 5 \text{ MHz} (VCC = 1.8 \text{ to } 5.5 \text{ V})^{2}$
Current Cons	umption	Typ. 6.5 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 3.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 3.5 μ A (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)) Typ. 2.0 μ A (VCC = 3.0 V, stop mode)
Operating Am	bient Temperature	-20 to 85°C (N version) -40 to 85°C (D version) ⁽¹⁾
Package		32-pin LQFP
		Package code: PLQP0032GB-A (previous code: 32P6U-A)

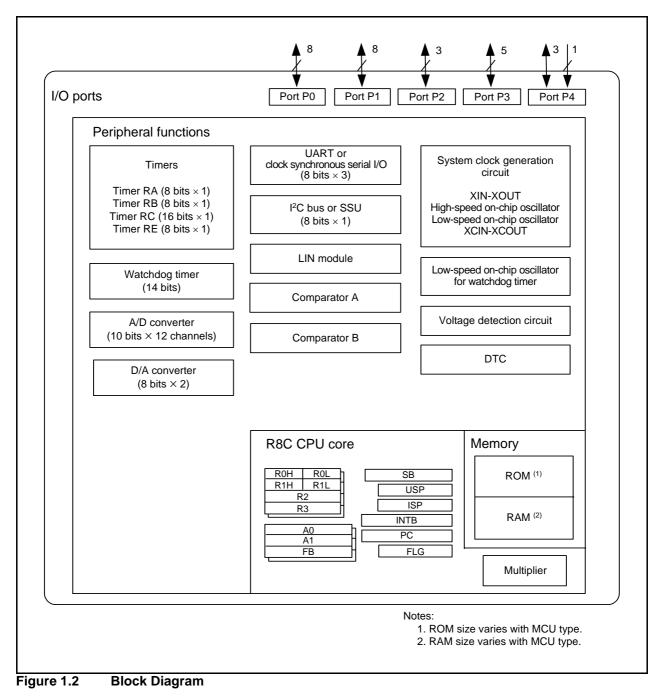
Table 1.2	Specifications	for R8C/33M	Group (2)

Note: 1. Specify the D version if D version functions are to be used.



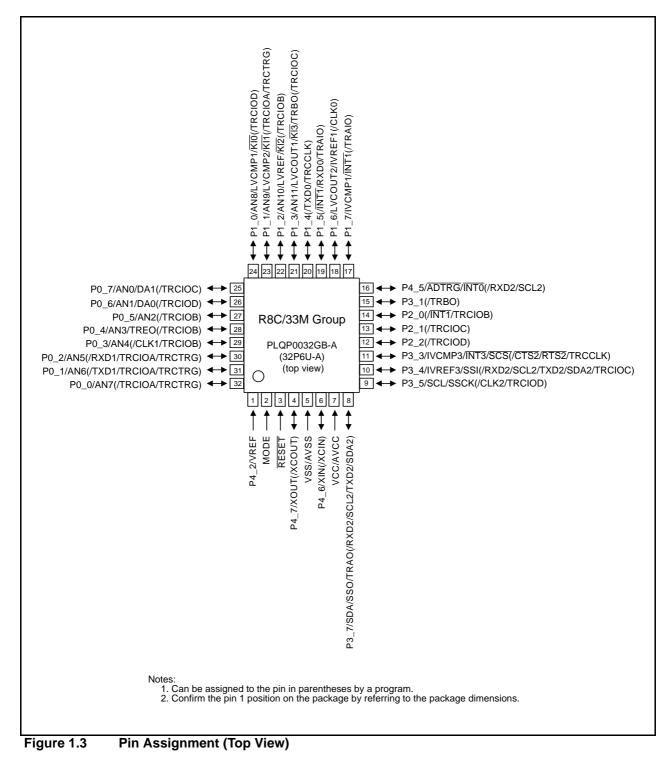
1.3 Block Diagram

Figure 1.2 shows a Block Diagram.



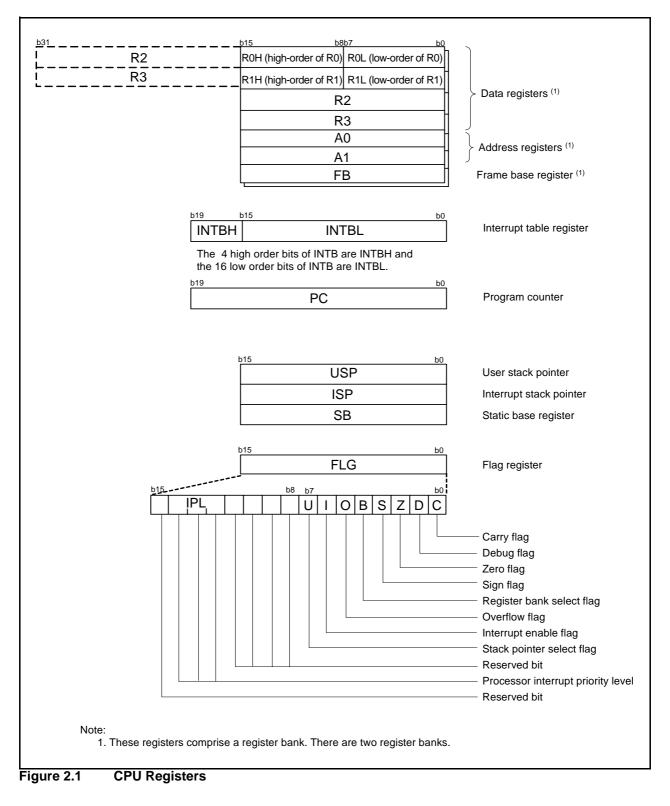
1.4 Pin Assignment

Figure 1.3 shows Pin Assignment (Top View). Table 1.4 outlines the Pin Name Information by Pin Number.



2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.



Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Eh	SSU Interrupt Control Register / IIC bus Interrupt Control Register ⁽²⁾	SSUIC / IICIC	XXXXX000b
004FN 0050h		00010 / 11010	~~~~~
	LIADTO Transmit Interrupt Control Degister	COTIC	
0051h	UARTO Transmit Interrupt Control Register	SOTIC	XXXXX000b
0052h	UARTO Receive Interrupt Control Register	SORIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INTOIC	XX00X000b
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
0069h			
006An 006Bh			
006Bh			
006Ch 006Dh			
006Eh			
006Fh			
0070h			
0071h		1/01/5//2	
0072h	Voltage Monitor 1/Compare A1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage Monitor 2/Compare A2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0078h 0079h			
0078h			
0078h 0079h			
0078h 0079h 007Ah			
0078h 0079h 007Ah 007Bh			
0078h 0079h 007Ah 007Bh 007Ch			

SFR Information (2)⁽¹⁾ Table 4.2

Notes: 1. The blank areas are reserved and cannot be accessed by users. 2. Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.8	SFR Information (8) ⁽¹⁾
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Address Register Symbol Attresset 01Cbh Address Match Interrupt Register 0 RMAD 0 XXh 01Cbh Address Match Interrupt Enable Register 0 AIER0 0000/XXXb 01Cbh Address Match Interrupt Enable Register 1 AIER1 00h 01Cbh Address Match Interrupt Enable Register 1 AIER1 0h 01Cbh Address Match Interrupt Enable Register 1 AIER1 0h 01Cbh Address Match Interrupt Enable Register 1 AIER1 0h 01Cbh Interrupt Enable Register 1 AIER1 Interrupt Enable Register 1 01Cbh Interrupt Enable Register 1 AIER1 Interrupt Enable Register 1 01Cbh Interrupt Enable Register 1 Interrupt Enable Register 1 Interrupt Enable Register 1 01Cbh Interrupt Enable Register 1 Interrupt Enable Register 1 Interrupt Enable Register 1	A -1.1		0	A4 D (
OTOTAL XN 000XXXXb 01C2h Address Match Interrupt Enable Register 0 AIERO 006 01C3h Address Match Interrupt Register 1 RMAD1 XXh 01C3h Address Match Interrupt Register 1 AIERO 000 01C3h Address Match Interrupt Enable Register 1 AIER1 00h 01C3h Address Match Interrupt Enable Register 1 AIER1 00h 01C3h Address Match Interrupt Enable Register 1 AIER1 00h 01C3h - - - - 01C3h - - - - - 01C3h - - - - - - 01C3h - <t< td=""><td></td><td></td><td></td><td></td></t<>				
0102h Adress Match Interrupt Enable Register 0 AER 0000XXXXb 0102h Address Match Interrupt Register 1 RMAD1 XXh 0102bn Address Match Interrupt Register 1 AIER1 000 0102bn Address Match Interrupt Enable Register 1 AIER1 000 0102bn Address Match Interrupt Enable Register 1 AIER1 000 0102bn Address Match Interrupt Enable Register 1 AIER1 000 0102bn Interrupt Enable Register 1 AIER1 000 0102bn Interrupt Enable Register 1 Interrupt Enable Register 1 Interrupt Enable Register 1 0102bn Interrupt Enable Register 1 Interrupt Enable Register 1 Interrupt Enable Register 1 Interrupt Enable Register 1 0102bn Interrupt Enable Register 1 Interrupt Enable R		Address Match Interrupt Register 0	RMAD0	
01C3h Address Match Interrupt Register 0 AIER0 Ohn 01C3h Address Match Interrupt Register 1 RMAD1 XXh 01C6h Address Match Interrupt Enable Register 1 AIER1 00h 01C6h AIdress Match Interrupt Enable Register 1 AIER1 00h 01C6h Image: Comparison of the second of				
OTCAh Address Match Interrupt Register 1 NAh XXh OTCSh 0000XXXXb 0000XXXb 0000XXXb OTCSh 01Ch Address Match Interrupt Enable Register 1 AIE1 00h OTCSh 0 0 0 0 0 OTCSh 0 0 0 0 0 OTCSh 0 0 0 0 0 OTCSh 0 0 0 0 0 0 OTCSh 0 </td <td></td> <td></td> <td></td> <td>0000XXXXb</td>				0000XXXXb
OTCSh XXh XXh OTCSh Address Match Interrupt Enable Register 1 AIER1 Oth OTCSh Address Match Interrupt Enable Register 1 AIER1 Oth OTCSh Image: Comparison of the second of the secon	01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
OTCSh XXh XXh OTCSh Address Match Interrupt Enable Register 1 AIER1 Oth OTCSh Address Match Interrupt Enable Register 1 AIER1 Oth OTCSh Image: Comparison of the second of the secon	01C4h		RMAD1	XXh
0102h Adress Match Interrupt Enable Register 1 AIR1 0000XXXXb 0102h Adress Match Interrupt Enable Register 1 AIR1 00h 0102h Adress Match Interrupt Enable Register 1 Image: Comparison of the compa				
01C7h Address Match Interrupt Enable Register 1 AIER1 00h 01C8h				
01C8h		Address Motoh Interrunt Englis Deviator 1		
0102h		Address Match Interrupt Enable Register 1	AIER1	UUN
01CAh				
01CBh				
01CCh	01CAh			
01CCh	01CBh			
01CDh				
01CEh				
01CFh				
OfDDn				
01D1h				
01D2h				
01D3h	01D1h			
01D3h	01D2h			
0104h			1	
0105h				
0106h				
0107h				
0109h				
0109h				
01DAh				
01DAh	01D9h			
01DBh				
01DCh				
01DDh			-	
01DEh Pull-Up Control Register 0 PUR0 00h 01Eih Pull-Up Control Register 1 PUR1 00h 01E3h PUR1 00h 01E3h <				
01DFh Pull-Up Control Register 0 PUR0 00h 01E1h Pull-Up Control Register 1 00h 01E2h 00h 01E2h PUR1 00h 01E3h 00h 01E3h PUR1 00h 01E3h 00h 01E3h PUR1 00h 01E3h 01E3h 01E3h 01E3h PUR1 PUR1 01h 01E3h 00h 01F3h 00h 01F3h				
O1E0h PuIk-Up Control Register 0 PUR0 O0h 01E1h PuIk-Up Control Register 1 PUR1 O0h 01E3h 01E3h 01E3h 01E3h 01E4h				
01E1h Pull-Up Control Register 1 PUR1 00h 01E2h				
01E1h Pull-Up Control Register 1 PUR1 00h 01E2h 01E3h 01E3h 01E4h 01E6h	01E0h	Pull-Up Control Register 0	PUR0	00h
01E2h	01E1h		PUR1	00h
01E3h				
01E4h				
01E5h				
01E6h	01E4h			
01E7h				
01E8hImage: constraint of the second sec				
01E9h	01E7h			
01E9h	01E8h			
01EAhImage: constraint of the second sec				
01EBh01ECh01ECh01ECh				
01ECh				
01EDhImage: constraint of the second sec				_
01EEhImage: constraint of the second sec				
01EFhPort P1 Drive Capacity Control RegisterP1DRR00h01F0hPort P2 Drive Capacity Control RegisterP2DRR00h01F2hDrive Capacity Control Register 0DRR000h01F3hDrive Capacity Control Register 1DRR100h01F5hInput Threshold Control Register 0VLT000h01F6hInput Threshold Control Register 1VLT000h01F6hInput Threshold Control Register 1VLT100h01F7h00h00h01F8h00h01F8hComparator B Control Register 0INTCMP00h01F8hComparator B Control Register 0INTEN00h01FAhExternal Input Enable Register 0INTEN00h01FChINT Input Filter Select Register 0INTF00h01FChINT Input Filter Select Register 0INTF00h01FChINT00h01FBh00h01FChINTNother00h01FChINT Input Filter Select Register 0INTF00h01FChINT00h00h00h01FChINTNother00h01FChKey Input Enable Register 0KIEN00h01FFhVV00h00h				
01F0hPort P1 Drive Capacity Control RegisterP1DRR00h01F1hPort P2 Drive Capacity Control Register 0DRR000h01F2hDrive Capacity Control Register 0DRR000h01F3hDrive Capacity Control Register 1DRR100h01F4h01F5hInput Threshold Control Register 0VLT000h01F6hInput Threshold Control Register 1VLT000h01F7h01F8hComparator B Control Register 0INTCMP00h01F8hComparator B Control Register 0INTEN00h01F8hComparator B Control Register 0INTF00h01F0hControl Register 0INTF00h01F0hControl Register 0INTF00h01F6hINT Input Filter Select Register 0INTF00h01F6hControl Register 0INTF00h01F6hKey Input Enable Register 0KIEN00h01F6hControl Register 0Control Register 0Control Register 001F6hControl Register 0Control Register 0				
01F0hPort P1 Drive Capacity Control RegisterP1DRR00h01F1hPort P2 Drive Capacity Control Register 0DRR000h01F2hDrive Capacity Control Register 0DRR000h01F3hDrive Capacity Control Register 1DRR100h01F4h01F5hInput Threshold Control Register 0VLT000h01F6hInput Threshold Control Register 1VLT000h01F7h01F8hComparator B Control Register 0INTCMP00h01F8hComparator B Control Register 0INTEN00h01F8hComparator B Control Register 0INTF00h01F0hControl Register 0INTF00h01F0hControl Register 0INTF00h01F6hINT Input Filter Select Register 0INTF00h01F6hControl Register 0INTF00h01F6hKey Input Enable Register 0KIEN00h01F6hControl Register 0Control Register 0Control Register 001F6hControl Register 0Control Register 0	01EFh			
01F1hPort P2 Drive Capacity Control RegisterP2DRR00h01F2hDrive Capacity Control Register 0DRR000h01F3hDrive Capacity Control Register 1DRR100h01F4h01F5hInput Threshold Control Register 0VLT000h01F6hInput Threshold Control Register 1VLT100h01F7h01F8hComparator B Control Register 0INTCMP00h01F9h01FAhExternal Input Enable Register 0INTEN00h01FBh01FChINT Input Filter Select Register 0INTF00h01FDh </td <td></td> <td>Port P1 Drive Capacity Control Register</td> <td>P1DRR</td> <td>00h</td>		Port P1 Drive Capacity Control Register	P1DRR	00h
01F2hDrive Capacity Control Register 0DRR000h01F3hDrive Capacity Control Register 1DRR100h01F4h01F5hInput Threshold Control Register 0VLT000h01F6hInput Threshold Control Register 1VLT100h01F7h01F8hComparator B Control Register 0INTCMP00h01F9h01F8hExternal Input Enable Register 0INTEN00h01F8h01F8hINT Input Filter Select Register 0INTF00h01FCh </td <td>01F1h</td> <td>Port P2 Drive Capacity Control Register</td> <td></td> <td></td>	01F1h	Port P2 Drive Capacity Control Register		
01F3h Drive Capacity Control Register 1 DRR1 00h 01F4h 01F5h Input Threshold Control Register 0 VLT0 00h 01F6h Input Threshold Control Register 1 VLT1 00h 01F7h 01F8h Comparator B Control Register 0 INTCMP 00h 01F9h 01F8h Comparator B Control Register 0 INTEM 00h 01F8h External Input Enable Register 0 INTEN 00h 01FBh 00h 00h 00h				
01F4h VLT0 00h 01F5h Input Threshold Control Register 0 VLT0 00h 01F6h Input Threshold Control Register 1 VLT1 00h 01F7h VLT1 00h 00h 01F8h Comparator B Control Register 0 INTCMP 00h 01F9h INTEN 00h 00h 01F8h External Input Enable Register 0 INTEN 00h 01F8h INT Input Filter Select Register 0 INTF 00h 01FCh INT Input Filter Select Register 0 INTF 00h 01FCh INT Input Filter Select Register 0 INTF 00h 01FEh Key Input Enable Register 0 KIEN 00h 01FFh				
01F5h Input Threshold Control Register 0 VLT0 00h 01F6h Input Threshold Control Register 1 VLT1 00h 01F7h 01F8h Comparator B Control Register 0 INTCMP 00h 01F9h 01FAh External Input Enable Register 0 INTEN 00h 01FBh 01FCh INT Input Filter Select Register 0 INTF 00h 01FDh 01FCh INT Input Filter Select Register 0 INTF 00h 01FDh 01FFh Key Input Enable Register 0 KIEN 00h		Drive Capacity Control Register 1	UKK1	UUN
01F6h Input Threshold Control Register 1 VLT1 00h 01F7h INTCMP 00h 01F8h Comparator B Control Register 0 INTCMP 00h 01F9h INTEN 00h 01FAh External Input Enable Register 0 INTEN 00h 01FBh INTFN 00h 01FCh INT Input Filter Select Register 0 INTF 00h 01FDh INTFN 00h 01FDh INTF 00h 01FEh Key Input Enable Register 0 KIEN 00h 01FFh VLT1 00h INTF INTF				
01F6h Input Threshold Control Register 1 VLT1 00h 01F7h INTCMP 00h 01F8h Comparator B Control Register 0 INTCMP 00h 01F9h INTEN 00h 01FAh External Input Enable Register 0 INTEN 00h 01FBh INTFN 00h 01FCh INT Input Filter Select Register 0 INTF 00h 01FDh INTFN 00h 01FDh INTF 00h 01FEh Key Input Enable Register 0 KIEN 00h 01FFh VLT1 00h INTF INTF			VLT0	00h
01F7h Image: Constraint of C		Input Threshold Control Register 1	VLT1	00h
01F8h Comparator B Control Register 0 INTCMP 00h 01F9h INTEN 00h 01FAh External Input Enable Register 0 INTEN 00h 01FBh INT Input Filter Select Register 0 INTF 00h 01FCh INT Input Filter Select Register 0 INTF 00h 01FDh INTF 00h 01FEh Key Input Enable Register 0 KIEN 00h 01FFh View Input Enable Register 0 Kien 00h		· · · · · · · · · · · · · · · · · · ·		
01F9h INTEN 00h 01FAh External Input Enable Register 0 INTEN 00h 01FBh INT Input Filter Select Register 0 INTF 00h 01FDh INTF 00h 01FEh Key Input Enable Register 0 KIEN 00h 01FFh Intersection of the select Register 0 Intersection of the select Register 0	01F8h	Comparator B Control Register 0	INTCMP	00h
01FAh External Input Enable Register 0 INTEN 00h 01FBh 01FCh INT Input Filter Select Register 0 INTF 00h 01FDh 01FDh 00h 00h 01FEh Key Input Enable Register 0 KIEN 00h 01FFh 00h 00h 00h				
01FBh 01FCh INT Input Filter Select Register 0 INTF 00h 01FDh 01FEh Key Input Enable Register 0 KIEN 00h 01FFh 01FFh 00h 00h 00h		Esternel Innut English Deviator (0.01
01FCh INT Input Filter Select Register 0 INTF 00h 01FDh 01FEh KIEN 00h 01FFh KIEN 00h		External input Enable Register U	INTEN	UUN
01FDh 01FEh 01FEh Key Input Enable Register 0 01FFh KIEN				
01FDh 01FEh 01FEh Key Input Enable Register 0 01FFh KIEN		INT Input Filter Select Register 0	INTF	00h
01FEh Key Input Enable Register 0 KIEN 00h 01FFh 00h				
01FFh	01FEh	Key Input Enable Register 0	KIEN	00h
	X: Undefined		1	

X: Undefined Note: 1. The blank areas are reserved and cannot be accessed by users.

2270h DTC Control Data 6 DTC Source Data 6 XNn 2277h XNn XNn 2277h XNn XNn 277h XNn XNn	Address	Register	Symbol	After Reset
2271h Xh 2272h Xh 2273h Xh 2274h Xh 2274h Xh 2274h Xh 2274h Xh 2277h Xh 227h DTC Control Data 7 227h Xh 228h DTC Control Data 8 228h DTC Control Data 9 228h DTC Control Data 10 228h DTC Control Data 10				
2272h Xh 2273h Xh 2273h Xh 2273h Xh 2275h Xh 2275h Xh 277b				
2273h Xh 2274h Xh 2277h Xh 2277h Xh 2277h Xh 2277h DTC Control Data 7 Xh 2277h Xh Xh 2267h Xh Xh 2268h DTC Control Data 8 DTCD8 Xh 2268h ZCRh Xh Xh 2268h ZCRh Xh Xh 2268h ZCRh Xh Xh 2268h ZCRh Xh Xh 2268h DTC Control Data 10 DTCD10 Xh 2268h ZCRh Xh		4		
2273h Xh 2275h Xh 2277h DTC control Data 7 277b DTC control Data 7 277b DTC control Data 7 277b Xh 277b <t< td=""><td></td><td>4</td><td></td><td></td></t<>		4		
2278h Xh 2277h Xh 2267h Yh 2268h Xh 2268h Xh <td></td> <td>4</td> <td></td> <td></td>		4		
2C7/h XXh 2C8/h XXh 2C8/h </td <td></td> <td>4</td> <td></td> <td></td>		4		
2C77h Xh 2C78h DTC Control Data 7 2C78h XKh 2C78h XKh 2C78h XKh 2C78h XKh 2C7Rh XKh 2C7Rh XKh 2C7bh XKh 2C8bh DTC Control Data 8 2C8bh XXh		4		
2C78h DTC Control Data 7 XXh 2C79h XXh XXh 2C77h XXh XXh 2C77h XXh XXh 2C77h XXh XXh 2C7bh XXh XXh 2C7bh XXh XXh 2C7bh XXh XXh 2C7bh XXh XXh 2C68h XXh XXh 2C8h XXh XXh 2C8h </td <td></td> <td>4</td> <td></td> <td></td>		4		
2C79h XXh 2C7Ah XXh 2C7Bh XXh 2C7Ch XXh 2C7Ch XXh 2C7Fh XXh 2C60h DTC Control Data 8 2C62h XXh		DTO Original Data 7	DTOD7	
2C7Ah Xxh 2C7Bh Xxh 2C7Ch Xxh 2C7Dh Xxh 2C7Dh Xxh 2C7Dh Xxh 2C7Dh Xxh 2C7Dh Xxh 2C7Ph Xxh 2C81h Xxh 2C84h Xxh 2C87h Xxh 2C87h </td <td></td> <td>DIC Control Data 7</td> <td>DICD7</td> <td></td>		DIC Control Data 7	DICD7	
2C7Rh Xh 2C7Ch Xh 2C8h Xh 2C		4		
2C7Ch Xin 2C7Dh Xin 2C7Fh Xin 2C7Fh Xin 2C7Fh Xin 2C87h Xin 2C87h Xin 2C88h Xin 2C88h </td <td></td> <td></td> <td></td> <td></td>				
2C7Dh Xh 2C7Fh Xh 2C80h DTC Control Data 8 2C81h Xh 2C85h Xh 2C85h Xh 2C85h Xh 2C86h Xh 2C87h Xh 2C88h				
2C7Eh Xh 2C7Fh Xh 2C7Fh Xh 2C8h DTC Control Data 8 2C8h Xh 2C8h TC Control Data 9 2C8h DTC Control Data 9 2C8h TC Control Data 9 2C8h TC Control Data 9 2C8h DTC Control Data 9 2C8h Xh 2C9h Xh 2C9h Xh 2C9h Xh 2C3h Xh 2C3h Xh 2C3h Xh </td <td></td> <td></td> <td></td> <td></td>				
2C7Fh Xh 2C80h DTC Control Data 8 Xh 2C81h DTC Control Data 8 Xh 2C81h Xh Xh 2C81h Cash Xh 2C81h Control Data 9 Xh 2C81h DTC Control Data 9 Xh 2C81h DTC Control Data 10 DTCD9 Xh 2C82h Xh Xh Xh 2C82h Xh Xh Xh 2C82h TC Control Data 10 DTCD10 Xh 2C82h Xh Xh Xh 2C82h TC Control Data 10 TC Control Data 10 Xh 2C82h Xh Xh Xh 2C82h Xh Xh Xh 2C82h Xh Xh Xh <				
12 C30h 2 C3h 2 C3h				
2281h Xh 2C32h Xh 2C33h Xh 2C34h Xh 2C35h Xh 2C36h TC Control Data 9 2C38h DTC Control Data 9 2C38h Xh 2C38h TC Control Data 9 2C38h DTC Control Data 9 2C38h Xh 2C38h TC Control Data 10 2C39h TC Control Data 11 2C39h TC Control Data 12 2C4Ah TXh 2C39h TC Control Data 12 2C4Ah TXh				
2C82h Xxh Xxh 2C83h Xxh Xxh 2C83h Xxh Xxh 2C88h DTC Control Data 9 Xxh 2C88h DTC Control Data 9 Xxh 2C88h Xxh Xxh 2C89h Xxh Xxh 2C99h Xxh Xxh <td></td> <td>DTC Control Data 8</td> <td>DTCD8</td> <td></td>		DTC Control Data 8	DTCD8	
2/283h 2/264h Xxh 2/268h Xxh Xxh 2/269h Xxh Xxh	2C81h			XXh
2/283h 2/264h Xxh 2/268h Xxh Xxh 2/269h Xxh Xxh	2C82h]		
2C84h Xxh Xxh 2C85h Xxh Xxh 2C88h DTC Control Data 9 Xxh 2C88h DTC Control Data 9 Xxh 2C88h Xxh Xxh 2C99h DTC Control Data 10 DTCD10 Xxh 2C99h Xxh Xxh Xxh	2C83h]		XXh
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ZC9EhXXh2C3FhDTC Control Data 12DTCD12XXh2CA0hDTC Control Data 12DTCD12XXh2CA2hZCA3hXXhXXh2CA3hZCA4hXXhXXh2CA4hZCA4hXXhXXh2CA4hZCA5hXXhXXh2CA4hZCA6hXXhXXh2CA6hZCA7hXXhXXh2CA8hDTC Control Data 13DTC Control Data 13DTCD13XXh2CA8hZCA9hXXhXXh2CA8hZCAAhXXhXXh2CA8hZCAAhXXhXXh2CAAhZCAAhXXhXXh2CAAhZCAAhXXhXXh2CAAhZCAAhXXhXXh2CAAhZCAAhXXhXXh2CAAhZCAAhXXhXXh2CAAhZCAAHXXhXXh2CAAhZCAAHXXhXXh2CAAhZCAAHXXhXXh2CAAHZCAAHXXhXXh2CAAHXXhXXhXXh2CAAHXXhXXhXXh2CAAHXXhXXhXXh2CAAHXXhXXhXXh2CAAHXXhXXhXXh2CAAHXXhXXhXXh2CAAHXXhXXhXXh2CAAHXXhXXhXXh2CAAHXXhXXhXXh2CAAHXXhXXhXXH2CAAHXXHXXHXXH <td>2C9Ch</td> <td>]</td> <td></td> <td></td>	2C9Ch]		
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2C9FhXXh2CA0hDTC Control Data 12DTCD12XXh2CA1hXXhXXh2CA2hXXhXXh2CA3hXXhXXh2CA4hXXhXXh2CA4hXXhXXh2CA5hXXhXXh2CA6hXXhXXh2CA8hDTC Control Data 13XXh2CA8hDTC Control Data 13DTCD13XXh2CA8hZCA9hXXhXXh2CA8hZCA8hXXhXXh2CA8hZCAAhXXhXXh2CA8hZCAAhXXhXXh2CAAhZCAAhXXhXXh2CAAhZCAChXXhXXh2CAChXXhXXhXXh2CAAhZCAAhXXhXXh2CAAhZCAAhXXhXXh2CAAhXXhXXhXXh2CAAhXXhXXhXXh2CAFhXXhXXhXXh]		XXh
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2CA6h XXh 2CA7h XXh 2CA8h DTC Control Data 13 2CA9h ZCA9h 2CAAh XXh 2CACh XXh 2CAAh XXh 2CAAh XXh 2CAAh XXh 2CAAh XXh		1		
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2CA8h 2CA9h 2CAAhDTC Control Data 13DTCD13XXh XXh2CAAh 2CABhZCACh 2CAChXXhXXh2CADh 2CAEhXXhXXh2CAFhXXhXXh		1		
2CA9hXXh2CAAhXXh2CABhXXh2CAChXXh2CADhXXh2CAEhXXh2CAFhXXh		DTC Control Data 13		
2CAAhXXh2CABhXXh2CAChXXh2CADhXXh2CAEhXXh2CAFhXXh			010013	
2CABhXXh2CAChXXh2CADhXXh2CAEhXXh2CAFhXXh		4		
2CACh XXh 2CADh XXh 2CAEh XXh 2CAFh XXh		4		
2CADh XXh 2CAEh XXh 2CAFh XXh	2CABN	4		
2CAEh XXh 2CAFh XXh		4		
2CAFh XXh		4		
		4		
	2CAFh			XXN

X: Undefined Note: 1. The blank areas are reserved and cannot be accessed by users.

Address	Register	Symbol	After Reset
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h		DIODI4	XXh
2CB1h	4		XXh
	4		
2CB3h	4		XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh	-		XXh
2CBBh	4		XXh
2CBDh	-		XXh
	4		
2CBDh	-		XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h	1		XXh
2CC3h	1		XXh
2000h	1		XXh
2CC5h	4		XXh
	4		XXh
2CC6h	-		
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh	-		XXh
2CCEh			XXh
2CCFh	4		XXh
	DTC Control Data 10	DTCD18	
2CD0h	DTC Control Data 18	DICD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h	4		XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD0h		DICDIS	XXh
	-		
2CDAh	-		XXh
2CDBh	4		XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh]		XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
20E111	4		XXh
2CE3h	4		XXh
	4		
2CE4h	4		XXh
2CE5h	4		XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h	1		XXh
2CEAh	1		XXh
2CEBh	1		XXh
2CEDh	4		XXh
	4		
2CEDh	4		XXh
2CEEh	4		XXh
2CEFh			XXh
X. Undefined			

SFR Information (11)⁽¹⁾ Table 4.11

X: Undefined Note: 1. The blank areas are reserved and cannot be accessed by users.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
Vcc/AVcc	Supply voltage		-0.3 to 6.5	V
Vi	Input voltage		-0.3 to Vcc + 0.3	V
Vo	Output voltage		-0.3 to Vcc + 0.3	V
Pd	Power dissipation	$-40^{\circ}C \le T_{opr} \le 85^{\circ}C$	500	mW
Topr	Operating ambient temperature		-20 to 85 (N version) / -40 to 85 (D version)	°C
Tstg	Storage temperature		-65 to 150	°C



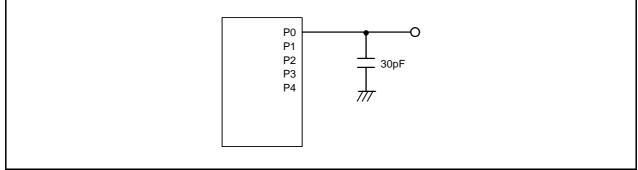


Figure 5.1 Ports P0 to P4 Timing Measurement Circuit



Symbol	Parameter	Conditions	Standard			Unit
Symbol		Conditions	Min.	Тур.	Max.	Unit
-	Program/erase endurance (2)		10,000 (3)	-	-	times
-	Byte program time (program/erase endurance ≤ 1,000 times)		-	160	1,500	μS
-	Byte program time (program/erase endurance > 1,000 times)		-	300	1,500	μs
-	Block erase time (program/erase endurance ≤ 1,000 times)		-	0.2	1	S
-	Block erase time (program/erase endurance > 1,000 times)		-	0.3	1	S
td(SR-SUS)	Time delay from suspend request until suspend		-	-	5+CPU clock × 3 cycles	ms
-	Interval from erase start/restart until following suspend request		0	-	_	μS
-	Time from suspend until erase restart		-	I	30+CPU clock × 1 cycle	μs
td(CMDRST- READY)	Time from when command is forcibly terminated until reading is enabled		-	-	30+CPU clock × 1 cycle	μs
-	Program, erase voltage		2.7	-	5.5	V
-	Read voltage		1.8	-	5.5	V
-	Program, erase temperature		-20 (7)	-	85	°C
-	Data hold time ⁽⁸⁾	Ambient temperature = 55 °C	20	-	-	year

Table 5.8 Flash Memory (Data flash Block A to Block D) Electrical Characteristics

Notes:

1. Vcc = 2.7 to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

2. Definition of programming/erasure endurance

The programming and erasure endurance is defined on a per-block basis. If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.

However, the same address must not be programmed more than once per erase operation (overwriting prohibited).

3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).

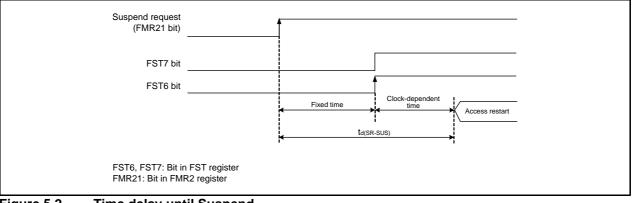
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.

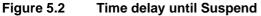
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.

6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.

7. -40°C for D version.

8. The data hold time includes time that the power supply is off or the clock is not supplied.





Cumhal	Devenueter		Standard			Unit
Symbol	Parameter	Condition	Min.	Тур.	Max.	Unit
Vdet0	Voltage detection level Vdet0_0 ⁽²⁾		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 (2)		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (2)		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 ⁽²⁾		3.55	3.80	4.05	V
-	Voltage detection 0 circuit response time ⁽⁴⁾	At the falling of Vcc from 5 V to (Vdet0_0 – 0.1) V	-	6	150	μS
-	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	-	1.5	-	μΑ
td(E-A)	Waiting time until voltage detection circuit operation starts $^{\rm (3)}$		-	-	100	μS

Table 5.9 **Voltage Detection 0 Circuit Electrical Characteristics**

Notes:

1. The measurement condition is Vcc = 1.8 V to 5.5 V and $T_{opr} = -20$ to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version). 2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.

3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

4. Time until the voltage monitor 0 reset is generated after the voltage passes Vdet0.

Table 5.10 Voltage Detection 1 Circuit Electrical Characteri
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Symbol	Parameter	Condition		1	Unit	
Symbol	Falailletei	Condition	Min.	Тур.	Max.	Unit
Vdet1	Voltage detection level Vdet1_0 ⁽²⁾	At the falling of Vcc	2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 ⁽²⁾	At the falling of Vcc	2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 (2)	At the falling of Vcc	2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 (2)	At the falling of Vcc	2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 (2)	At the falling of Vcc	2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 ⁽²⁾	At the falling of Vcc	2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 ⁽²⁾	At the falling of Vcc	2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 ⁽²⁾	At the falling of Vcc	3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 (2)	At the falling of Vcc	3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 ⁽²⁾	At the falling of Vcc	3.30	3.55	3.85	V
	Voltage detection level Vdet1_A ⁽²⁾	At the falling of Vcc	3.45	3.70	4.00	V
	Voltage detection level Vdet1_B (2)	At the falling of Vcc	3.60	3.85	4.15	V
	Voltage detection level Vdet1_C ⁽²⁾	At the falling of Vcc	3.75	4.00	4.30	V
	Voltage detection level Vdet1_D (2)	At the falling of Vcc	3.90	4.15	4.45	V
	Voltage detection level Vdet1_E ⁽²⁾	At the falling of Vcc	4.05	4.30	4.60	V
	Voltage detection level Vdet1_F ⁽²⁾	At the falling of Vcc	4.20	4.45	4.75	V
-	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected	-	0.07	-	V
		Vdet1_6 to Vdet1_F selected	-	0.10	_	V
-	Voltage detection 1 circuit response time ⁽³⁾	At the falling of Vcc from 5 V to (Vdet1_0 – 0.1) V	-	60	150	μS
-	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	-	1.7	-	μΑ
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽⁴⁾		-	-	100	μS

Notes:

1. The measurement condition is Vcc = 1.8 V to 5.5 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version).

2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.

3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes Vdet1.

4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Sympol	Symbol Parameter Condition:		Conditions		ard	Unit	
Symbol	Paramete	ſ	Min.		Тур.	Max.	Unit
tsucyc	SSCK clock cycle tim	e		4	-	_	tCYC ⁽²⁾
tнı	SSCK clock "H" width			0.4	-	0.6	tsucyc
tlo	SSCK clock "L" width			0.4	-	0.6	tsucyc
trise	SSCK clock rising	Master		-	-	1	tCYC (2)
	time	Slave		-	-	1	μS
t FALL	SSCK clock falling	Master		-	-	1	tcyc ⁽²⁾
	time	Slave		-	-	1	μS
ts∪	SSO, SSI data input s	setup time		100	-	-	ns
tн	SSO, SSI data input h	nold time		1	-	-	tCYC ⁽²⁾
tlead	SCS setup time	Slave		1tcyc + 50	-	_	ns
tlag	SCS hold time	Slave		1tcyc + 50	-	-	ns
tod	SSO, SSI data output	delay time		-	-	1	tCYC (2)
tsa	SSI slave access time		$2.7~V \leq Vcc \leq 5.5~V$	-	_	1.5tcyc + 100	ns
			$1.8 \text{ V} \leq \text{Vcc} < 2.7 \text{ V}$	-	-	1.5tcyc + 200	ns
tOR	SSI slave out open tir	ne	$2.7~\text{V} \leq \text{Vcc} \leq 5.5~\text{V}$	-	-	1.5tcyc + 100	ns
				-	-	1.5tcyc + 200	ns

Table 5.16 Timing Requirements of Synchronous Serial Communication Unit (SSU)⁽¹⁾

Notes:

1. Vcc = 1.8 to 5.5 V, Vss = 0 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified. 2. 1tcyc = 1/f1(s)



Symbol	Deremeter	Condition	Sta		1.1	
Symbol	Parameter	Condition	Min.	Тур.	Max.	Unit
tSCL	SCL input cycle time		12tcyc + 600 (2)	-	-	ns
tSCLH	SCL input "H" width		3tcyc + 300 (2)	-	-	ns
tSCLL	SCL input "L" width		5tcyc + 500 (2)	-	-	ns
tsf	SCL, SDA input fall time		-	-	300	ns
tSP	SCL, SDA input spike pulse rejection time		-	-	1tcyc (2)	ns
tBUF	SDA input bus-free time		5tcyc (2)	-	-	ns
t STAH	Start condition input hold time		3tcyc (2)	_	-	ns
t STAS	Retransmit start condition input setup time		3tcyc (2)	_	-	ns
t STOP	Stop condition input setup time		3tcyc (2)	-	-	ns
tSDAS	Data input setup time		1tcyc + 40 (2)	-	-	ns
t SDAH	Data input hold time		10	-	-	ns

Timing Requirements of I²C bus Interface ⁽¹⁾ **Table 5.17**

Notes:

1. Vcc = 1.8 to 5.5 V, Vss = 0 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified. 2. 1tcvc = 1/f1(s)

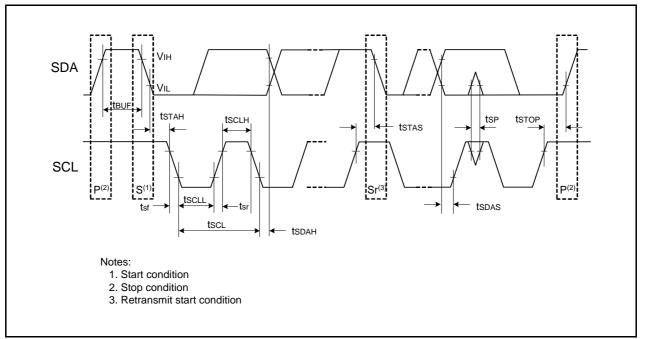






Table 5.22 Serial Interface

Symbol	Parameter		Star	Unit	
Symbol		Parameter			Unit
tc(CK)	CLKi input cycle time	When external clock is selected	200	-	ns
tw(CKH)	CLKi input "H" width		100	-	ns
tW(CKL)	CLKi input "L" width		100	-	ns
td(C-Q)	TXDi output delay time		-	90	ns
th(C-Q)	TXDi hold time		0	-	ns
tsu(D-C)	RXDi input setup time		10	-	ns
th(C-D)	RXDi input hold time		90	-	ns
td(C-Q)	TXDi output delay time	When internal clock is selected	-	10	ns
tsu(D-C)	RXDi input setup time		90	-	ns
th(C-D)	RXDi input hold time		90	-	ns

i = 0 to 2 Note:

1. Vcc = 5 V and Topr = -20 to 85 °C (N version)/-40 to 85 °C (D version), unless otherwise specified.

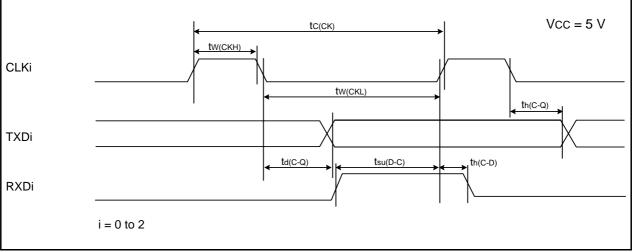


Figure 5.10 Serial Interface Timing Diagram when Vcc = 5 V

Table 5.23 External Interrupt INTi (i = 0, 1, 3) Input, Key Input Interrupt Kli (i = 0 to 3)

Svmbol	Parameter	Stan	Unit	
Symbol	Falanielei		Max.	Unit
tw(INH)	INTi input "H" width, Kli input "H" width	250 ⁽¹⁾	-	ns
tw(INL)	INTi input "L" width, Kli input "L" width	250 (2)	-	ns

Notes:

1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

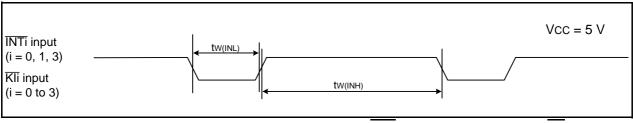


Figure 5.11 Input Timing Diagram for External Interrupt INTi and Key Input Interrupt Kli when Vcc = 5 V

Symbol	Dor	ameter	Conditi	<u></u>	S	tandard		Unit
Symbol	Par	Min. Typ.		Condition		Тур.	Max.	Unit
Vон	Output "H" voltage	Other than XOUT	Drive capacity High	Iон = -5 mA	Vcc - 0.5	-	Vcc	V
			Drive capacity Low	Іон = -1 mA	Vcc - 0.5	-	Vcc	V
		XOUT		Іон = -200 μА	1.0	-	Vcc	V
Vol	Output "L" voltage	Other than XOUT	Drive capacity High	IoL = 5 mA	-	-	0.5	V
			Drive capacity Low	IoL = 1 mA	_	-	0.5	V
		XOUT		IoL = 200 μA	-	-	0.5	V
VT+-VT-	Hysteresis	INTO, INT1, INT3, KIO, KI1, KI2, KI3, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, ADTRG, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO	Vcc = 3.0 V		0.1	0.4	_	V
		RESET	Vcc = 3.0 V		0.1	0.5	-	
Ін	Input "H" current		VI = 3 V, Vcc = 3.0 V		-	_	4.0	μA
lil	Input "L" current		VI = 0 V, Vcc = 3.0 V	/	_	-	-4.0	μA
Rpullup	Pull-up resistance		VI = 0 V, Vcc = 3.0 V	/	42	84	168	kΩ
Rfxin	Feedback resistance	XIN			-	0.3	-	MΩ
RfxCIN	Feedback resistance	XCIN			-	8	-	MΩ
Vram	RAM hold voltage		During stop mode		1.8	-	-	V

Table 5.24 Electrical Characteristics (3) [2.7 V \leq Vcc < 4.2 V]

Note:

1. 2.7 V \leq Vcc < 4.2 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.



Symbol	Parameter		Condition		Standar	d	Unit
Symbol	Parameter		Condition	Min.	Тур.	Max.	Unit
lcc	Power supply current (Vcc = 1.8 to 2.7 V) Single-chip mode, output pins are open,	High-speed clock mode	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	_	2.2	-	mA
	other pins are Vss		XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	0.8	_	mA
		High-speed on-chip oscillator	XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division	_	2.5	10	mA
		mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	1.7	-	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTIIC = MSTTRD = MSTTRC = 1	_	1	_	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	-	90	300	μA
	Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	-	80	350	μA	
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	-	40	_	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	15	90	μA
		XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	4	80	μA	
		XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	3.5	_	μA	
	Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	2.0	5	μA	
		XIN clock off, $T_{opr} = 85^{\circ}C$ High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	5.0	_	μA	



Timing requirements (Unless Otherwise Specified: Vcc = 2.2 V, Vss = 0 V at Topr = 25°C)

Table 5.32 External Clock Input (XOUT, XCIN)

Symbol	Parameter		Standard		
Symbol	Falanetei	Min. Max.		Unit	
tc(XOUT)	XOUT input cycle time	200	-	ns	
twh(xout)	XOUT input "H" width	90	-	ns	
twl(xout)	XOUT input "L" width	90	-	ns	
tc(XCIN)	XCIN input cycle time	14	-	μS	
tWH(XCIN)	XCIN input "H" width		-	μS	
twl(xcin)	XCIN input "L" width	7	-	μS	

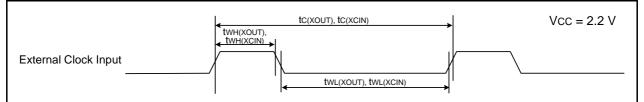


Figure 5.16 External Clock Input Timing Diagram when Vcc = 2.2 V

Table 5.33 TRAIO Input

Symbol	Parameter		Standard		
Symbol	Falameter	Min.	Max.	Unit	
tc(TRAIO)	TRAIO input cycle time	500	-	ns	
twh(traio)	TRAIO input "H" width	200	-	ns	
twl(traio)	TRAIO input "L" width	200	-	ns	

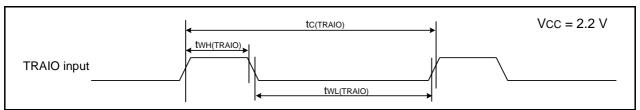


Figure 5.17 TRAIO Input Timing Diagram when Vcc = 2.2 V

REVISION HISTORY	R8C/33M Group Datasheet
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Rev.	Date		Description
Rev.	Dale	Page	Summary
0.10	Sep 28, 2010	-	First Edition issued
0.20	Feb 15, 2011	34	Table 5.11 revised, Note 2 added
		35	Table 5.13 and Table 5.14 revised
		41	Table 5.18 revised
		49	Table 5.30 revised
1.00	Jun 27, 2011	All pages	"Preliminary", "Under development" deleted
		4	Table 1.3 "(D): Under development" deleted
		27	Table 5.2 revised
		34	Table 5.11 revised
		35	Table 5.13 revised
		43	Table 5.20 revised
		44	Table 5.22 Note 1 added
		47	Table 5.26 revised
		48	Table 5.28 Note 1 added
		51	Table 5.32 revised
		52	Table 5.34 Note 1 added

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
- 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
 - In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do
 not access these addresses; the correct operation of LSI is not guaranteed if they are
 accessed.
- 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
- 5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

— The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.