



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	27
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.5К х 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21336mnfp-50

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1.5 Pin Functions

Tables 1.5 and 1.6 list Pin Functions.

Table 1.5Pin Functions (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	-	Apply 1.8 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power	AVCC, AVSS	-	Power supply for the A/D converter.
supply input			Connect a capacitor between AVCC and AVSS.
Reset input	RESET	I	Input "L" on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between
XIN clock output	XOUT	I/O	the XIN and XOUT pins ⁽¹⁾ . To use an external clock, input it to the XOUT pin and leave the XIN pin open.
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOUT
XCIN clock output	XCOUT	0	pins ⁽¹⁾ . To use an external clock, input it to the XCIN pin and leave the XCOUT pin open.
INT interrupt input	INTO, INT1, INT3	I	INT interrupt input pins. INT0 is timer RB, and RC input pin.
Key input interrupt	KI0 to KI3	I	Key input interrupt input pins
Timer RA TRAIO		I/O	Timer RA I/O pin
	TRAO	0	Timer RA output pin
Timer RB	TRBO	0	Timer RB output pin
Timer RC	TRCCLK	I	External clock input pin
	TRCTRG	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins
Timer RE	TREO	0	Divided clock output pin
Serial interface	CLK0, CLK1, CLK2	I/O	Transfer clock I/O pins
	RXD0, RXD1, RXD2	I	Serial data input pins
	TXD0, TXD1, TXD2	0	Serial data output pins
	CTS2	I	Transmission control input pin
	RTS2	0	Reception control output pin
	SCL2	I/O	I ² C mode clock I/O pin
	SDA2	I/O	I ² C mode data I/O pin
I ² C bus	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
SSU	SSI	I/O	Data I/O pin
	SCS	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin

I: Input O: Output I/O: Input and output

Note:

1. Refer to the oscillator manufacturer for oscillation characteristics.



2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

Address	Register	Symbol	After Reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h	LIN Control Register 2	LINCR2	00h
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0107h	Timer RB Control Register	TRBCR	00h
0108h	Timer RB One-Shot Control Register	TRBOCR	00h
	Timer RB I/O Control Register		00h
010Ah		TRBIOC	
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h	1		
0115h	1		
0116h	<u> </u>		
0117h	1		
0118h	Timer RE Second Data Register / Counter Data Register	TRESEC	00h
0119h	Timer RE Minute Data Register / Compare Data Register	TREMIN	00h
	Timer RE Hour Data Register	TREMIN	
011Ah	Timer RE Hour Data Register		00h
011Bh	Timer RE Day of Week Data Register	TREWK	00h
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0120h		TROORA	FFh
	Timer RC General Register B	TRCGRB	FFh
012Ah		IRCGRB	
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	0111111b
0133h	Timer RC Trigger Control Register	TRCADCR	00h
0134h			
0135h	<u> </u>		
	1		
()136h			
0136h 0137h			
0137h			
0137h 0138h			
0137h 0138h 0139h			
0137h 0138h 0139h 013Ah			
0137h 0138h 0139h 013Ah 013Bh			
0137h 0138h 0139h 013Ah 013Bh 013Ch			
0137h 0138h 0139h 013Ah 013Bh 013Ch 013Dh			
0137h 0138h 0139h 013Ah 013Bh 013Ch			

Table 4.5	SFR Informatior	1 (5) ⁽¹⁾
-----------	-----------------	----------------------

Note: 1. The blank areas are reserved and cannot be accessed by users.

			A.(
Address	Register	Symbol	After Reset
0180h	Timer RA Pin Select Register	TRASR	00h
0181h	Timer RB/RC Pin Select Register	TRBRCSR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h			
0185h			
0186h			
0187h			
0188h	UARTO Pin Select Register	U0SR	00h
0189h	UART1 Pin Select Register	U1SR	00h
	UART2 Pin Select Register 0	U2SR0	00h
018Ah	UARTZ PIN Select Register 0		
018Bh	UART2 Pin Select Register 1	U2SR1	00h
018Ch	SSU/IIC Pin Select Register	SSUIICSR	00h
018Dh			
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0193h	SS Transmit Data Register L / IIC bus Transmit Data Register ⁽²⁾	SSTDR / ICDRT	FFh
0195h	SS Transmit Data Register H (2)	SSTDRH	FFh
0196h	SS Receive Data Register L / IIC bus Receive Data Register (2)	SSRDR / ICDRR	FFh
0197h	SS Receive Data Register H (2)	SSRDRH	FFh
0198h	SS Control Register H / IIC bus Control Register 1 (2)	SSCRH / ICCR1	00h
0199h	SS Control Register L / IIC bus Control Register 2 ⁽²⁾	SSCRL / ICCR2	01111101b
		SSMR / ICMR	00010000b / 00011000b
019Ah	SS Mode Register / IIC bus Mode Register (2)		
019Bh	SS Enable Register / IIC bus Interrupt Enable Register ⁽²⁾	SSER / ICIER	00h
019Ch	SS Status Register / IIC bus Status Register (2)	SSSR / ICSR	00h / 0000X000b
019Dh	SS Mode Register 2 / Slave Address Register (2)	SSMR2 / SAR	00h
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			-
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B01 01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
			1
01BDh			
01BDh 01BEh 01BFh			

SFR Information (7)⁽¹⁾ Table 4.7

X: Undefined

Notes: 1. The blank areas are reserved and cannot be accessed by users. 2. Selectable by the IICSEL bit in the SSUIICSR register.



Table 4.8	SFR Information (8) ⁽¹⁾
-----------	------------------------------------

Address Register Symbol Attresset 01Cbh Address Match Interrupt Register 0 RMAD 0 XXh 01Cbh Address Match Interrupt Enable Register 0 AIER0 0000/XXXb 01Cbh Address Match Interrupt Enable Register 1 AIER1 00h 01Cbh Address Match Interrupt Enable Register 1 AIER1 0h 01Cbh Address Match Interrupt Enable Register 1 AIER1 0h 01Cbh Address Match Interrupt Enable Register 1 AIER1 0h 01Cbh Interrupt Enable Register 1 AIER1 Interrupt Enable Register 1 01Cbh Interrupt Enable Register 1 AIER1 Interrupt Enable Register 1 01Cbh Interrupt Enable Register 1 Interrupt Enable Register 1 Interrupt Enable Register 1 01Cbh Interrupt Enable Register 1 Interrupt Enable Register 1 Interrupt Enable Register 1	A -1.1		0	A4 D (
OTOTAL XN 000XXXXb 01C2h Address Match Interrupt Enable Register 0 AIERO 006 01C3h Address Match Interrupt Register 1 RMAD1 XXh 01C3h Address Match Interrupt Register 1 AIERO 000 01C3h Address Match Interrupt Enable Register 1 AIER1 00h 01C3h Address Match Interrupt Enable Register 1 AIER1 00h 01C3h Address Match Interrupt Enable Register 1 AIER1 00h 01C3h - - - - 01C3h - - - - - 01C3h - - - - - - 01C3h - <t< td=""><td></td><td></td><td></td><td></td></t<>				
0102h Adress Match Interrupt Enable Register 0 AER 0000XXXXb 0102h Address Match Interrupt Register 1 RMAD1 XXh 0102bn Address Match Interrupt Register 1 AIER1 000 0102bn Address Match Interrupt Enable Register 1 AIER1 000 0102bn Address Match Interrupt Enable Register 1 AIER1 000 0102bn Address Match Interrupt Enable Register 1 AIER1 000 0102bn Interrupt Enable Register 1 AIER1 000 0102bn Interrupt Enable Register 1 Interrupt Enable Register 1 Interrupt Enable Register 1 0102bn Interrupt Enable Register 1 Interrupt Enable Register 1 Interrupt Enable Register 1 Interrupt Enable Register 1 0102bn Interrupt Enable Register 1 Interrupt Enable R		Address Match Interrupt Register 0	RMAD0	
01C3h Address Match Interrupt Register 0 AIER0 Ohn 01C3h Address Match Interrupt Register 1 RMAD1 XXh 01C6h Address Match Interrupt Enable Register 1 AIER1 00h 01C6h AIdress Match Interrupt Enable Register 1 AIER1 00h 01C6h Image: Comparison of the second of				
OTCAh Address Match Interrupt Register 1 NAh XXh OTCSh 0000XXXXb 0000XXXb 0000XXXb OTCSh 01Ch Address Match Interrupt Enable Register 1 AIE1 00h OTCSh 0 0 0 0 0 OTCSh 0 0 0 0 0 OTCSh 0 0 0 0 0 OTCSh 0 0 0 0 0 0 OTCSh 0 </td <td></td> <td></td> <td></td> <td>0000XXXXb</td>				0000XXXXb
OTCSh XXh XXh OTCSh Address Match Interrupt Enable Register 1 AIER1 Oth OTCSh Address Match Interrupt Enable Register 1 AIER1 Oth OTCSh Image: Comparison of the second of the secon	01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
OTCSh XXh XXh OTCSh Address Match Interrupt Enable Register 1 AIER1 Oth OTCSh Address Match Interrupt Enable Register 1 AIER1 Oth OTCSh Image: Comparison of the second of the secon	01C4h		RMAD1	XXh
0102h Adress Match Interrupt Enable Register 1 AIR1 0000XXXXb 0102h Adress Match Interrupt Enable Register 1 AIR1 00h 0102h Adress Match Interrupt Enable Register 1 Image: Comparison of the compa				
01C7h Address Match Interrupt Enable Register 1 AIER1 00h 01C8h				
01C8h		Address Motoh Interrunt Englis Deviator 1		
0102h		Address Match Interrupt Enable Register 1	AIER1	UUN
01CAh				
01CBh				
01CCh	01CAh			
01CCh	01CBh			
01CDh				
01CEh				
01CFh				
OfDDn				
01D1h				
01D2h				
01D3h	01D1h			
01D3h	01D2h			
0104h			1	
0105h				
0106h				-
0107h				
0109h				
0109h				
01DAh				
01DAh	01D9h			
01DBh				
01DCh				
01DDh			-	
01DEh Pull-Up Control Register 0 PUR0 00h 01Eih Pull-Up Control Register 1 PUR1 00h 01E3h PUR1 00h 01E3h <				
01DFh Pull-Up Control Register 0 PUR0 00h 01E1h Pull-Up Control Register 1 00h 01E2h 00h 01E2h PUR1 00h 01E3h 00h 01E3h PUR1 00h 01E3h 00h 01E3h PUR1 00h 01E3h 01E3h 01E3h 01E3h PUR1 PUR1 01h 01E3h 00h 01F3h 00h 01F3h				
O1E0h PuIk-Up Control Register 0 PUR0 O0h 01E1h PuIk-Up Control Register 1 PUR1 O0h 01E3h 01E3h 01E3h 01E3h 01E4h				
01E1h Pull-Up Control Register 1 PUR1 00h 01E2h				
01E1h Pull-Up Control Register 1 PUR1 00h 01E2h 01E3h 01E3h 01E4h 01E6h	01E0h	Pull-Up Control Register 0	PUR0	00h
01E2h	01E1h		PUR1	00h
01E3h				
01E4h				
01E5h				
01E6h	01E4h			
01E7h				
01E8hImage: constraint of the second sec				
01E9h	01E7h			
01E9h	01E8h			
01EAhImage: constraint of the second sec				
01EBh01ECh01ECh01ECh				
01ECh				
01EDhImage: constraint of the second sec				
01EEhImage: constraint of the second sec				
01EFhPort P1 Drive Capacity Control RegisterP1DRR00h01F0hPort P2 Drive Capacity Control RegisterP2DRR00h01F2hDrive Capacity Control Register 0DRR000h01F3hDrive Capacity Control Register 1DRR100h01F5hInput Threshold Control Register 0VLT000h01F6hInput Threshold Control Register 1VLT000h01F6hInput Threshold Control Register 1VLT100h01F7h00h00h01F8h00h01F8hComparator B Control Register 0INTCMP00h01F8hComparator B Control Register 0INTEN00h01FAhExternal Input Enable Register 0INTEN00h01FChINT Input Filter Select Register 0INTF00h01FChINT Input Filter Select Register 0INTF00h01FChINT00h01FBh00h01FChINTNother00h01FChINT Input Filter Select Register 0INTF00h01FChINT00h00h00h01FChINTNother00h01FChKey Input Enable Register 0KIEN00h01FFhVV00h00h				
01F0hPort P1 Drive Capacity Control RegisterP1DRR00h01F1hPort P2 Drive Capacity Control Register 0DRR000h01F2hDrive Capacity Control Register 0DRR000h01F3hDrive Capacity Control Register 1DRR100h01F4h01F5hInput Threshold Control Register 0VLT000h01F6hInput Threshold Control Register 1VLT000h01F7h01F8hComparator B Control Register 0INTCMP00h01F8hComparator B Control Register 0INTEN00h01F8hComparator B Control Register 0INTF00h01F0hControl Register 0INTF00h01F0hControl Register 0INTF00h01F6hINT Input Filter Select Register 0INTF00h01F6hControl Register 0INTF00h01F6hKey Input Enable Register 0KIEN00h01F6hControl Register 0Control Register 0Control Register 001F6hControl Register 0Control Register 0				
01F0hPort P1 Drive Capacity Control RegisterP1DRR00h01F1hPort P2 Drive Capacity Control Register 0DRR000h01F2hDrive Capacity Control Register 0DRR000h01F3hDrive Capacity Control Register 1DRR100h01F4h01F5hInput Threshold Control Register 0VLT000h01F6hInput Threshold Control Register 1VLT000h01F7h01F8hComparator B Control Register 0INTCMP00h01F8hComparator B Control Register 0INTEN00h01F8hComparator B Control Register 0INTF00h01F0hControl Register 0INTF00h01F0hControl Register 0INTF00h01F6hINT Input Filter Select Register 0INTF00h01F6hControl Register 0INTF00h01F6hKey Input Enable Register 0KIEN00h01F6hControl Register 0Control Register 0Control Register 001F6hControl Register 0Control Register 0	01EFh			
01F1hPort P2 Drive Capacity Control RegisterP2DRR00h01F2hDrive Capacity Control Register 0DRR000h01F3hDrive Capacity Control Register 1DRR100h01F4h01F5hInput Threshold Control Register 0VLT000h01F6hInput Threshold Control Register 1VLT100h01F7h01F8hComparator B Control Register 0INTCMP00h01F9h01FAhExternal Input Enable Register 0INTEN00h01FBh01FChINT Input Filter Select Register 0INTF00h01FDh </td <td></td> <td>Port P1 Drive Capacity Control Register</td> <td>P1DRR</td> <td>00h</td>		Port P1 Drive Capacity Control Register	P1DRR	00h
01F2hDrive Capacity Control Register 0DRR000h01F3hDrive Capacity Control Register 1DRR100h01F4h01F5hInput Threshold Control Register 0VLT000h01F6hInput Threshold Control Register 1VLT100h01F7h01F8hComparator B Control Register 0INTCMP00h01F9h01F8hExternal Input Enable Register 0INTEN00h01F8h01F8hINT Input Filter Select Register 0INTF00h01FCh </td <td>01F1h</td> <td>Port P2 Drive Capacity Control Register</td> <td></td> <td></td>	01F1h	Port P2 Drive Capacity Control Register		
01F3h Drive Capacity Control Register 1 DRR1 00h 01F4h 01F5h Input Threshold Control Register 0 VLT0 00h 01F6h Input Threshold Control Register 1 VLT1 00h 01F7h 01F8h Comparator B Control Register 0 INTCMP 00h 01F9h 01F8h Comparator B Control Register 0 INTEM 00h 01F8h External Input Enable Register 0 INTEN 00h 01FBh 00h 00h 00h				
01F4h VLT0 00h 01F5h Input Threshold Control Register 0 VLT0 00h 01F6h Input Threshold Control Register 1 VLT1 00h 01F7h VLT1 00h 00h 01F8h Comparator B Control Register 0 INTCMP 00h 01F9h INTEN 00h 00h 01F8h External Input Enable Register 0 INTEN 00h 01F8h INT Input Filter Select Register 0 INTF 00h 01FCh INT Input Filter Select Register 0 INTF 00h 01FCh INT Input Filter Select Register 0 INTF 00h 01FEh Key Input Enable Register 0 KIEN 00h 01FFh				
01F5h Input Threshold Control Register 0 VLT0 00h 01F6h Input Threshold Control Register 1 VLT1 00h 01F7h 01F8h Comparator B Control Register 0 INTCMP 00h 01F9h 01FAh External Input Enable Register 0 INTEN 00h 01FBh 01FCh INT Input Filter Select Register 0 INTF 00h 01FDh 01FCh INT Input Filter Select Register 0 INTF 00h 01FDh 01FFh Key Input Enable Register 0 KIEN 00h		Drive Capacity Control Register 1	UKK1	UUN
01F6h Input Threshold Control Register 1 VLT1 00h 01F7h INTCMP 00h 01F8h Comparator B Control Register 0 INTCMP 00h 01F9h INTEN 00h 01FAh External Input Enable Register 0 INTEN 00h 01FBh INTFN 00h 01FCh INT Input Filter Select Register 0 INTF 00h 01FDh INTFN 00h 01FDh INTF 00h 01FEh Key Input Enable Register 0 KIEN 00h 01FFh VLT1 00h INTF INTF				
01F6h Input Threshold Control Register 1 VLT1 00h 01F7h INTCMP 00h 01F8h Comparator B Control Register 0 INTCMP 00h 01F9h INTEN 00h 01FAh External Input Enable Register 0 INTEN 00h 01FBh INTFN 00h 01FCh INT Input Filter Select Register 0 INTF 00h 01FDh INTFN 00h 01FDh INTF 00h 01FEh Key Input Enable Register 0 KIEN 00h 01FFh VLT1 00h INTF INTF			VLT0	00h
01F7h Image: Constraint of C		Input Threshold Control Register 1	VLT1	00h
01F8h Comparator B Control Register 0 INTCMP 00h 01F9h INTEN 00h 01FAh External Input Enable Register 0 INTEN 00h 01FBh INT Input Filter Select Register 0 INTF 00h 01FCh INT Input Filter Select Register 0 INTF 00h 01FDh INTF 00h 01FEh Key Input Enable Register 0 KIEN 00h 01FFh View Input Enable Register 0 Kien 00h		· · · · · · · · · · · · · · · · · · ·		
01F9h INTEN 00h 01FAh External Input Enable Register 0 INTEN 00h 01FBh INT Input Filter Select Register 0 INTF 00h 01FDh INTF 00h 01FEh Key Input Enable Register 0 KIEN 00h 01FFh Intersection of the select Register 0 Intersection of the select Register 0	01F8h	Comparator B Control Register 0	INTCMP	00h
01FAh External Input Enable Register 0 INTEN 00h 01FBh 01FCh INT Input Filter Select Register 0 INTF 00h 01FDh 01FDh 00h 00h 01FEh Key Input Enable Register 0 KIEN 00h 01FFh 00h 00h 00h				
01FBh 01FCh INT Input Filter Select Register 0 INTF 00h 01FDh 01FEh Key Input Enable Register 0 KIEN 00h 01FFh 01FFh 00h 00h 00h		Esternel Innut English Deviator (0.01
01FCh INT Input Filter Select Register 0 INTF 00h 01FDh 01FEh KIEN 00h 01FFh KIEN 00h		External input Enable Register U	INTEN	UUN
01FDh 01FEh 01FEh Key Input Enable Register 0 01FFh KIEN				
01FDh 01FEh 01FEh Key Input Enable Register 0 01FFh KIEN		INT Input Filter Select Register 0	INTF	00h
01FEh Key Input Enable Register 0 KIEN 00h 01FFh 00h				
01FFh	01FEh	Key Input Enable Register 0	KIEN	00h
	X: Undefined		1	

X: Undefined Note: 1. The blank areas are reserved and cannot be accessed by users.

Address	Register	Symbol	After Reset
2C00h	DTC Transfer Vector Area		XXh
2C01h	DTC Transfer Vector Area		XXh
2C02h	DTC Transfer Vector Area		XXh
2C03h	DTC Transfer Vector Area		XXh
2C04h	DTC Transfer Vector Area		XXh
2C05h	DTC Transfer Vector Area		XXh
2C06h	DTC Transfer Vector Area		XXh
2C07h	DTC Transfer Vector Area		XXh
2C08h	DTC Transfer Vector Area		XXh
2C09h	DTC Transfer Vector Area		XXh
2C0Ah	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
2C3Ah	DTC Transfer Vector Area		XXh
2C3Bh	DTC Transfer Vector Area		XXh
2C3Ch	DTC Transfer Vector Area		XXh
2C3Dh	DTC Transfer Vector Area		XXh
2C3Eh	DTC Transfer Vector Area		XXh
2C3Fh	DTC Transfer Vector Area	DTODO	XXh
2C40h	DTC Control Data 0	DTCD0	XXh
2C41h	4		XXh
2C42h 2C43h	4		XXh XXh
2C43h 2C44h	4		XXh
2C4411 2C45h	4		XXh
2C45h	4		XXh
2C4011 2C47h	4		XXh
2C48h	DTC Control Data 1	DTCD1	XXh
2C49h		ысы	XXh
2C43h	-		XXh
2C4Bh	4		XXh
2C4Ch	4		XXh
2C4Dh	4		XXh
2C4Eh	4		XXh
2C4Fh	4		XXh
2C50h	DTC Control Data 2	DTCD2	XXh
2C51h		-	XXh
2C52h	1		XXh
2C53h	1		XXh
2C54h	1		XXh
2C55h			XXh
2C56h			XXh
2C57h	1		XXh
2C58h	DTC Control Data 3	DTCD3	XXh
2C59h			XXh
2C5Ah			XXh
2C5Bh			XXh
2C5Ch			XXh
2C5Dh			XXh
2C5Eh]		XXh
2C5Fh]		XXh
2C60h	DTC Control Data 4	DTCD4	XXh
2C61h]		XXh
2C62h]		XXh
2C63h]		XXh
2C64h			XXh
2C65h			XXh
2C66h			XXh
2C67h			XXh
2C68h	DTC Control Data 5	DTCD5	XXh
2C69h]		XXh
2C6Ah]		XXh
2C6Bh]		XXh
2C6Ch]		XXh
2C6Dh]		XXh
2C6Eh]		XXh
			XXh

SFR Information (9)⁽¹⁾ Table 4.9

X: Undefined Note: 1. The blank areas are reserved and cannot be accessed by users.

2270h DTC Control Data 6 DTC Source Data 6 XNn 2277h XNn XNn 2277h XNn XNn 277h XNn XNn	Address	Register	Symbol	After Reset
2271h Xh 2272h Xh 2273h Xh 2274h Xh 2274h Xh 2274h Xh 2274h Xh 2277h Xh 227h DTC Control Data 7 227h Xh 228h DTC Control Data 8 228h DTC Control Data 9 228h DTC Control Data 10 228h DTC Control Data 10				
2272h Xh 2273h Xh 2273h Xh 2273h Xh 2275h Xh 2275h Xh 277b				
2273h Xh 2274h Xh 2277h Xh 2277h Xh 2277h Xh 2277h DTC Control Data 7 Xh 2277h Xh Xh 2267h Xh Xh 2268h DTC Control Data 8 DTCD8 Xh 2268h ZCRh Xh Xh 2268h ZCRh Xh Xh 2268h ZCRh Xh Xh 2268h ZCRh Xh Xh 2268h DTC Control Data 10 DTCD10 Xh 2268h ZCRh Xh		4		
2273h Xh 2275h Xh 2277h DTC control Data 7 277b DTC control Data 7 277b DTC control Data 7 277b Xh 277b <t< td=""><td></td><td>4</td><td></td><td></td></t<>		4		
2278h Xh 2277h Xh 2267h Yh 2268h Xh 2268h Xh <td></td> <td>4</td> <td></td> <td></td>		4		
2C7/h XXh 2C8/h XXh 2C8/h </td <td></td> <td>4</td> <td></td> <td></td>		4		
2C77h Xh 2C78h DTC Control Data 7 2C78h XKh 2C78h XKh 2C78h XKh 2C78h XKh 2C7Rh XKh 2C7Rh XKh 2C7bh XKh 2C8bh DTC Control Data 8 2C8bh XXh		4		
2C78h DTC Control Data 7 XXh 2C79h XXh XXh 2C77h XXh XXh 2C77h XXh XXh 2C77h XXh XXh 2C7bh XXh XXh 2C7bh XXh XXh 2C7bh XXh XXh 2C7bh XXh XXh 2C68h XXh XXh 2C8h XXh XXh 2C8h </td <td></td> <td>4</td> <td></td> <td></td>		4		
2C79h XXh 2C7Ah XXh 2C7Bh XXh 2C7Ch XXh 2C7Ch XXh 2C7Fh XXh 2C60h DTC Control Data 8 2C62h XXh		DTO Original Data 7	DTOD7	
2C7Ah Xxh 2C7Bh Xxh 2C7Ch Xxh 2C7Dh Xxh 2C7Dh Xxh 2C7Dh Xxh 2C7Dh Xxh 2C7Dh Xxh 2C7Ph Xxh 2C81h Xxh 2C84h Xxh 2C87h Xxh 2C87h </td <td></td> <td>DIC Control Data 7</td> <td>DICD7</td> <td></td>		DIC Control Data 7	DICD7	
2C7Rh Xh 2C7Ch Xh 2C8h Xh 2C		4		
2C7Ch Xin 2C7Dh Xin 2C7Fh Xin 2C7Fh Xin 2C7Fh Xin 2C87h Xin 2C87h Xin 2C88h Xin 2C88h </td <td></td> <td></td> <td></td> <td></td>				
2C7Dh Xh 2C7Fh Xh 2C80h DTC Control Data 8 2C81h Xh 2C85h Xh 2C85h Xh 2C85h Xh 2C86h Xh 2C87h Xh 2C88h				
2C7Eh Xh 2C7Fh Xh 2C7Fh Xh 2C8h DTC Control Data 8 2C8h Xh 2C8h TC Control Data 9 2C8h DTC Control Data 9 2C8h TC Control Data 9 2C8h TC Control Data 9 2C8h DTC Control Data 9 2C8h Xh 2C9h Xh 2C9h Xh 2C9h Xh 2C3h Xh 2C3h Xh 2C3h Xh </td <td></td> <td></td> <td></td> <td></td>				
2C7Fh Xh 2C80h DTC Control Data 8 Xh 2C81h DTC Control Data 8 Xh 2C81h Xh Xh 2C81h Cash Xh 2C81h Control Data 9 Xh 2C81h DTC Control Data 9 Xh 2C81h DTC Control Data 10 DTCD9 Xh 2C82h Xh Xh Xh 2C82h Xh Xh Xh 2C82h TC Control Data 10 DTCD10 Xh 2C82h Xh Xh Xh 2C82h TC Control Data 10 TC Control Data 10 Xh 2C82h Xh Xh Xh 2C82h Xh Xh Xh 2C82h Xh Xh Xh <				
12 C30h 2 C3h 2 C3h				
2281h Xh 2C32h Xh 2C33h Xh 2C34h Xh 2C35h Xh 2C36h TC Control Data 9 2C38h DTC Control Data 9 2C38h Xh 2C38h TC Control Data 9 2C38h DTC Control Data 9 2C38h Xh 2C38h TC Control Data 10 2C39h TC Control Data 11 2C39h TC Control Data 12 2C4Ah TXh 2C39h TC Control Data 12 2C4Ah TXh				
2C82h Xxh Xxh 2C83h Xxh Xxh 2C83h Xxh Xxh 2C88h DTC Control Data 9 Xxh 2C88h DTC Control Data 9 Xxh 2C88h Xxh Xxh 2C89h Xxh Xxh 2C99h Xxh Xxh <td></td> <td>DTC Control Data 8</td> <td>DTCD8</td> <td></td>		DTC Control Data 8	DTCD8	
2/283h 2/264h Xxh 2/268h Xxh Xxh 2/269h Xxh Xxh	2C81h			XXh
2/283h 2/264h Xxh 2/268h Xxh Xxh 2/269h Xxh Xxh	2C82h]		
2C84h Xxh Xxh 2C85h Xxh Xxh 2C88h DTC Control Data 9 Xxh 2C88h DTC Control Data 9 Xxh 2C88h Xxh Xxh 2C99h DTC Control Data 10 DTCD10 Xxh 2C99h Xxh Xxh Xxh	2C83h]		XXh
20285h 20287h 20288h 20289h 20289h 20289h 20289h 20289h 20289h 20289h 20289h 20289h 20289h 20289h 20289h 20289h 20289h 20289h 20297h 20297h 20297h 20299h 20209h 20299h 20299h 2020000000000	2C84h	1		
2088h Xxh 2087h Xxh 2088h DTC Control Data 9 Xxh 2088h DTC Control Data 9 Xxh 2088h Xxh Xxh 2088h TC Control Data 10 DTCD10 Xxh 2099h DTC Control Data 10 Xxh Xxh 2099h Z099h Xxh Xxh 2099h Z099h Xxh Xxh 2099h DTC Control Data 11 Xxh Xxh 2099h Z099h Xxh Xxh 2099h DTC Control Data 11 Xxh Xxh 2099h Xxh Xxh Xxh 2099h DTC Control Data 12 Xxh Xxh		1		
2287h Xh 2288h DTC Control Data 9 Xh 2288h DTC Control Data 9 Xh 2288h Xh Xh 2088h Xh Xh 2088h Xh Xh 2088h Xh Xh 2089h Xh Xh 2089h Xh Xh 2089h TC Control Data 10 Xh 2089h DTC Control Data 10 Xh 2099h DTC Control Data 10 Xh 2099h ZCGah Xh 2099h DTC Control Data 10 Xh 2099h ZCGah Xh 2099h DTC Control Data 11 Xh 2099h DTC Control Data 11 Xh 2099h ZCGah Xh 2099h DTC Control Data 11 Xh 2099h ZCGah Xh 2099h DTC Control Data 11 Xh 2099h ZCGAh Xh 2099h ZCGAh Xh		1		
2288h DTC Control Data 9 Xh 2C88h Xh Xh 2C88h DTC Control Data 10 DTCD10 Xh 2C93h Xh Xh Xh 2C93h DTC Control Data 11 DTCD11 Xh 2C98h DTC Control Data 11 Xh Xh 2C98h DTC Control Data 12 Xh Xh 2C97h Xh Xh Xh 2C40h Xh Xh Xh		1		
20289h Xxh 20284h Xxh 20284h Xxh 2028bh Xxh 2028bh Xxh 2028bh Xxh 2028bh Xxh 2028bh Xxh 2028bh DTC Control Data 10 2029th DTC Control Data 10 2029th Xxh 2029th Xxh 2039h ZCGayh 2039h DTC Control Data 10 2039h DTC Control Data 10 2039h ZCGayh 2039h ZCGayh 2039h DTC Control Data 11 2039h DTC Control Data 11 2039h ZCGayh 2039h ZCGayh 2039h DTC Control Data 11 2039h ZCGayh 2039h ZCGayh 2039h ZCGayh 2030h ZCArth 2030h ZCArth 2040h ZC Control Data 12 2040h ZCArth 2040h Z		DTC Control Data 9	DTCD9	
228Ah Xxh 228Bh Xxh 229th Xxh 2293h Xxh 2298h DTC Control Data 11 Xxh 2299h DTC Control Data 11 Xxh 229gh Xxh Xxh 220gh		4		
2268h Xxh 2268bh Xxh 2268bh Xxh 2268bh Xxh 2268bh Xxh 2268bh Xxh 2269th DTC Control Data 10 2269th Xxh 2269th Xxh 2269th Xxh 2269th Xxh 229th Xxh 220th Xxh 220th Xxh 220th Xxh		4		
2280h Xxh 2282h Xxh 2282h Xxh 2289h Xxh 2291h Xxh 2293h Xxh 2294h Xxh 2295h Xxh 2295h Xxh 2295h Xxh 2205h Xxh 2205h Xxh 2205h Xxh 2205h Xxh 2205h </td <td></td> <td>4</td> <td></td> <td></td>		4		
2280h Xh Xh 228Fh Xh Xh 2209h DTC Control Data 10 Xh Xh 2291h Xh Xh Xh 2093h ZC93h Xh Xh 2093h Xh Xh Xh 2093h DTC Control Data 11 DTCD11 Xh 2093h Xh Xh Xh 2093h Xh Xh Xh 2093h DTC Control Data 11 DTCD11 Xh 2093h Xh Xh Xh 2093h Xh Xh Xh 2093h Xh Xh Xh 2004h Xh Xh		4		
2C8Eh Xxh 2C9Bh Xxh 2C90h DTC Control Data 10 Xxh 2C93h Xxh 2C96h Xxh 2C98h DTC Control Data 11 2C98h DTC Control Data 11 2C98h DTC Control Data 11 2C98h ZC98h 2C98h DTC Control Data 11 2C98h Xxh 2C98h Xxh 2C98h ZC98h 2C98h DTC Control Data 11 2C98h DTC Control Data 12 ZCA0h Xxh 2C98h Xxh 2C40h Xxh 2C40h Xxh 2CA3h Xxh 2CA3h Xxh 2CA4h Xxh 2CA8h DTC Control Data 13		4		
2C8Fh Xxh 2C90h DTC Control Data 10 DTCD10 XXh 2C92h XXh XXh XXh 2C93h Xxh XXh XXh 2C93h XXh XXh XXh 2C93h XXh XXh XXh 2C93h XXh XXh XXh 2C95h XXh XXh XXh 2C97h DTC Control Data 11 DTCD11 XXh 2C98h DTC Control Data 11 XXh XXh 2C98h DTC Control Data 11 XXh XXh 2C97h XXh XXh XXh 2C98h DTC Control Data 11 XXh XXh 2C97h XXh XXh XXh 2C97h XXh XXh XXh 2C97h ZC4h XXh XXh 2C97h ZC4h XXh XXh 2C42h XXh XXh XXh 2CA2h XXh XXh XXh		4		
2030h DTC Control Data 10 XXh 2031h Z032h XXh 2033h Z033h XXh 2036h Z036h XXh 2036h Z036h XXh 2037h XXh XXh 2038h DTC Control Data 11 DTCD10 XXh 2039h DTC Control Data 11 XXh XXh 2039h Z03Ph XXh XXh 2039h Z03Ph XXh XXh 2039h Z03Ph XXh XXh 2039h Z03Ph XXh XXh 2030h XXh XXh XXh 2031h ZCAth XXh XXh 2031h ZCAth XXh XXh 2032h ZCAth XXh XXh 2032h ZCAth		4		
2C31h XXh 2C33h XXh 2C34h XXh 2C35h XXh 2C36h XXh 2C39h XXh 2C39h XXh 2C39h XXh 2C39h DTC Control Data 11 2C39h DTC Control Data 11 2C39h XXh 2C4h XXh 2CAh XXh 2CAh XXh 2CAth XXh 2CAth XXh		DTC Control Data 10	DTCD10	
2C32h XXh 2C33h XXh 2C35h XXh 2C36h XXh 2C39h XXh 2C39h DTC Control Data 11 XXh 2C39h DTC Control Data 11 XXh 2C39h DTC Control Data 11 XXh 2C39h XXh XXh 2C4h XXh XXh 2CAh XXh XXh 2CAh XXh XXh 2CAh XXh XXh <		DIC Control Data 10	DICDIO	
2C93h Xh 2C93h Xh 2C96h Xh 2C97h Xh 2C98h DTC Control Data 11 2C99h Xh 2C4Ah Xh 2CAh Xh 2CAAh Xh		4		
2C94h XXh 2C95h XXh 2C97h XXh 2C97h XXh 2C97h XXh 2C98h DTC Control Data 11 XXh 2C99h XXh 2C9Fh XXh 2C9Fh XXh 2C4Ah DTC Control Data 12 2CA0h DTC Control Data 12 2CA3h XXh 2CA3h XXh 2CA3h XXh 2CA6h XXh 2CA8h DTC Control Data 13 2CA9h ZXAh 2CA2h XXh 2CA2h XXh 2CA2h XXh 2CA8h DTC Control Data 13 2CA9h ZXAh 2CA2h XXh 2CA2h XXh <td></td> <td>4</td> <td></td> <td></td>		4		
2C95h XXh 2C97h XXh 2C98h DTC Control Data 11 XXh 2C98h DTC Control Data 11 XXh 2C99h XXh XXh 2C99h XXh XXh 2C99h XXh XXh 2C99ch XXh XXh 2C99ch XXh XXh 2C99ch XXh XXh 2C99ch XXh XXh 2C9Fh XXh XXh 2C9Fh DTC Control Data 12 DTCD12 XXh 2CA0h DTC Control Data 12 DTCD12 XXh 2CA2h XXh XXh XXh 2CA2h XXh XXh XXh 2CA3h XXh XXh XXh 2CA6h XXh XXh XXh 2CA6h XXh XXh XXh 2CA6h DTC Control Data 13 DTC D13 XXh 2CA2h XAh XXh XXh 2CA2h		4		
2C96h Xxh 2C97h Xxh 2C99h DTC Control Data 11 Xxh 2C99h Xxh Xxh 2C99h Xxh Xxh 2C99h Xxh Xxh 2C98h DTC Control Data 12 Xxh 2CA0h DTC Control Data 12 Xxh 2CA3h Xxh Xxh 2CA3h Xxh Xxh 2CA3h Xxh Xxh 2CA3h Xxh Xxh 2CA6h Xxh Xxh 2CA8h DTC Control Data 13 DTCD13 Xxh 2CA8h Xxh Xxh Xxh 2CA8h Xxh Xxh Xxh 2CA		4		
2C97h XXh 2C98h DTC Control Data 11 XXh 2C99h XXh XXh 2C99h XXh XXh 2C98h DTC Control Data 12 XXh 2C97h DTC Control Data 12 XXh 2CA1h ZCA2h XXh 2CA2h XXh XXh 2CA3h DTC Control Data 13 XXh 2CA3h XXh XX				
2C98h DTC Control Data 11 XXh 2C99h XXh XXh 2C98h XXh XXh 2C98h XXh XXh 2C98h XXh XXh 2C98h XXh XXh 2C99h XXh XXh 2C99h XXh XXh 2C99h XXh XXh 2C99h DTC Control Data 12 Xh 2CA0h DTC Control Data 12 XXh 2CA1h XXh XXh 2CA2h XXh XXh 2CA2h XXh XXh 2CA3h XXh XXh 2CA4h XXh XXh 2CA6h XXh XXh 2CA8h DTC Control Data 13 DTCD13 Xxh 2CA9h XXh XXh XXh 2CA9h XXh XXh XXh 2CA8h DTC Control Data 13 XXh XXh 2CA9h XXh XXh XXh				
2C99h XXh 2C9Bh XXh 2C9Bh XXh 2C9Bh XXh 2C9Bh XXh 2C9Dh XXh 2C9Fh XXh 2C9Fh XXh 2C9Fh XXh 2C9Fh XXh 2C9Fh XXh 2CA0h DTC Control Data 12 2CA1h XXh 2CA2h XXh 2CA2h XXh 2CA2h XXh 2CA3h XXh 2CA4h XXh 2CA4h XXh 2CA4h XXh 2CA6h XXh 2CA6h XXh 2CA6h XXh 2CA8h DTC Control Data 13 2CA8h DTC Control Data 13 2CA9h XXh 2CA8h XXh 2CA8h XXh 2CA8h XXh 2CA8h XXh 2CA8h XXh 2CA8h <td< td=""><td></td><td></td><td></td><td></td></td<>				
2C9Ah XXh 2C9Bh XXh 2C9Dh XXh 2C9Eh XXh 2C9Fh XXh 2C40h XXh 2CA0h DTC Control Data 12 2CA1h DTC Control Data 12 2CA2h XXh 2CA3h XXh 2CA4h XXh 2CA3h XXh 2CA4h XXh 2CA5h XXh 2CA6h XXh 2CA3h XXh 2CA4h XXh 2CA5h XXh 2CA6h XXh 2CA7h XXh 2CA8h DTC Control Data 13 2CA8h DTC Control Data 13 2CA8h XXh 2CA9h XXh 2CA8h XXh 2CA8h<		DTC Control Data 11	DTCD11	
2C9Bh XXh 2C9Ch XXh 2C9Eh XXh 2C9Fh XXh 2C9Fh XXh 2C9Fh XXh 2C9Fh DTC Control Data 12 2CA0h DTC D12 XXh 2CA1h XXh XXh 2CA2h XXh XXh 2CA3h XXh XXh 2CA7h DTC Control Data 13 XXh 2CA8h XXh XXh 2CA9h XXh XXh 2CA9h XXh XXh 2CA8h XXh XXh 2CA8h XXh XXh 2CA8h XXh				
2C9Ch XXh 2C9Bh XXh 2C9Fh XXh 2CA0h DTC Control Data 12 XXh 2CA1h XXh 2CA2h XXh 2CA3h XXh 2CA3h XXh 2CA4h XXh 2CA4h XXh 2CA3h XXh 2CA3h XXh 2CA4h XXh 2CA3h XXh 2CA4h XXh 2CA3h XXh 2CA4h XXh 2CA3h XXh 2CA4h XXh 2CA6h XXh 2CA6h XXh 2CA6h XXh 2CA8h DTC Control Data 13 2CA9h DTCD13 XXh 2CA9h XXh 2CA9h XXh 2CA9h XXh 2CA8h XXh 2CA8h XXh 2CA9h XXh 2CA9h XXh				
ZC9DhXXh2C9FhXXh2CA0hDTC Control Data 122CA1hDTC Control Data 122CA1hXXh2CA2hXXh2CA3hXXh2CA3hXXh2CA4hXXh2CA4hXXh2CA4hXXh2CA4hXXh2CA4hXXh2CA4hXXh2CA4hXXh2CA4hXXh2CA6hXXh2CA7hXXh2CA8hDTC Control Data 132CA9hZCA4h2CA4hXXh2CA4hXXh2CA4hXXh2CA4hXXh2CA4hXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh				
ZC9EhXXh2C3FhDTC Control Data 12DTCD12XXh2CA0hDTC Control Data 12DTCD12XXh2CA2hZCA3hXXhXXh2CA3hZCA4hXXhXXh2CA4hZCA4hXXhXXh2CA4hZCA5hXXhXXh2CA4hZCA6hXXhXXh2CA6hZCA7hXXhXXh2CA8hDTC Control Data 13DTC Control Data 13DTCD13XXh2CA8hZCA9hXXhXXh2CA8hZCAAhXXhXXh2CA8hZCAAhXXhXXh2CAAhZCAAhXXhXXh2CAAhZCAAhXXhXXh2CAAhZCAAhXXhXXh2CAAhZCAAhXXhXXh2CAAhZCAAhXXhXXh2CAAhZCAAHXXhXXh2CAAhZCAAHXXhXXh2CAAhZCAAHXXhXXh2CAAHZCAAHXXhXXh2CAAHXXhXXhXXh2CAAHXXhXXhXXh2CAAHXXhXXhXXh2CAAHXXhXXhXXh2CAAHXXhXXhXXh2CAAHXXhXXhXXh2CAAHXXhXXhXXh2CAAHXXhXXhXXh2CAAHXXhXXhXXh2CAAHXXhXXhXXH2CAAHXXHXXHXXH <td>2C9Ch</td> <td>]</td> <td></td> <td></td>	2C9Ch]		
2C9FhXXh2CA0hDTC Control Data 12DTCD12XXh2CA1hXXhXXh2CA2hXXhXXh2CA3hXXhXXh2CA4hXXhXXh2CA4hXXhXXh2CA5hXXhXXh2CA6hXXhXXh2CA8hDTC Control Data 13XXh2CA8hDTC Control Data 13DTCD13XXh2CA8hZCA9hXXhXXh2CA8hZCA8hXXhXXh2CA8hZCAAhXXhXXh2CA8hZCAAhXXhXXh2CAAhZCAAhXXhXXh2CAAhZCAChXXhXXh2CAChXXhXXhXXh2CAAhZCAAhXXhXXh2CAAhZCAAhXXhXXh2CAAhXXhXXhXXh2CAAhXXhXXhXXh2CAFhXXhXXhXXh	2C9Dh]		
2C9FhXXh2CA0hDTC Control Data 12DTCD12XXh2CA1hXXhXXh2CA2hXXhXXh2CA3hXXhXXh2CA4hXXhXXh2CA4hXXhXXh2CA5hXXhXXh2CA6hXXhXXh2CA8hDTC Control Data 13XXh2CA8hDTC Control Data 13DTCD13XXh2CA8hZCA9hXXhXXh2CA8hZCA8hXXhXXh2CA8hZCAAhXXhXXh2CA8hZCAAhXXhXXh2CAAhZCAAhXXhXXh2CAAhZCAChXXhXXh2CAChXXhXXhXXh2CAAhZCAAhXXhXXh2CAAhZCAAhXXhXXh2CAAhXXhXXhXXh2CAAhXXhXXhXXh2CAFhXXhXXhXXh]		XXh
2CA0h 2CA1h 2CA2h 2CA3h 2CA3h 2CA4h 2CA4h 2CA4h 2CA5h 2CA6h 2CA6h 2CA7hDTC Control Data 12XXh <br< td=""><td></td><td>1</td><td></td><td></td></br<>		1		
2CA1h XXh 2CA2h XXh 2CA3h XXh 2CA4h XXh 2CA4h XXh 2CA4h XXh 2CA5h XXh 2CA6h XXh 2CA7h XXh 2CA7h XXh 2CA7h XXh 2CA7h XXh 2CA7h XXh 2CA7h XXh 2CA8h DTC Control Data 13 2CA9h XXh 2CA8h XXh		DTC Control Data 12	DTCD12	XXh
2CA2h XXh 2CA3h XXh 2CA4h XXh 2CA5h XXh 2CA6h XXh 2CA7h XXh 2CA8h XXh 2CA8h XXh 2CA7h XXh 2CA8h DTC Control Data 13 2CA9h ZCA9h 2CA8h XXh		1		
2CA3hXXh2CA4hXXh2CA5hXXh2CA6hXXh2CA7hXXh2CA8hDTC Control Data 132CA9hXXh2CA4hXXh2CA9hXXh2CA4hXXh2CA8hDTC D132CA8hXXh2CA9hXXh2CA8hXXh2CA8hXXh2CA8hXXh2CA8hXXh2CA8hXXh2CA2hXXh2CAChXXh2CA2hXXh2CA2hXXh2CA2hXXh2CAFhXXh		1		
2CA4h XXh 2CA5h XXh 2CA6h XXh 2CA7h XXh 2CA8h DTC Control Data 13 2CA9h XXh 2CA8h DTC Control Data 13 2CA8h DTCD13 2CA8h XXh 2CA9h XXh 2CA9h XXh 2CA8h XXh 2CA8h XXh 2CA8h XXh 2CAAh XXh 2CAFh XXh		1		
ZCA5hXXh2CA6hXXh2CA7hXXh2CA7hXXh2CA8hDTC Control Data 132CA9hXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAAhXXh2CAFhXXh		1		XXh
2CA6h XXh 2CA7h XXh 2CA8h DTC Control Data 13 2CA9h ZCA9h 2CAAh XXh 2CACh XXh 2CAAh XXh 2CAAh XXh 2CAAh XXh 2CAAh XXh		1		
2CA7hXXh2CA8hDTC Control Data 13DTCD132CA9hXXh2CAAhXXh2CAAhXXh2CAChXXh2CAChXXh2CAChXXh2CAEhXXh2CAFhXXh		1		
2CA8h 2CA9h 2CAAhDTC Control Data 13DTCD13XXh XXh2CAAh 2CABhZCACh 2CAChXXhXXh2CADh 2CAEhXXhXXh2CAFhXXhXXh		1		
2CA9hXXh2CAAhXXh2CABhXXh2CAChXXh2CADhXXh2CAEhXXh2CAFhXXh		DTC Control Data 13		
2CAAhXXh2CABhXXh2CAChXXh2CADhXXh2CAEhXXh2CAFhXXh			010013	
2CABhXXh2CAChXXh2CADhXXh2CAEhXXh2CAFhXXh		4		
2CACh XXh 2CADh XXh 2CAEh XXh 2CAFh XXh		4		
2CADh XXh 2CAEh XXh 2CAFh XXh	2CABN	4		
2CAEh XXh 2CAFh XXh		4		
2CAFh XXh		4		
		4		
	2CAFh			XXN

X: Undefined Note: 1. The blank areas are reserved and cannot be accessed by users.

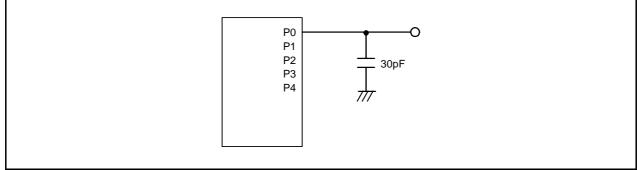


Figure 5.1 Ports P0 to P4 Timing Measurement Circuit



C: make al	Parameter	Conditions	Standard			Linit
Symbol		Conditions	Min.	Тур.	Max.	Unit
_	Program/erase endurance (2)		1,000 (3)	-	-	times
_	Byte program time		-	80	500	μs
-	Block erase time		-	0.3	-	s
td(SR-SUS)	Time delay from suspend request until suspend		-	-	5+CPU clock × 3 cycles	ms
_	Interval from erase start/restart until following suspend request		0	-	_	μS
-	Time from suspend until erase restart		-	-	30+CPU clock × 1 cycle	μS
td(CMDRST- READY)	Time from when command is forcibly terminated until reading is enabled		-	-	30+CPU clock × 1 cycle	μS
-	Program, erase voltage		2.7	-	5.5	V
-	Read voltage		1.8	_	5.5	V
-	Program, erase temperature		0	_	60	°C
-	Data hold time ⁽⁷⁾	Ambient temperature = 55°C	20	-	-	year

Table 5.7 Flash Memory (Program ROM) Electrical Characteristics

Notes:

1. Vcc = 2.7 to 5.5 V and $T_{opr} = 0$ to 60°C, unless otherwise specified.

2. Definition of programming/erasure endurance

The programming and erasure endurance is defined on a per-block basis. If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.

However, the same address must not be programmed more than once per erase operation (overwriting prohibited).

3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).

4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.

5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.

6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.

7. The data hold time includes time that the power supply is off or the clock is not supplied.



Sumbol	Parameter	Condition	Standard			Unit
Symbol	Faranteler	Condition	Min.	Тур.	Max.	Unit
Vdet2	Voltage detection level Vdet2_0 ⁽²⁾	At the falling of Vcc	3.70	4.00	4.30	V
	Voltage detection level Vdet2_EXT (2)	At the falling of LVCMP2	1.20	1.34	1.48	V
-	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		-	0.10	-	V
-	Voltage detection 2 circuit response time ⁽³⁾	At the falling of Vcc from $5 \text{ V to } (\text{Vdet2}_0 - 0.1) \text{ V}$	-	20	150	μS
-	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	-	1.7	-	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽⁴⁾		-	-	100	μS

Table 5.11 Voltage Detection 2 Circuit Electrical Characteristics

Notes:

- 1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = -20 to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version).
- 2. The voltage detection level varies with detection targets. Select the level with the VCA24 bit in the VCA2 register.
- 3. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.

4. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

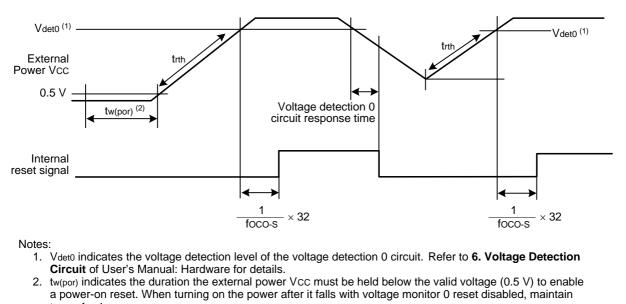
Table 5.12 Power-on Reset Circuit ⁽²⁾

Symbol	Parameter	Condition		Unit		
	Falameter	Condition	Min.	Тур.	Max.	Unit
trth	External power Vcc rise gradient	(1)	0	Ì	50,000	mV/ms

Notes:

1. The measurement condition is $T_{opr} = -20$ to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version), unless otherwise specified.

2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



tw(por) for 1 ms or more.

Figure 5.3 Power-on Reset Circuit Electrical Characteristics

Symbol	Parameter	Condition		Standard		Unit
Symbol	Parameter	Condition	Min.	Тур.	Max.	Unit
_	High-speed on-chip oscillator frequency after reset	Vcc = 1.8 V to 5.5 V −20°C ≤ Topr ≤ 85°C	39.4	40	40.6	MHz
		Vcc = 1.8 V to 5.5 V -40°C ≤ Topr ≤ 85°C	39.4	40	40.6	MHz
		Vcc = 1.8 V to 5.5 V Topr =25°C	39.6	40	40.4	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into	Vcc = 1.8 V to 5.5 V −20°C ≤ Topr ≤ 85°C	36.311	36.864	37.417	MHz
	the FRA1 register and the FRA5 register correction value into the FRA3 register ⁽²⁾	Vcc = 1.8 V to 5.5 V −40°C ≤ Topr ≤ 85°C	36.311	36.864	37.417	MHz
		Vcc = 1.8 V to 5.5 V Topr =25°C	36.495	36.864	37.233	MHz
	High-speed on-chip oscillator frequency when the FRA6 register correction value is written into	Vcc = 1.8 V to 5.5 V −20°C ≤ Topr ≤ 85°C	31.52	32	32.48	MHz
	correction value into the FRA3 register	Vcc = 1.8 V to 5.5 V -40°C ≤ Topr ≤ 85°C	31.52	32	32.48	MHz
		Vcc = 1.8 V to 5.5 V Topr =25°C	31.68	32	32.32	MHz
-	Oscillation stability time	Vcc = 5.0 V, Topr = 25°C	-	100	450	μS
_	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	-	500	-	μA

Table 5.13 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Notes:

1. Vcc = 1.8 to 5.5 V, Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

2. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.14 L	ow-speed On-Chip Oscillator Circuit Electrical Characteristics
--------------	--

Symbol	Parameter	Condition		Standard		Unit	
Symbol	Falameter	Condition	Min.	Тур.	Max.	Unit	
fOCO-S	Low-speed on-chip oscillator frequency		60	125	250	kHz	
-	Oscillation stability time	Vcc = 5.0 V, Topr = 25°C	-	30	100	μS	
_	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	-	2	-	μA	
fOCO-WDT	Low-speed on-chip oscillator frequency for the watchdog timer		60	125	250	kHz	
-	Oscillation stability time	Vcc = 5.0 V, Topr = 25°C	-	30	100	μS	
-	Self power consumption at oscillation	VCC = 5.0 V, Topr = $25^{\circ}C$	-	2	-	μA	

Note:

1. Vcc = 1.8 to 5.5 V, Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.15 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	0,	Unit		
Symbol	Falanetei	Condition	Min. Typ. Max.	Offic		
td(P-R)	Time for internal power supply stabilization during		-	-	2,000	μS
	power-on ⁽²⁾					

Notes:

The measurement condition is Vcc = 1.8 to 5.5 V and Topr = 25°C.
 Waiting time until the internal power supply generation circuit stabilizes during power-on.

Symbol	Parameter	Condition	Sta	andard		Unit
Symbol	Parameter	Condition	Min.	Тур.	Max.	Unit
tSCL	SCL input cycle time		12tcyc + 600 (2)	-	-	ns
tSCLH	SCL input "H" width		3tcyc + 300 (2)	-	-	ns
tSCLL	SCL input "L" width		5tcyc + 500 (2)	-	-	ns
tsf	SCL, SDA input fall time		-	-	300	ns
tSP	SCL, SDA input spike pulse rejection time		-	-	1tcyc (2)	ns
tbuf	SDA input bus-free time		5tcyc (2)	-	-	ns
t STAH	Start condition input hold time		3tcyc (2)	_	-	ns
t STAS	Retransmit start condition input setup time		3tcyc (2)	_	-	ns
t STOP	Stop condition input setup time		3tcyc (2)	-	-	ns
tSDAS	Data input setup time		1tcyc + 40 (2)	-	-	ns
t SDAH	Data input hold time		10	-	-	ns

Timing Requirements of I²C bus Interface ⁽¹⁾ **Table 5.17**

Notes:

1. Vcc = 1.8 to 5.5 V, Vss = 0 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified. 2. 1tcvc = 1/f1(s)

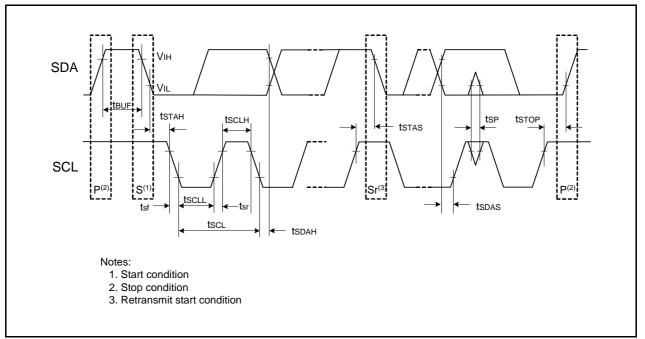






Table 5.19Electrical Characteristics (2) [3.3 V \leq Vcc \leq 5.5 V]
(Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition		Standard	4	Unit
_				Min.	Тур.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V)	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	-	6.5	15	mA
	Single-chip mode, output pins are open, other pins		XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	-	5.3	12.5	mA
	are Vss		XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	-	3.6	-	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	3.0	-	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	2.2	_	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	1.5	_	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	-	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	3.0	-	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTIIC = MSTTRD = MSTTRC = 1	-	1	-	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	-	90	400	μA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	_	85	400	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	_	47	-	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	15	100	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	4	90	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	3.5	-	μΑ
		Stop mode	XIN clock off, Topr = 25° C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	2.0	5.0	μA
			XIN clock off, Topr = 85° C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	5.0	-	μA



Symbol	Dor	ameter	Conditi	<u></u>	Standard			Unit
Symbol	Par	ameter	Conditi	on	Min.	Тур.	Max.	Unit
Vон	Output "H" voltage	Other than XOUT	Drive capacity High	Iон = -5 mA	Vcc - 0.5	-	Vcc	V
			Drive capacity Low	Іон = -1 mA	Vcc - 0.5	-	Vcc	V
		XOUT		Іон = -200 μА	1.0	-	Vcc	V
Vol	Output "L" voltage	Other than XOUT	Drive capacity High	IoL = 5 mA	-	-	0.5	V
			Drive capacity Low	IoL = 1 mA	_	-	0.5	V
		XOUT		IoL = 200 μA	-	-	0.5	V
VT+-VT-	Hysteresis	INTO, INT1, INT3, KIO, KI1, KI2, KI3, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, ADTRG, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO	Vcc = 3.0 V		0.1	0.4	_	V
		RESET	Vcc = 3.0 V		0.1	0.5	-	
Ін	Input "H" current		VI = 3 V, Vcc = 3.0 V		-	_	4.0	μA
lil	Input "L" current		VI = 0 V, Vcc = 3.0 V	/	_	-	-4.0	μA
Rpullup	Pull-up resistance		VI = 0 V, Vcc = 3.0 V	/	42	84	168	kΩ
Rfxin	Feedback resistance	XIN			-	0.3	-	MΩ
RfxCIN	Feedback resistance	XCIN			-	8	-	MΩ
Vram	RAM hold voltage		During stop mode		1.8	-	-	V

Table 5.24 Electrical Characteristics (3) [2.7 V \leq Vcc < 4.2 V]

Note:

1. 2.7 V \leq Vcc < 4.2 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.



Symbol	Dor	ameter	Conditi	<u></u>	S	tandard		Unit
Symbol	Fai	ameter	Conditi	UII	Min.	Тур.	Max.	Unit
Vон	Output "H" voltage	Other than XOUT	Drive capacity High	Іон = -2 mA	Vcc - 0.5	-	Vcc	V
			Drive capacity Low	Iон = -1 mA	Vcc - 0.5	-	Vcc	V
		XOUT		Іон = -200 μА	1.0	-	Vcc	V
Vol	Output "L" voltage	Other than XOUT	Drive capacity High	Iol = 2 mA	-	-	0.5	V
			Drive capacity Low	IoL = 1 mA	-	-	0.5	V
		XOUT		IOL = 200 μA	-	-	0.5	V
VT+-VT-	Hysteresis	INTO, INT1, INT3, KIO, KI1, KI2, KI3, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, ADTRG, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO	Vcc = 2.2 V		0.05	0.20	_	V
		RESET	Vcc = 2.2 V		0.05	0.2	-	V
Ін	Input "H" current		VI = 2.2 V, Vcc = 2.2	2 V	-	-	4.0	μΑ
lı∟	Input "L" current		VI = 0 V, Vcc = 2.2 \	/	-	-	-4.0	μΑ
Rpullup	Pull-up resistance		VI = 0 V, Vcc = 2.2 \	/	70	140	300	kΩ
Rfxin	Feedback resistance	XIN			-	0.3	-	MΩ
RfxCIN	Feedback resistance	XCIN			-	8	-	MΩ
Vram	RAM hold voltage		During stop mode		1.8	-	_	V

Table 5.30 Electrical Characteristics (5) [1.8 V \leq Vcc < 2.7 V]

Note:

1. $1.8 \text{ V} \le \text{Vcc} < 2.7 \text{ V}$ and $\text{T}_{opr} = -20 \text{ to } 85^{\circ}\text{C}$ (N version) / -40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.



Symbol	Parameter		Condition		Standar	d	Unit
Symbol	Parameter		Condition	Min.	Тур.	Max.	Unit
lcc	Power supply current (Vcc = 1.8 to 2.7 V) Single-chip mode, output pins are open,	High-speed clock mode	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	_	2.2	-	mA
	other pins are Vss	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	Low-speed on-chip oscillator on = 125 kHz	-	0.8	_	mA
		High-speed on-chip oscillator	XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division	_	2.5	10	mA
		mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	1.7	-	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTIIC = MSTTRD = MSTTRC = 1	_	1	_	mA
	Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	-	90	300	μA	
	Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	-	80	350	μA	
		XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	-	40	_	μA	
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	15	90	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	4	80	μA
		XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	3.5	_	μA	
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	2.0	5	μA
		XIN clock off, $T_{opr} = 85^{\circ}C$ High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	5.0	_	μA	



Timing requirements (Unless Otherwise Specified: Vcc = 2.2 V, Vss = 0 V at Topr = 25°C)

Table 5.32 External Clock Input (XOUT, XCIN)

Symbol	Parameter	Standard		Lloit	
Symbol	Falanetei	Min.	Max.	Unit	
tc(XOUT)	XOUT input cycle time	200	-	ns	
twh(xout)	XOUT input "H" width	90	-	ns	
twl(xout)	XOUT input "L" width	90	-	ns	
tc(XCIN)	XCIN input cycle time	14	-	μS	
tWH(XCIN)	XCIN input "H" width	7	-	μS	
twl(xcin)	XCIN input "L" width	7	-	μS	

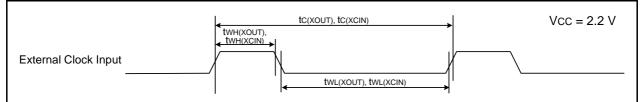


Figure 5.16 External Clock Input Timing Diagram when Vcc = 2.2 V

Table 5.33 TRAIO Input

Symbol	Parameter	Stan	dard	Unit ns ns
	Falameter	Min.	Max.	Unit
tc(TRAIO)	TRAIO input cycle time	500	-	ns
twh(traio)	TRAIO input "H" width	200	-	ns
twl(traio)	TRAIO input "L" width	200	-	ns

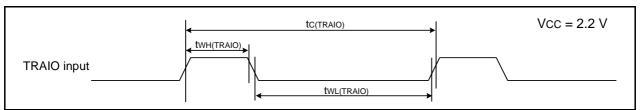


Figure 5.17 TRAIO Input Timing Diagram when Vcc = 2.2 V

Table 5.34 Serial Interface

Symbol	Parameter		Standard		Unit
			Min.	Max.	Unit
tc(CK)	CLKi input cycle time	When external clock is selected	800	-	ns
tW(CKH)	CLKi input "H" width		400	-	ns
tW(CKL)	CLKi input "L" width		400	-	ns
td(C-Q)	TXDi output delay time		-	200	ns
th(C-Q)	TXDi hold time		0	-	ns
tsu(D-C)	RXDi input setup time	XDi input setup time 150 –		ns	
th(C-D)	RXDi input hold time		90	-	ns
td(C-Q)	TXDi output delay time	When internal clock is selected	-	200	ns
tsu(D-C)	RXDi input setup time		150	-	ns
th(C-D)	RXDi input hold time		90	-	ns

i = 0 to 2

Note: 1. Vcc = 2.2 V and Topr = -20 to 85 °C (N version)/-40 to 85 °C (D version), unless otherwise specified.

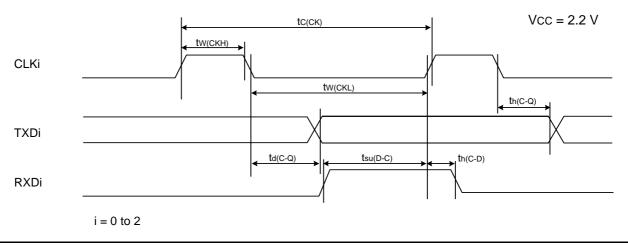


Figure 5.18 Serial Interface Timing Diagram when Vcc = 2.2 V

Table 5.35External Interrupt INTi (i = 0, 1, 3) Input, Key Input Interrupt Kli (i = 0 to 3)

Symbol	Parameter		Standard	
			Max.	Unit
tw(INH)	INTi input "H" width, Kli input "H" width		-	ns
tw(INL)	INTi input "L" width, Kli input "L" width		-	ns

Notes:

1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

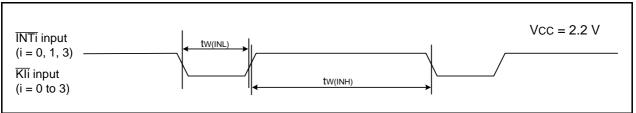


Figure 5.19 Input Timing Diagram for External Interrupt INTi and Key Input Interrupt Kli when Vcc = 2.2 V

REVISION HISTORY	R8C/33M Group Datasheet
-------------------------	-------------------------

Rev.	Date	Description	
		Page	Summary
0.10	Sep 28, 2010	-	First Edition issued
0.20	Feb 15, 2011	34	Table 5.11 revised, Note 2 added
		35	Table 5.13 and Table 5.14 revised
		41	Table 5.18 revised
		49	Table 5.30 revised
1.00	Jun 27, 2011	All pages	"Preliminary", "Under development" deleted
		4	Table 1.3 "(D): Under development" deleted
		27	Table 5.2 revised
		34	Table 5.11 revised
		35	Table 5.13 revised
		43	Table 5.20 revised
		44	Table 5.22 Note 1 added
		47	Table 5.26 revised
		48	Table 5.28 Note 1 added
		51	Table 5.32 revised
		52	Table 5.34 Note 1 added

All trademarks and registered trademarks are the property of their respective owners.

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
- 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
 - In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do
 not access these addresses; the correct operation of LSI is not guaranteed if they are
 accessed.
- 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
- 5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

— The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.