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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	46
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 2x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkv31f256vlh12

Table of Contents

1 Ratings.....	5	3.6 Analog.....	32
1.1 Thermal handling ratings.....	5	3.6.1 ADC electrical specifications.....	32
1.2 Moisture handling ratings.....	5	3.6.2 CMP and 6-bit DAC electrical specifications.....	36
1.3 ESD handling ratings.....	5	3.6.3 12-bit DAC electrical characteristics.....	39
1.4 Voltage and current operating ratings.....	5	3.6.4 Voltage reference electrical specifications.....	42
2 General.....	6	3.7 Timers.....	43
2.1 AC electrical characteristics.....	6	3.8 Communication interfaces.....	43
2.2 Nonswitching electrical specifications.....	6	3.8.1 DSPI switching specifications (limited voltage range).....	44
2.2.1 Voltage and current operating requirements.....	6	3.8.2 DSPI switching specifications (full voltage range).....	45
2.2.2 LVD and POR operating requirements.....	7	3.8.3 Inter-Integrated Circuit Interface (I2C) timing.....	47
2.2.3 Voltage and current operating behaviors.....	8	3.8.4 UART switching specifications.....	49
2.2.4 Power mode transition operating behaviors.....	9	3.9 Kinetis Motor Suite.....	49
2.2.5 Power consumption operating behaviors.....	10	4 Dimensions.....	49
2.2.6 EMC radiated emissions operating behaviors.....	16	4.1 Obtaining package dimensions.....	49
2.2.7 Designing with radiated emissions in mind.....	17	5 Pinout.....	50
2.2.8 Capacitance attributes.....	17	5.1 KV31F Signal Multiplexing and Pin Assignments.....	50
2.3 Switching specifications.....	17	5.2 Recommended connection for unused analog and digital pins.....	54
2.3.1 Device clock specifications.....	17	5.3 KV31F Pinouts.....	55
2.3.2 General switching specifications.....	18	6 Part identification.....	57
2.4 Thermal specifications.....	18	6.1 Description.....	57
2.4.1 Thermal operating requirements.....	19	6.2 Format.....	58
2.4.2 Thermal attributes.....	19	6.3 Fields.....	58
3 Peripheral operating requirements and behaviors.....	20	6.4 Example.....	59
3.1 Core modules.....	20	7 Terminology and guidelines.....	59
3.1.1 SWD electricals	20	7.1 Definitions.....	59
3.1.2 JTAG electricals.....	21	7.2 Examples.....	59
3.2 System modules.....	24	7.3 Typical-value conditions.....	60
3.3 Clock modules.....	24	7.4 Relationship between ratings and operating requirements.....	60
3.3.1 MCG specifications.....	24	7.5 Guidelines for ratings and operating requirements.....	61
3.3.2 IRC48M specifications.....	27	8 Revision History.....	61
3.3.3 Oscillator electrical specifications.....	27		
3.4 Memories and memory interfaces.....	29		
3.4.1 Flash electrical specifications.....	29		
3.4.2 EzPort switching specifications.....	31		
3.5 Security and integrity modules.....	32		

General

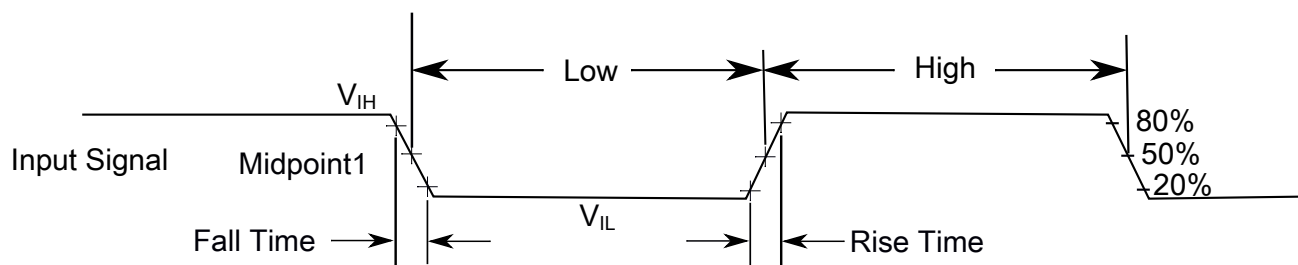
Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	-0.3	3.8	V
I_{DD}	Digital supply current	—	158	mA
V_{DIO}	Digital input voltage	-0.3	$V_{DD} + 0.3$	V
V_{AIO}	Analog ¹	-0.3	$V_{DD} + 0.3$	V
I_D	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 2. Input signal measurement reference

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	

Table continues on the next page...

Table 2. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
V_{LVW1L}	Low-voltage warning thresholds — low range					1
	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μ s	

1. Rising threshold is the sum of falling threshold and hysteresis voltage

2.2.3 Voltage and current operating behaviors

Table 3. Voltage and current operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{OH}	Output high voltage — Normal drive pad except RESET_B					
	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -5\text{ mA}$	$V_{DD} - 0.5$	—	—	V	1
	$1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -2.5\text{ mA}$	$V_{DD} - 0.5$	—	—	V	
V_{OH}	Output high voltage — High drive pad except RESET_B					
	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -20\text{ mA}$	$V_{DD} - 0.5$	—	—	V	1
	$1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -10\text{ mA}$	$V_{DD} - 0.5$	—	—	V	
I_{OHT}	Output high current total for all ports	—	—	100	mA	
V_{OL}	Output low voltage — Normal drive pad except RESET_B					
	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 5\text{ mA}$	—	—	0.5	V	1
	$1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 2.5\text{ mA}$	—	—	0.5	V	
V_{OL}	Output low voltage — High drive pad except RESET_B					
	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 20\text{ mA}$	—	—	0.5	V	1
	$1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 10\text{ mA}$	—	—	0.5	V	
V_{OL}	Output low voltage — RESET_B					

Table continues on the next page...

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at frequencies between 50 MHz and 100MHz. MCG in PEE mode at frequencies greater than 100 MHz.
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

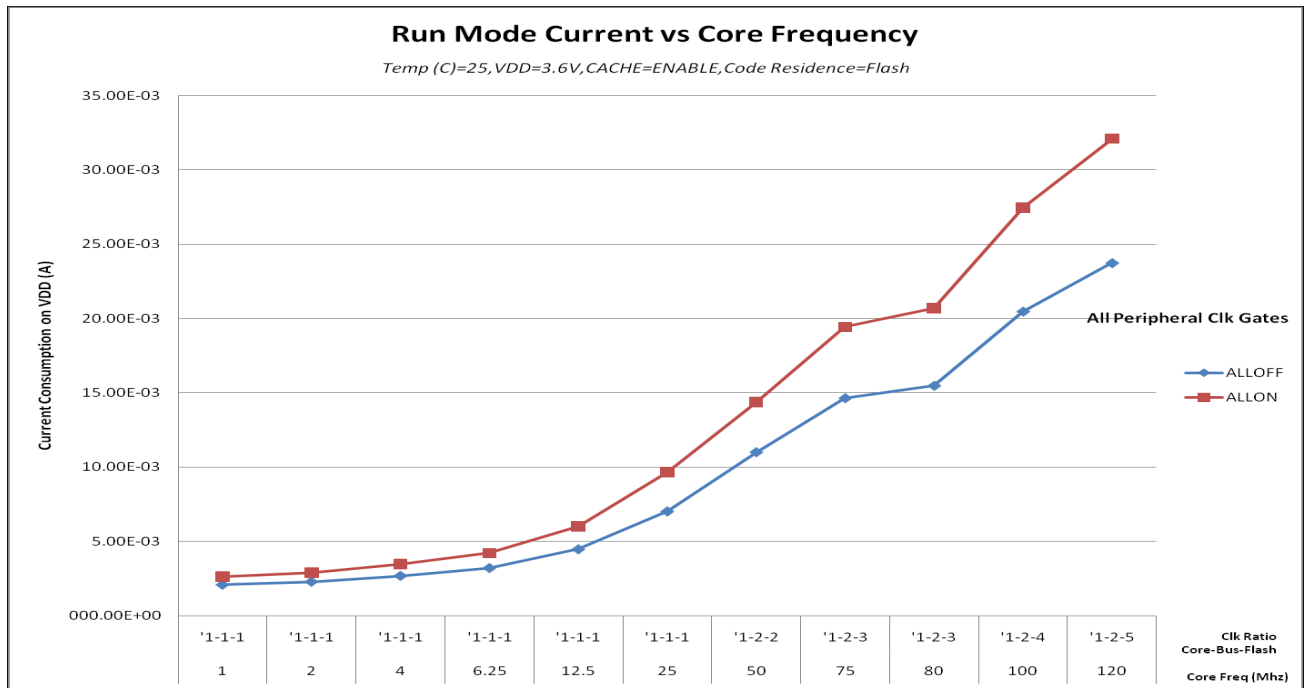


Figure 3. Run mode supply current vs. core frequency

Table 9. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
$f_{\text{LPTMR_pin}}$	LPTMR clock	—	25	MHz	
$f_{\text{LPTMR_ERCLK}}$	LPTMR external reference clock	—	16	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled) — Asynchronous path	50	—	ns	4
	Mode select ($\overline{\text{EZP_CS}}$) hold time after reset deassertion	2	—	Bus clock cycles	
	Port rise and fall time • Slew disabled • $1.71 \leq V_{\text{DD}} \leq 2.7\text{V}$ • $2.7 \leq V_{\text{DD}} \leq 3.6\text{V}$ • Slew enabled • $1.71 \leq V_{\text{DD}} \leq 2.7\text{V}$ • $2.7 \leq V_{\text{DD}} \leq 3.6\text{V}$	— — — —	10 5 30 16	ns ns ns ns	5

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater of synchronous and asynchronous timing must be met.
3. These pins have a passive filter enabled on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
4. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
5. 25 pF load

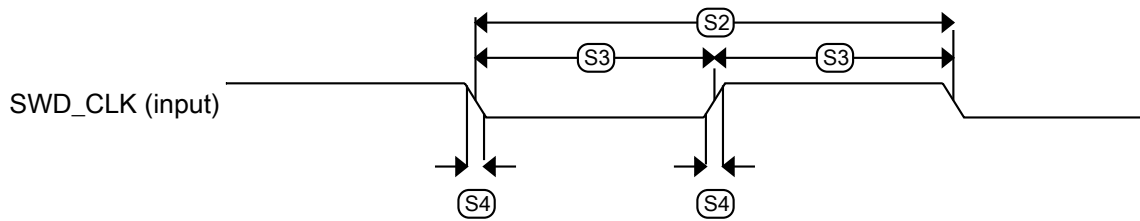


Figure 5. Serial wire clock input timing

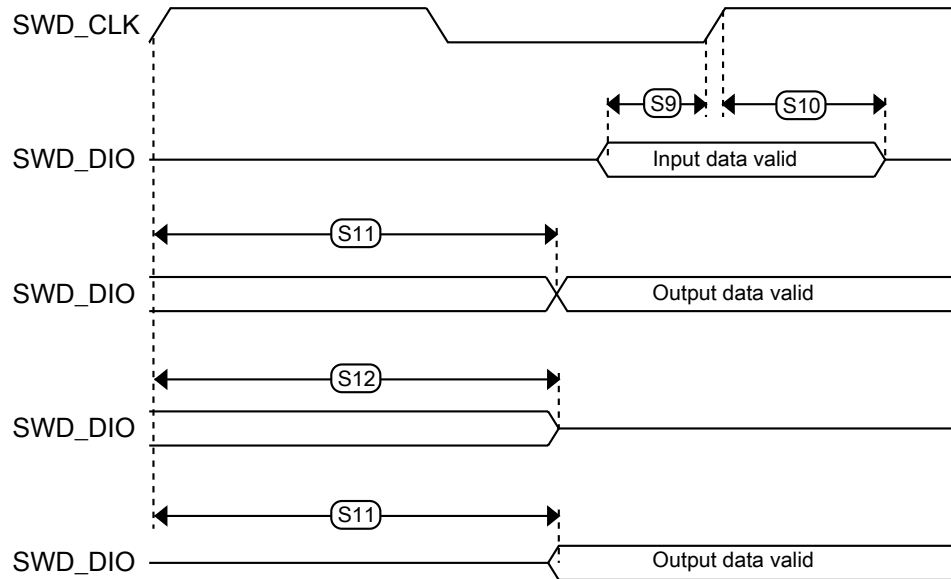


Figure 6. Serial wire data timing

3.1.2 JTAG electricals

Table 13. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation - Boundary Scan - JTAG and CJTAG	0 0	10 20	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width	50	—	ns

Table continues on the next page...

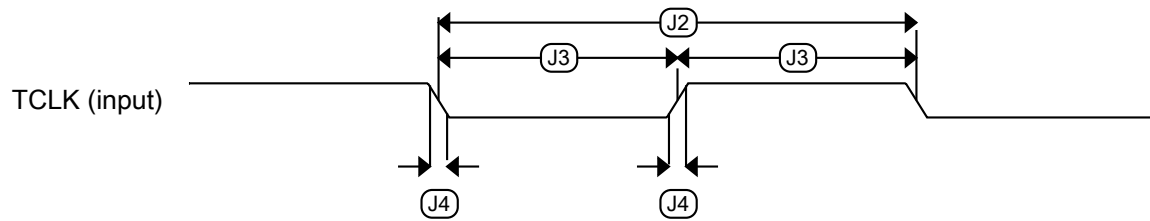


Figure 7. Test clock input timing

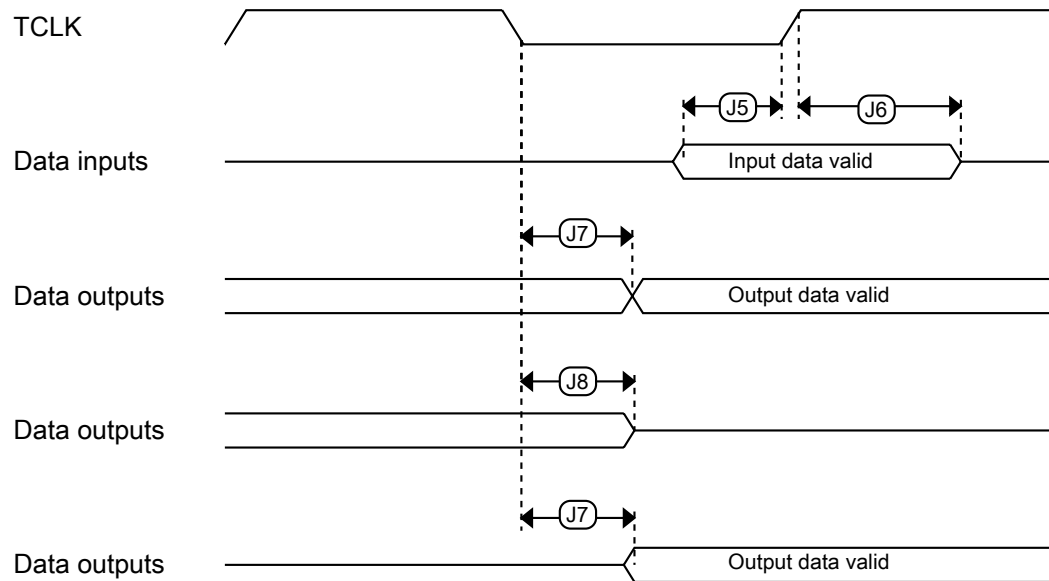


Figure 8. Boundary scan (JTAG) timing

3.3.1 MCG specifications

Table 15. MCG specifications

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f _{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C		—	32.768	—	kHz	
Δf _{ints_t}	Total deviation of internal reference frequency (slow clock) over voltage and temperature		—	+0.5/-0.7	± 2	%	
f _{ints_t}	Internal reference frequency (slow clock) — user trimmed		31.25	—	39.0625	kHz	
Δf _{dco_res_t}	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM		—	± 0.3	± 0.6	%f _{dco}	1
Δf _{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—	+0.5/-0.7	± 2	%f _{dco}	1, 2
Δf _{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C		—	± 0.3	± 1.5	%f _{dco}	1
f _{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C		—	4	—	MHz	
Δf _{intf_ft}	Frequency deviation of internal reference clock (fast clock) over temperature and voltage — factory trimmed at nominal VDD and 25 °C		—	+1/-2	± 5	%f _{intf_ft}	
f _{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C		3	—	5	MHz	
f _{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f _{ints_t}	—	—	kHz	
f _{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f _{ints_t}	—	—	kHz	
FLL							
f _{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f _{dco}	DCO output frequency range	Low range (DRS=00) 640 × f _{fll_ref}	20	20.97	25	MHz	3, 4
		Mid range (DRS=01) 1280 × f _{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f _{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f _{fll_ref}	80	83.89	100	MHz	
f _{dco_t_DMX32}	DCO output frequency	Low range (DRS=00) 732 × f _{fll_ref}	—	23.99	—	MHz	5, 6
		Mid range (DRS=01) 1464 × f _{fll_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10)	—	71.99	—	MHz	

Table continues on the next page...

3.3.2 IRC48M specifications

Table 16. IRC48M specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{DD}	Supply voltage	1.71	—	3.6	V	
I _{DD48M}	Supply current	—	400	500	μA	
f _{irc48m}	Internal reference frequency	—	48	—	MHz	
Δf _{irc48m_ol_hv}	Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over 0°C to 70°C	—	± 0.2	± 0.5	%f _{irc48m}	1
Δf _{irc48m_ol_hv}	Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over full temperature	—	± 0.4	± 1.0	%f _{irc48m}	1
Δf _{irc48m_ol_lv}	Open loop total deviation of IRC48M frequency at low voltage (VDD=1.71V-1.89V) over full temperature	—	± 0.5	± 1.5	%f _{irc48m}	1
J _{cyc_irc48m}	Period Jitter (RMS)	—	35	150	ps	
t _{irc48mst}	Startup time	—	2	3	μs	2

1. The maximum value represents characterized results equivalent to the mean plus or minus three times the standard deviation (mean ± 3 sigma).
2. IRC48M startup time is defined as the time between clock enablement and clock availability for system use. Enable the clock by one of the following settings:
 - MCG operating in an external clocking mode and MCG_C7[OSCSEL]=10 or MCG_C5[PLLCLKEN0]=1, or
 - SIM_SOPT2[PLLFLSEL]=11

3.3.3 Oscillator electrical specifications

3.3.3.1 Oscillator DC electrical specifications

Table 17. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{DD}	Supply voltage	1.71	—	3.6	V	
I _{DDOSC}	Supply current — low-power mode (HGO=0) • 32 kHz • 4 MHz • 8 MHz (RANGE=01) • 16 MHz • 24 MHz • 32 MHz	—	500	—	nA	1
		—	200	—	μA	
		—	300	—	μA	
		—	950	—	μA	
		—	1.2	—	mA	
		—	1.5	—	mA	
I _{DDOSC}	Supply current — high-gain mode (HGO=1)					1

Table continues on the next page...

Table 17. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	32 kHz 4 MHz 8 MHz (RANGE=01) 16 MHz 24 MHz 32 MHz	—	25	—	μA	
		—	400	—	μA	
		—	500	—	μA	
		—	2.5	—	mA	
		—	3	—	mA	
		—	4	—	mA	
C _x	EXTAL load capacitance	—	—	—		2, 3
C _y	XTAL load capacitance	—	—	—		2, 3
R _F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R _S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V _{pp} ⁵	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V _{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V _{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C

2. See crystal or resonator manufacturer's recommendation

3. C_x and C_y can be provided by using either integrated capacitors or external components.4. When low-power mode is selected, R_F is integrated and must not be attached externally.

5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

3.3.3.2 Oscillator frequency specifications

Table 18. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc_hi_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc_hi_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

3.4 Memories and memory interfaces

3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

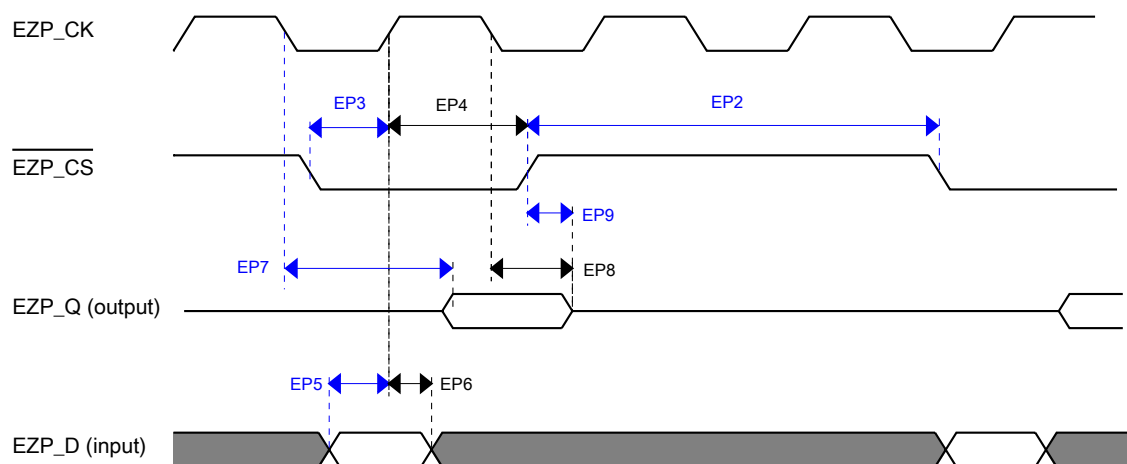


Figure 11. EzPort Timing Diagram

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog

3.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 24](#) and [Table 25](#) are achievable on the differential pins ADCx_DPx, ADCx_DMx.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

3.6.1.1 16-bit ADC operating conditions

Table 24. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} ($V_{DD} - V_{DDA}$)	-100	0	+100	mV	2

Table continues on the next page...

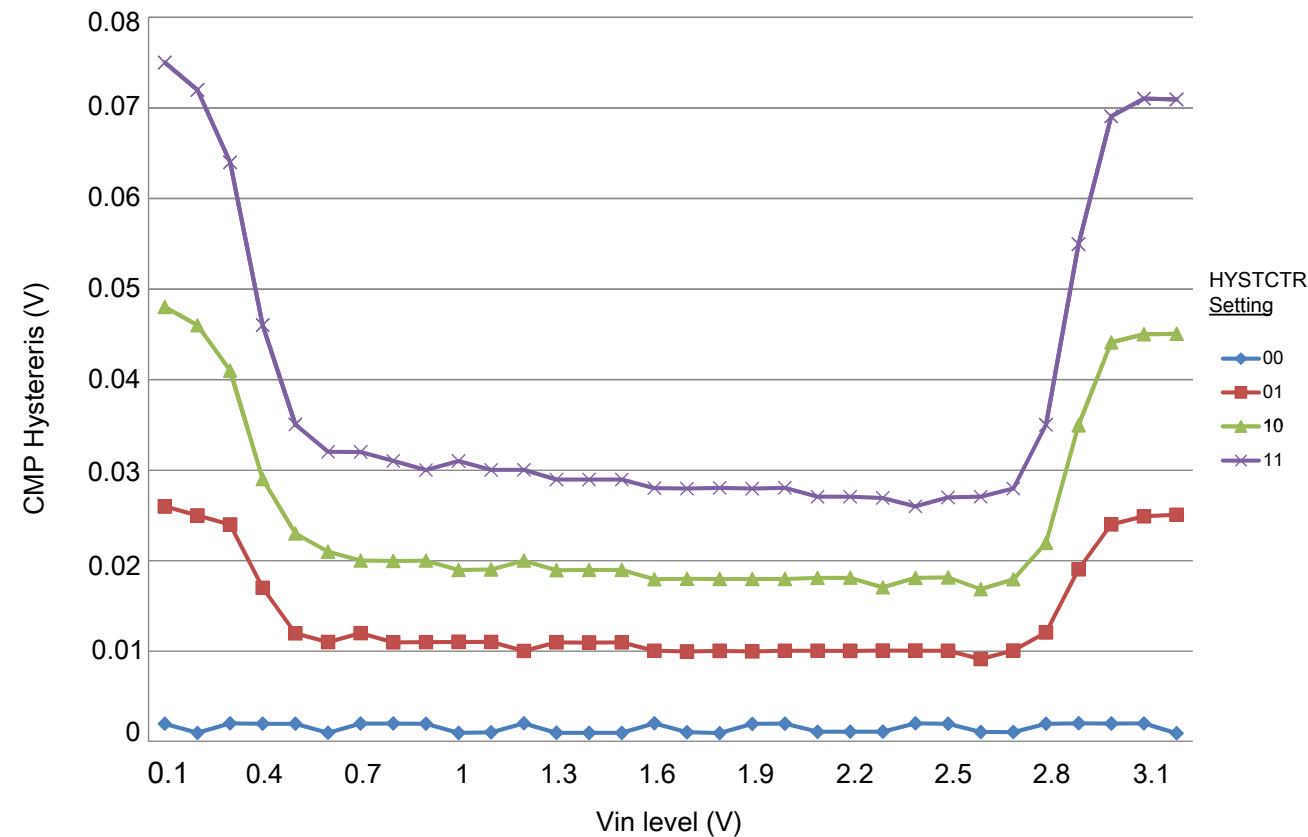


Figure 15. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

Table 30. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25°C	1.1920	1.1950	1.1980	V	1
V_{out}	Voltage reference output with user trim at nominal V_{DDA} and temperature=25°C	1.1945	1.1950	1.1955	V	1
V_{step}	Voltage reference trim step	—	0.5	—	mV	1
V_{tdrift}	Temperature drift ($V_{max} - V_{min}$ across the full temperature range)	—	—	15	mV	1
I_{bg}	Bandgap only current	—	—	80	μA	
I_{lp}	Low-power buffer current	—	—	360	μA	1
I_{hp}	High-power buffer current	—	—	1	mA	1
ΔV_{LOAD}	Load regulation • current = ± 1.0 mA	—	200	—	μV	1, 2
T_{stup}	Buffer startup time	—	—	100	μs	
$T_{chop_osc_st_up}$	Internal bandgap start-up delay with chop oscillator enabled	—	—	35	ms	
V_{vdift}	Voltage drift ($V_{max} - V_{min}$ across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 31. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	70	°C	

Table 32. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{tdrift}	Temperature drift ($V_{max} - V_{min}$ across the limited temperature range)	—	10	mV	

3.7 Timers

See [General switching specifications](#).

3.8 Communication interfaces

3.8.2 DSPI switching specifications (full voltage range)

The Deserial Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 35. Master mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	15	MHz	
DS1	DSPI_SCK output cycle time	$4 \times t_{\text{BUS}}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{\text{SCK}}/2) - 4$	$(t_{\text{SCK}}/2) + 4$	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	$(t_{\text{BUS}} \times 2) - 4$	—	ns	2
DS4	DSPI_SCK to DSPI_PCSn invalid delay	$(t_{\text{BUS}} \times 2) - 4$	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-4.5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	24.6	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

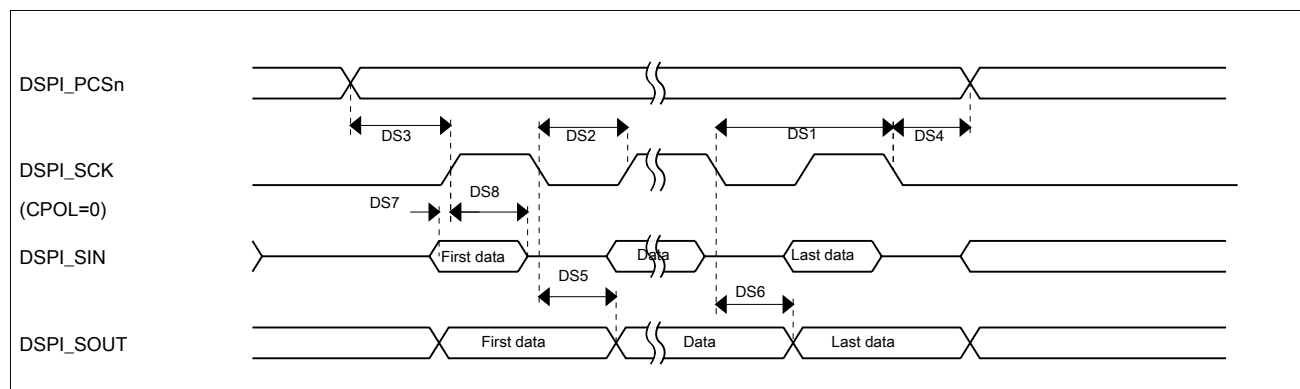


Figure 21. DSPI classic SPI timing — master mode

Pinout

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
41	—	VSS	VSS	VSS								
42	28	PTA12	DISABLED		PTA12		FTM1_CH0				FTM1_QD_ PHA	
43	29	PTA13/ LLWU_P4	DISABLED		PTA13/ LLWU_P4		FTM1_CH1				FTM1_QD_ PHB	
44	—	PTA14	DISABLED		PTA14	SPI0_PCS0	UART0_TX					
45	—	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_RX					
46	—	PTA16	DISABLED		PTA16	SPI0_SOUT	UART0_ CTS_b					
47	—	PTA17	ADC1_SE17	ADC1_SE17	PTA17	SPI0_SIN	UART0_ RTS_b					
48	30	VDD	VDD	VDD								
49	31	VSS	VSS	VSS								
50	32	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0				
51	33	PTA19	XTAL0	XTAL0	PTA19	FTM0_FLT0	FTM1_FLT0	FTM_CLKIN1		LPTMR0_ ALT1		
52	34	RESET_b	RESET_b	RESET_b								
53	35	PTB0/ LLWU_P5	ADC0_SE8/ ADC1_SE8	ADC0_SE8/ ADC1_SE8	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_ PHA	UART0_RX	
54	36	PTB1	ADC0_SE9/ ADC1_SE9	ADC0_SE9/ ADC1_SE9	PTB1	I2C0_SDA	FTM1_CH1	FTM0_FLT2	EWM_IN	FTM1_QD_ PHB	UART0_TX	
55	37	PTB2	ADC0_SE12	ADC0_SE12	PTB2	I2C0_SCL	UART0_ RTS_b	FTM0_FLT1		FTM0_FLT3		
56	38	PTB3	ADC0_SE13	ADC0_SE13	PTB3	I2C0_SDA	UART0_ CTS_b			FTM0_FLT0		
57	—	PTB9	DISABLED		PTB9	SPI1_PCS1	LPUART0_ CTS_b					
58	—	PTB10	ADC1_SE14	ADC1_SE14	PTB10	SPI1_PCS0	LPUART0_ RX			FTM0_FLT1		
59	—	PTB11	ADC1_SE15	ADC1_SE15	PTB11	SPI1_SCK	LPUART0_ TX			FTM0_FLT2		
60	—	VSS	VSS	VSS								
61	—	VDD	VDD	VDD								
62	39	PTB16	DISABLED		PTB16	SPI1_SOUT	UART0_RX	FTM_CLKIN0		EWM_IN		
63	40	PTB17	DISABLED		PTB17	SPI1_SIN	UART0_TX	FTM_CLKIN1		EWM_OUT_ b		
64	41	PTB18	DISABLED		PTB18		FTM2_CH0			FTM2_QD_ PHA		
65	42	PTB19	DISABLED		PTB19		FTM2_CH1			FTM2_QD_ PHB		
66	—	PTB20	DISABLED		PTB20					CMP0_OUT		
67	—	PTB21	DISABLED		PTB21					CMP1_OUT		
68	—	PTB22	DISABLED		PTB22							
69	—	PTB23	DISABLED		PTB23		SPI0_PCS5					

Pinout

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
97	61	PTD4/LLWU_P14	DISABLED		PTD4/LLWU_P14	SPI0_PCS1	UART0_RTS_b	FTM0_CH4		EWM_IN	SPI1_PCS0	
98	62	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_b	FTM0_CH5		EWM_OUT_b	SPI1_SCK	
99	63	PTD6/LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6		FTM0_FLT0	SPI1_SOUT	
100	64	PTD7	DISABLED		PTD7		UART0_TX	FTM0_CH7		FTM0_FLT1	SPI1_SIN	

5.2 Recommended connection for unused analog and digital pins

The following table shows the recommended connections for analog interface pins if those analog interfaces are not used in the customer's application.

Table 39. Recommended connection for unused analog interfaces

Pin Type		Short recommendation	Detailed recommendation
Analog/non GPIO	PGAx/ADCx	Float	Analog input - Float
Analog/non GPIO	ADCx/CMPx	Float	Analog input - Float
Analog/non GPIO	VREF_OUT	Float	Analog output - Float
Analog/non GPIO	DACx_OUT	Float	Analog output - Float
Analog/non GPIO	RTC_WAKEUP_B	Float	Analog output - Float
Analog/non GPIO	XTAL32	Float	Analog output - Float
Analog/non GPIO	EXTAL32	Float	Analog input - Float
GPIO/Analog	PTA18/EXTAL0	Float	Analog input - Float
GPIO/Analog	PTA19/XTAL0	Float	Analog output - Float
GPIO/Analog	PTx/ADCx	Float	Float (default is analog input)
GPIO/Analog	PTx/CMPx	Float	Float (default is analog input)
GPIO/Digital	PTA0/JTAG_TCLK	Float	Float (default is JTAG with pulldown)
GPIO/Digital	PTA1/JTAG_TDI	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA2/JTAG_TDO	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA3/JTAG_TMS	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA4/NMI_b	10kΩ pullup or disable and float	Pull high or disable in PCR & FOPT and float
GPIO/Digital	PTx	Float	Float (default is disabled)
VDDA	VDDA	Always connect to VDD potential	Always connect to VDD potential

Table continues on the next page...

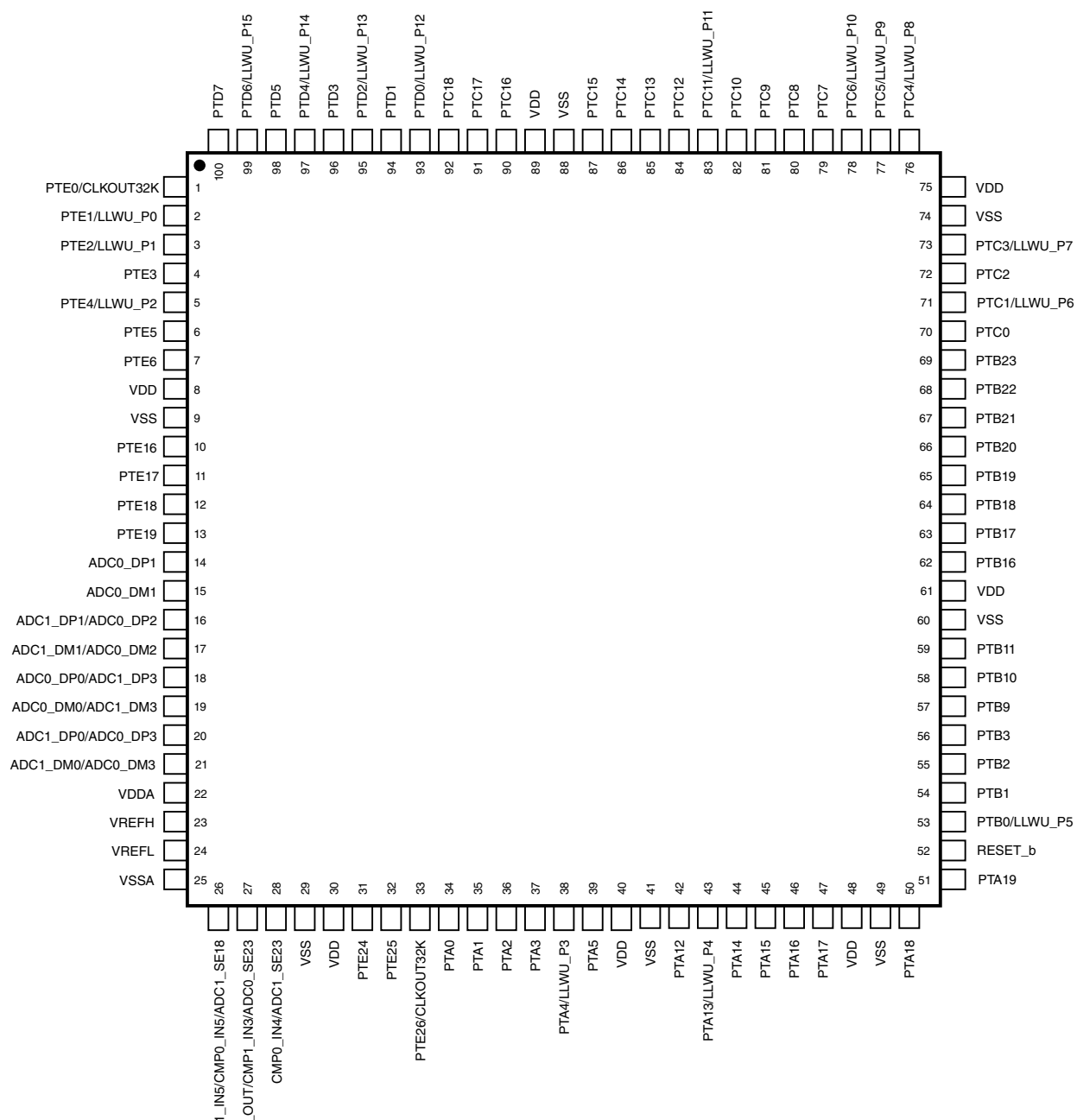


Figure 25. KV31F 100 LQFP pinout diagram (top view)

6 Part identification

Table 40. Revision History (continued)

Rev. No.	Date	Substantial Changes
		- Updated the Part Number Example - Updated IRC48M specifications table
6	10/2015	- In "Power consumption operating behaviors" section, added "Low power mode peripheral adders—typical value" table - In "Thermal operating requirements" table, in footnote, corrected "$T_J = T_A + \Theta_{JA}$" to "$T_J = T_A + R_{\Theta JA}$" - Updated "IRC48M specifications" table - Updated "NVM program/erase timing specifications" table; updated values for $t_{hversall}$ (Erase All high-voltage time) - In "Slave mode DSPI timing (limited voltage range)" table, added footnote regarding maximum frequency of operation - Added new section, "Recommended connections for unused analog and digital pins"
5	4/2015	- Throughout: Removed notes stating that the 64-pin MAPBGA package for this product is not yet available - On page 1: - Under "Security and integrity modules" added "Hardware random-number generator" - Under "Communication interfaces," updated I²C bullet to indicate support for up to 1 Mbps operation - Under "Operating characteristics," specified that voltage range includes flash writes - In figure, "Functional block diagram," added "Random-number generator" and "Flash access control" - In "Voltage and current operating requirements" table: - Removed content related to positive injection - Updated footnote 1 to say that all analog and I/O pins are internally clamped to V_{SS} only (not V_{SS} and V_{DD}) through ESD protection diodes. - In "Power consumption operating behaviors" table: - Added additional temperature data in power consumption table - Added Max IDD values based on characterization results equivalent to mean + 3 sigma - Updated "EMC radiated emissions operating behaviors" table - In "Thermal operating requirements" table, added the following footnote for ambient temperature: "Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is: $T_J = T_A + \Theta_{JA} \times \text{chip power dissipation}$" - Updated "IRC48M Specifications": - Updated maximum values for $\Delta_{firc48m_lv}$ and $\Delta_{firc48m_hv}$ (full temperature) - Added specifications for $\Delta_{firc48m_hv}$ (-40°C to 85°C) - In "I²C timing" table, - Added the following footnote on maximum Fast mode value for SCL Clock Frequency: "The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only be achieved when using the High drive pins across the full voltage range and when using the Normal drive pins and $V_{DD} \geq 2.7$ V." - Updated minimum Fast mode value for LOW period of the SCL clock to 1.25 μ - Added "I²C 1 Mbps timing" table - Specified that the figure, "KV31F 64 LQFP Pinout Diagram" is a top view - Specified that the figure, "KV31F 100 LQFP Pinout Diagram" is a top view - Removed Section 6, "Ordering parts."
4	7/2014	In "Power consumption operating behaviors table":

Table continues on the next page...

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