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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	AVR
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	123
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/atmel/at32uc3c064c-alur">https://www.e-xfl.com/product-detail/atmel/at32uc3c064c-alur</a>

## 2. Overview

### 2.1 Block diagram

Figure 2-1. Block diagram

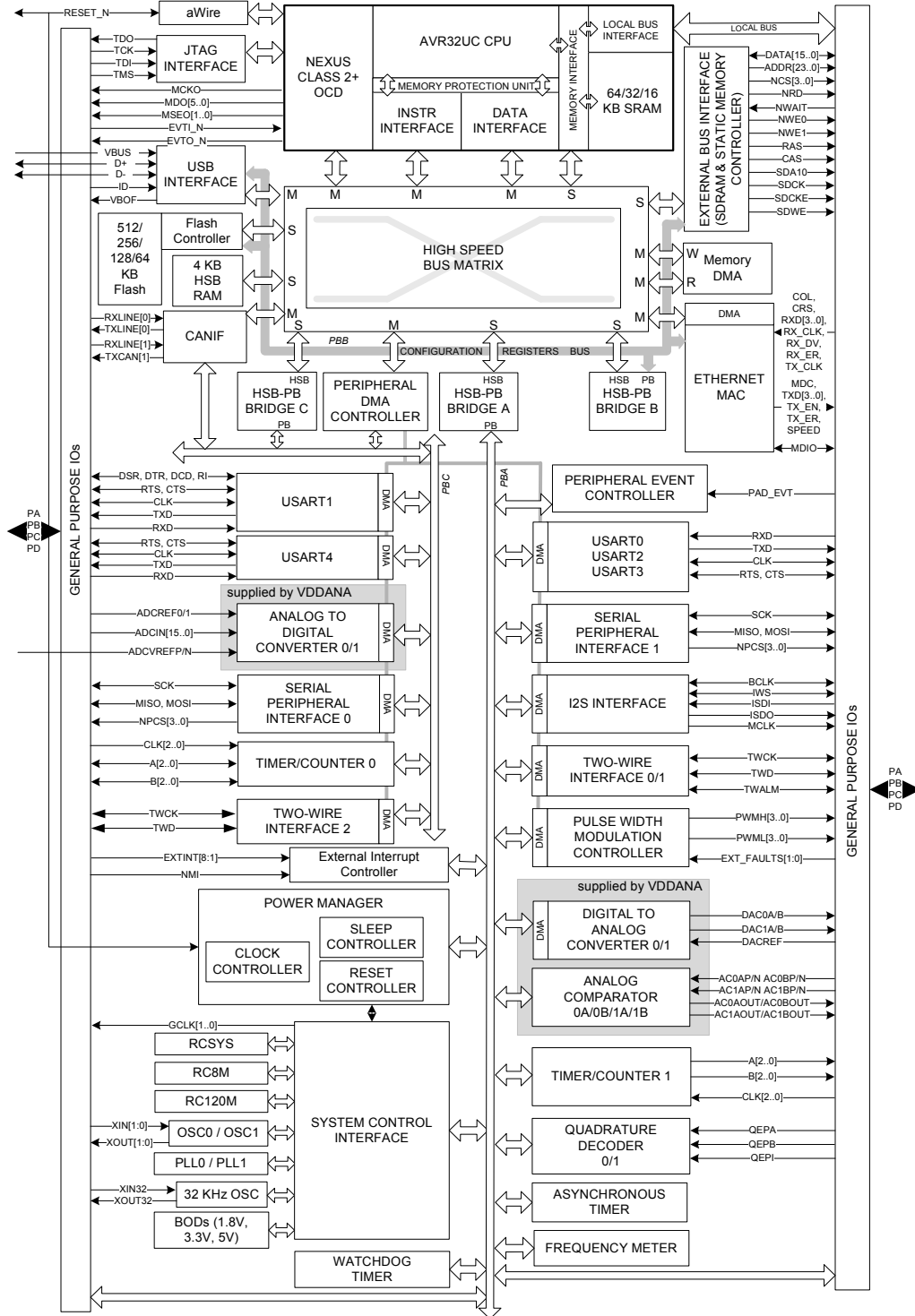
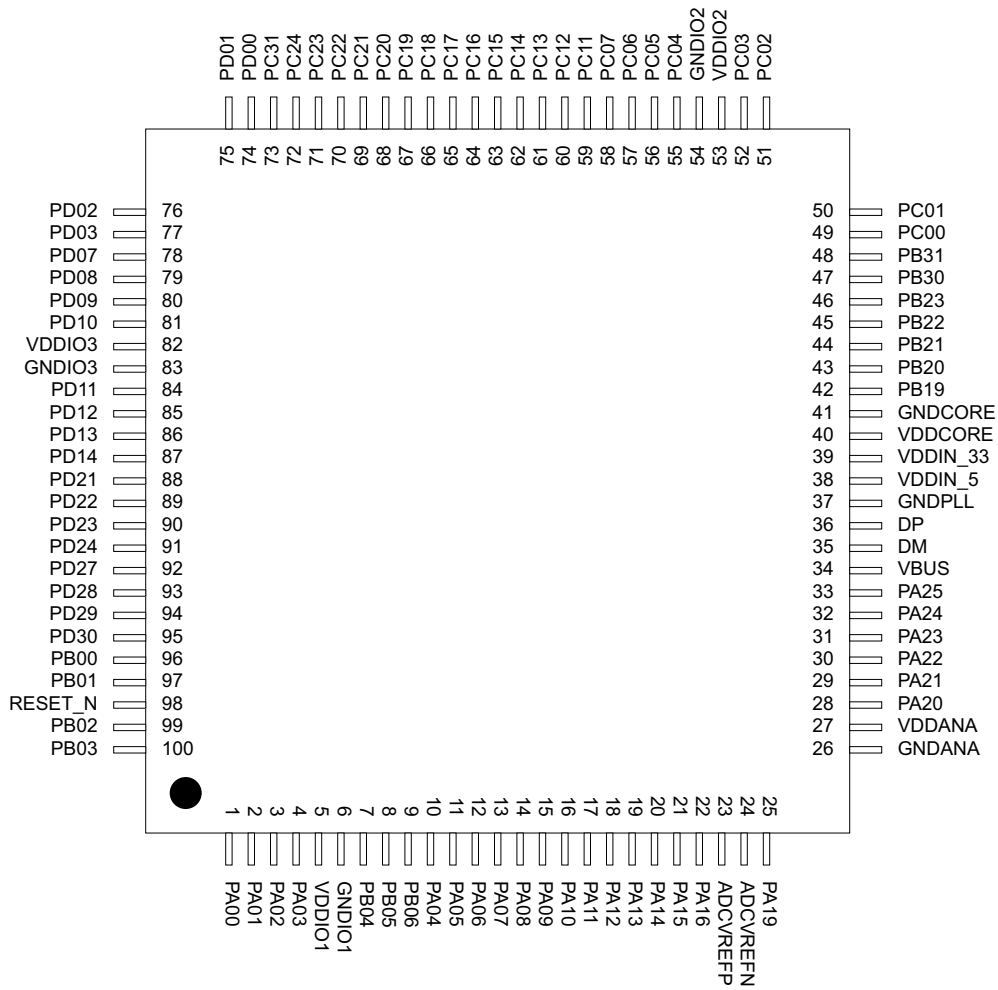


Figure 3-2. TQFP100 Pinout



**Table 3-1. GPIO Controller Function Multiplexing**

TQFP / QFN 64	TQFP 100	LQFP 144	PIN	GPIO	Supply	Pin Type (1)	GPIO function					
							A	B	C	D	E	F
16	25	36	PA19	19	VDDANA	x1/x2	ADCIN8	EIC - EXTINT[1]				
19	28	39	PA20	20	VDDANA	x1/x2	ADCIN9	AC0AP0	AC0AP0 or DAC0A			
20	29	40	PA21	21	VDDANA	x1/x2	ADCIN10	AC0BN0	AC0BN0 or DAC0B			
21	30	41	PA22	22	VDDANA	x1/x2	ADCIN11	AC0AN0	PEVC - PAD_EVT [4]		MACB - SPEED	
22	31	42	PA23	23	VDDANA	x1/x2	ADCIN12	AC0BP0	PEVC - PAD_EVT [5]		MACB - WOL	
	32	43	PA24	24	VDDANA	x1/x2	ADCIN13	SPI1 - NPCS[2]				
	33	44	PA25	25	VDDANA	x1/x2	ADCIN14	SPI1 - NPCS[3]	EIC - EXTINT[0]			
		45	PA26	26	VDDANA	x1/x2	AC0AP1	EIC - EXTINT[1]				
		46	PA27	27	VDDANA	x1/x2	AC0AN1	EIC - EXTINT[2]				
		47	PA28	28	VDDANA	x1/x2	AC0BP1	EIC - EXTINT[3]				
		48	PA29	29	VDDANA	x1/x2	AC0BN1	EIC - EXTINT[0]				
62	96	140	PB00	32	VDDIO1	x1	USART0 - CLK	CANIF - RXLINE[1]	EIC - EXTINT[8]	PEVC - PAD_EVT [10]		
63	97	141	PB01	33	VDDIO1	x1		CANIF - TXLINE[1]		PEVC - PAD_EVT [11]		
	99	143	PB02	34	VDDIO1	x1		USBC - ID	PEVC - PAD_EVT [6]	TC1 - A1		
	100	144	PB03	35	VDDIO1	x1		USBC - VBOF	PEVC - PAD_EVT [7]			
	7	7	PB04	36	VDDIO1	x1/x2	SPI1 - MOSI	CANIF - RXLINE[0]	QDEC1 - QEPI		MACB - TXD[2]	
	8	8	PB05	37	VDDIO1	x1/x2	SPI1 - MISO	CANIF - TXLINE[0]	PEVC - PAD_EVT [12]	USART3 - CLK	MACB - TXD[3]	
	9	9	PB06	38	VDDIO1	x2/x4	SPI1 - SCK		QDEC1 - QEPA	USART1 - CLK	MACB - TX_ER	
		10	PB07	39	VDDIO1	x1/x2	SPI1 - NPCS[0]	EIC - EXTINT[2]	QDEC1 - QEPB		MACB - RX_DV	
		11	PB08	40	VDDIO1	x1/x2	SPI1 - NPCS[1]	PEVC - PAD_EVT [1]	PWM - PWML[0]		MACB - RXD[0]	
		12	PB09	41	VDDIO1	x1/x2	SPI1 - NPCS[2]		PWM - PWMH[0]		MACB - RXD[1]	
		13	PB10	42	VDDIO1	x1/x2	USART1 - DTR	SPI0 - MOSI	PWM - PWML[1]			



**Table 3-7.** Signal Description List

Signal Name	Function	Type	Active Level	Comments
VDDIN_5	1.8V Voltage Regulator Input	Power Input		Power Supply: 4.5V to 5.5V or 3.0V to 3.6 V
VDDIN_33	USB I/O power supply	Power Output/ Input		Capacitor Connection for the 3.3V voltage regulator or power supply: 3.0V to 3.6 V
VDDCORE	1.8V Voltage Regulator Output	Power output		Capacitor Connection for the 1.8V voltage regulator
GNDIO1 GNDIO2 GNDIO3	I/O Ground	Ground		
GNDANA	Analog Ground	Ground		
GNDCORE	Ground of the core	Ground		
GNDPLL	Ground of the PLLs	Ground		
<b>Analog Comparator Interface - ACIFA0/1</b>				
AC0AN1/AC0AN0	Negative inputs for comparator AC0A	Analog		
AC0AP1/AC0AP0	Positive inputs for comparator AC0A	Analog		
AC0BN1/AC0BN0	Negative inputs for comparator AC0B	Analog		
AC0BP1/AC0BP0	Positive inputs for comparator AC0B	Analog		
AC1AN1/AC1AN0	Negative inputs for comparator AC1A	Analog		
AC1AP1/AC1AP0	Positive inputs for comparator AC1A	Analog		
AC1BN1/AC1BN0	Negative inputs for comparator AC1B	Analog		
AC1BP1/AC1BP0	Positive inputs for comparator AC1B	Analog		
ACAOUT/ACBOUT	analog comparator outputs	output		
<b>ADC Interface - ADCIFA</b>				
ADCIN[15:0]	ADC input pins	Analog		
ADCREFO	Analog positive reference 0 voltage input	Analog		
ADCREF1	Analog positive reference 1 voltage input	Analog		
ADCVREFP	Analog positive reference connected to external capacitor	Analog		

Debug state can be entered as described in the *AVR32UC Technical Reference Manual*.

Debug state is exited by the *retd* instruction.

#### 4.4.3.3 Secure State

The AVR32 can be set in a secure state, that allows a part of the code to execute in a state with higher security levels. The rest of the code can not access resources reserved for this secure code. Secure State is used to implement FlashVault technology. Refer to the *AVR32UC Technical Reference Manual* for details.

#### 4.4.4 System Registers

The system registers are placed outside of the virtual memory space, and are only accessible using the privileged *mfsr* and *mtsr* instructions. The table below lists the system registers specified in the AVR32 architecture, some of which are unused in AVR32UC. The programmer is responsible for maintaining correct sequencing of any instructions following a *mtsr* instruction. For detail on the system registers, refer to the *AVR32UC Technical Reference Manual*.

**Table 4-3.** System Registers

Reg #	Address	Name	Function
0	0	SR	Status Register
1	4	EVBA	Exception Vector Base Address
2	8	ACBA	Application Call Base Address
3	12	CPUCR	CPU Control Register
4	16	ECR	Exception Cause Register
5	20	RSR_SUP	Unused in AVR32UC
6	24	RSR_INT0	Unused in AVR32UC
7	28	RSR_INT1	Unused in AVR32UC
8	32	RSR_INT2	Unused in AVR32UC
9	36	RSR_INT3	Unused in AVR32UC
10	40	RSR_EX	Unused in AVR32UC
11	44	RSR_NMI	Unused in AVR32UC
12	48	RSR_DBG	Return Status Register for Debug mode
13	52	RAR_SUP	Unused in AVR32UC
14	56	RAR_INT0	Unused in AVR32UC
15	60	RAR_INT1	Unused in AVR32UC
16	64	RAR_INT2	Unused in AVR32UC
17	68	RAR_INT3	Unused in AVR32UC
18	72	RAR_EX	Unused in AVR32UC
19	76	RAR_NMI	Unused in AVR32UC
20	80	RAR_DBG	Return Address Register for Debug mode
21	84	JECR	Unused in AVR32UC
22	88	JOSP	Unused in AVR32UC
23	92	JAVA_LV0	Unused in AVR32UC

**Table 4-4.** Priority and Handler Addresses for Events

Priority	Handler Address	Name	Event source	Stored Return Address
1	0x80000000	Reset	External input	Undefined
2	Provided by OCD system	OCD Stop CPU	OCD system	First non-completed instruction
3	EVBA+0x00	Unrecoverable exception	Internal	PC of offending instruction
4	EVBA+0x04	TLB multiple hit	MPU	PC of offending instruction
5	EVBA+0x08	Bus error data fetch	Data bus	First non-completed instruction
6	EVBA+0x0C	Bus error instruction fetch	Data bus	First non-completed instruction
7	EVBA+0x10	NMI	External input	First non-completed instruction
8	Autovectored	Interrupt 3 request	External input	First non-completed instruction
9	Autovectored	Interrupt 2 request	External input	First non-completed instruction
10	Autovectored	Interrupt 1 request	External input	First non-completed instruction
11	Autovectored	Interrupt 0 request	External input	First non-completed instruction
12	EVBA+0x14	Instruction Address	CPU	PC of offending instruction
13	EVBA+0x50	ITLB Miss	MPU	PC of offending instruction
14	EVBA+0x18	ITLB Protection	MPU	PC of offending instruction
15	EVBA+0x1C	Breakpoint	OCD system	First non-completed instruction
16	EVBA+0x20	Illegal Opcode	Instruction	PC of offending instruction
17	EVBA+0x24	Unimplemented instruction	Instruction	PC of offending instruction
18	EVBA+0x28	Privilege violation	Instruction	PC of offending instruction
19	EVBA+0x2C	Floating-point	UNUSED	
20	EVBA+0x30	Coprocessor absent	Instruction	PC of offending instruction
21	EVBA+0x100	Supervisor call	Instruction	PC(Supervisor Call) +2
22	EVBA+0x34	Data Address (Read)	CPU	PC of offending instruction
23	EVBA+0x38	Data Address (Write)	CPU	PC of offending instruction
24	EVBA+0x60	DTLB Miss (Read)	MPU	PC of offending instruction
25	EVBA+0x70	DTLB Miss (Write)	MPU	PC of offending instruction
26	EVBA+0x3C	DTLB Protection (Read)	MPU	PC of offending instruction
27	EVBA+0x40	DTLB Protection (Write)	MPU	PC of offending instruction
28	EVBA+0x44	DTLB Modified	UNUSED	

**Table 5-3.** Peripheral Address Mapping

0xFFFF3800	TWIM0	Two-wire Master Interface - TWIM0
0xFFFF3C00	TWIM1	Two-wire Master Interface - TWIM1
0xFFFF4000	TWIS0	Two-wire Slave Interface - TWIS0
0xFFFF4400	TWIS1	Two-wire Slave Interface - TWIS1
0xFFFF4800	IISC	Inter-IC Sound (I2S) Controller - IISC
0xFFFF4C00	PWM	Pulse Width Modulation Controller - PWM
0xFFFF5000	QDEC0	Quadrature Decoder - QDEC0
0xFFFF5400	QDEC1	Quadrature Decoder - QDEC1
0xFFFF5800	TC1	Timer/Counter - TC1
0xFFFF5C00	PEVC	Peripheral Event Controller - PEVC
0xFFFF6000	ACIFA0	Analog Comparators Interface - ACIFA0
0xFFFF6400	ACIFA1	Analog Comparators Interface - ACIFA1
0xFFFF6800	DACIFB0	DAC interface - DACIFB0
0xFFFF6C00	DACIFB1	DAC interface - DACIFB1
0xFFFF7000	AW	aWire - AW

## 5.4 CPU Local Bus Mapping

Some of the registers in the GPIO module are mapped onto the CPU local bus, in addition to being mapped on the Peripheral Bus. These registers can therefore be reached both by accesses on the Peripheral Bus, and by accesses on the local bus.

Mapping these registers on the local bus allows cycle-deterministic toggling of GPIO pins since the CPU and GPIO are the only modules connected to this bus. Also, since the local bus runs at CPU speed, one write or read operation can be performed per clock cycle to the local bus-mapped GPIO registers.



## 6. Supply and Startup Considerations

### 6.1 Supply Considerations

#### 6.1.1 Power Supplies

The AT32UC3C has several types of power supply pins:

- **VDDIO pins (VDDIO1, VDDIO2, VDDIO3):** Power I/O lines. Two voltage ranges are available: 5V or 3.3V nominal. The VDDIO pins should be connected together.
- **VDDANA:** Powers the Analog part of the device (Analog I/Os, ADC, ACs, DACs). 2 voltage ranges available: 5V or 3.3V nominal.
- **VDDIN\_5:** Input voltage for the 1.8V and 3.3V regulators. Two Voltage ranges are available: 5V or 3.3V nominal.
- **VDDIN\_33:**
  - USB I/O power supply
  - if the device is 3.3V powered: Input voltage, voltage is 3.3V nominal.
  - if the device is 5V powered: stabilization for the 3.3V voltage regulator, requires external capacitors
- **VDDCORE:** Stabilization for the 1.8V voltage regulator, requires external capacitors.
- **GNDCORE:** Ground pins for the voltage regulators and the core.
- **GNDANA:** Ground pin for Analog part of the design
- **GNDPLL:** Ground pin for the PLLs
- **GNDIO pins (GNDIO1, GNDIO2, GNDIO3):** Ground pins for the I/O lines. The GNDIO pins should be connected together.

See "[Electrical Characteristics](#)" on page 50 for power consumption on the various supply pins.

For decoupling recommendations for the different power supplies, please refer to the schematic checklist.

#### 6.1.2 Voltage Regulators

The AT32UC3C embeds two voltage regulators:

- One 1.8V internal regulator that converts from VDDIN\_5 to 1.8V. The regulator supplies the output voltage on VDDCORE.
- One 3.3V internal regulator that converts from VDDIN\_5 to 3.3V. The regulator supplies the USB pads on VDDIN\_33. If the USB is not used or if VDDIN\_5 is within the 3V range, the 3.3V regulator can be disabled through the VREG33CTL field of the VREGCTRL SCIF register.

#### 6.1.3 Regulators Connection

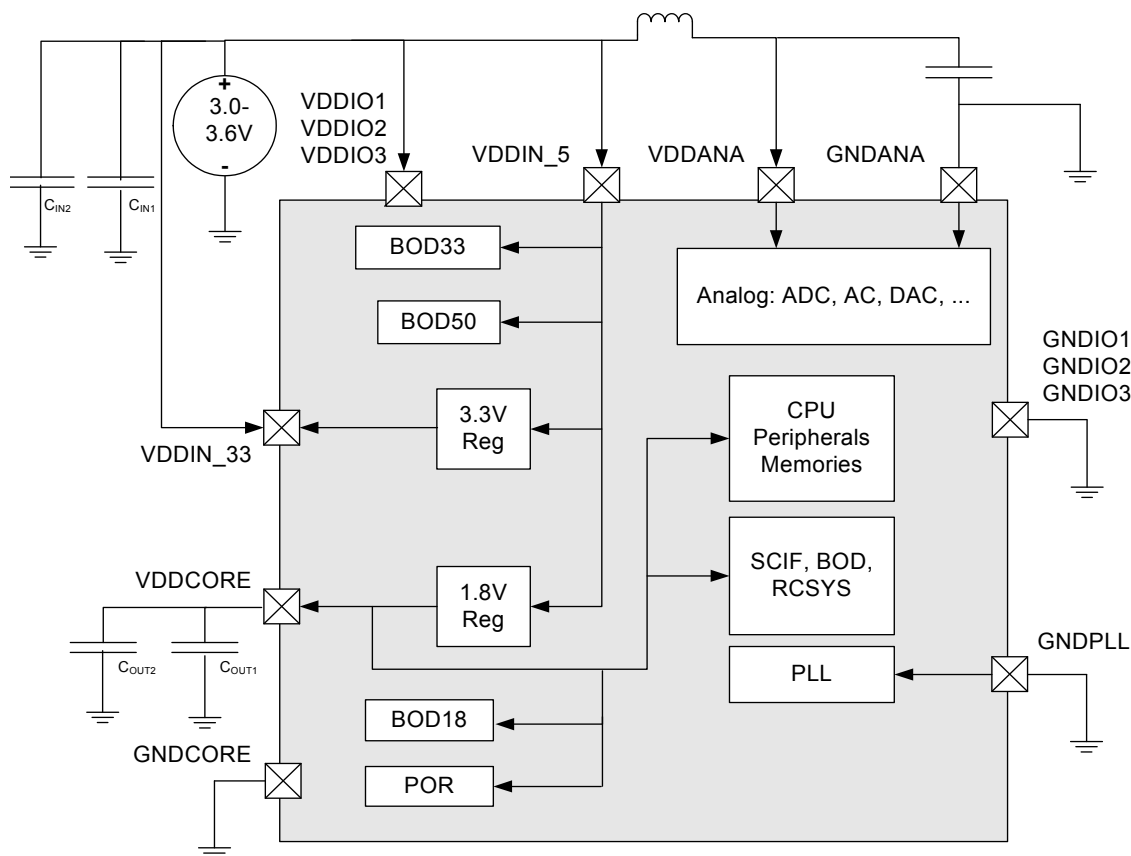
The AT32UC3C supports two power supply configurations.

- 5V single supply mode
- 3.3V single supply mode

##### 6.1.3.1 5V Single Supply Mode

In 5V single supply mode, the 1.8V internal regulator is connected to the 5V source (VDDIN\_5 pin) and its output feeds VDDCORE.

**Figure 6-2.** 3 Single Power Supply Mode



## 6.1.4 Power-up Sequence

### 6.1.4.1 Maximum Rise Rate

To avoid risk of latch-up, the rise rate of the power supplies must not exceed the values described in [Table 7-2 on page 51](#).

Recommended order for power supplies is also described in this table.

### 6.1.4.2 Minimum Rise Rate

The integrated Power-Reset circuitry monitoring the powering supply requires a minimum rise rate for the VDDIN\_5 power supply.

See [Table 7-2 on page 51](#) for the minimum rise rate value.

If the application can not ensure that the minimum rise rate condition for the VDDIN power supply is met, the following configuration can be used:

- A logic “0” value is applied during power-up on pin RESET\_N until:
  - VDDIN\_5 rises above 4.5V in 5V single supply mode.
  - VDDIN\_33 rises above 3V in 3.3V single supply mode.

- PLL1 stopped
- Clocks
  - External clock on XIN0 as main clock source.
  - CPU, HSB, and PB clocks undivided

Consumption active is the added current consumption when the module clock is turned on and when the module is doing a typical set of operations.

**Table 7-5.** Typical Current Consumption by Peripheral<sup>(2)</sup>

Peripheral	Typ Consumption Active	Unit
ACIFA <sup>(1)</sup>	3	μA/MHz
ADCIFA <sup>(1)</sup>	7	
AST	3	
CANIF	25	
DACIFB <sup>(1)</sup>	3	
EBI	23	
EIC	0.5	
FREQM	0.5	
GPIO	37	
INTC	3	
MDMA	4	
PDCA	24	
PEVC	15	
PWM	40	
QDEC	3	
SAU	3	
SDRAMC	2	
SMC	9	
SPI	5	
TC	8	
TWIM	2	
TWIS	2	
USART	10	
USBC	5	
WDT	2	

- Notes:
1. Includes the current consumption on VDDANA.
  2. These numbers are valid for the measured condition only and must not be extrapolated to other frequencies.

**Table 7-6.** Normal I/O Pin Characteristics<sup>(1)</sup>

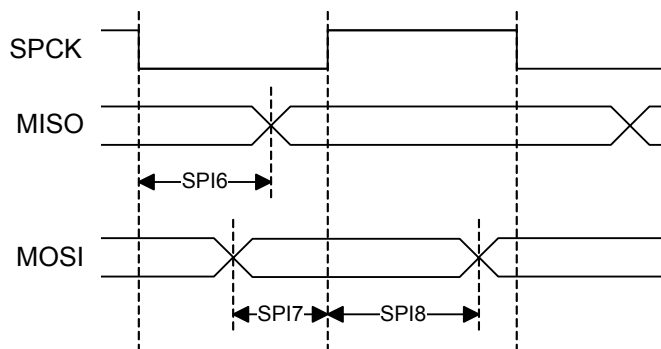
Symbol	Parameter	Condition	Min	Typ	Max	Units		
$t_{RISE}$	Rise time <sup>(3)</sup>	$V_{VDD} = 3.0V$	load = 10pF, pin drive x1 <sup>(2)</sup>			7.7	ns	
			load = 10pF, pin drive x2 <sup>(2)</sup>			3.4		
			load = 10pF, pin drive x4 <sup>(2)</sup>			1.9		
			load = 30pF, pin drive x1 <sup>(2)</sup>			16		
			load = 30pF, pin drive x2 <sup>(2)</sup>			7.5		
			load = 30pF, pin drive x4 <sup>(2)</sup>			3.8		
		$V_{VDD} = 4.5V$	load = 10pF, pin drive x1 <sup>(2)</sup>					5.3
			load = 10pF, pin drive x2 <sup>(2)</sup>					2.4
			load = 10pF, pin drive x4 <sup>(2)</sup>					1.3
			load = 30pF, pin drive x1 <sup>(2)</sup>					11.1
			load = 30pF, pin drive x2 <sup>(2)</sup>					5.2
			load = 30pF, pin drive x4 <sup>(2)</sup>					2.7
$t_{FALL}$	Fall time <sup>(3)</sup>	$V_{VDD} = 3.0V$	load = 10pF, pin drive x1 <sup>(2)</sup>			7.6	ns	
			load = 10pF, pin drive x2 <sup>(2)</sup>			3.5		
			load = 10pF, pin drive x4 <sup>(2)</sup>			1.9		
			load = 30pF, pin drive x1 <sup>(2)</sup>			15.8		
			load = 30pF, pin drive x2 <sup>(2)</sup>			7.3		
			load = 30pF, pin drive x4 <sup>(2)</sup>			3.8		
		$V_{VDD} = 4.5V$	load = 10pF, pin drive x1 <sup>(2)</sup>					5.2
			load = 10pF, pin drive x2 <sup>(2)</sup>					2.4
			load = 10pF, pin drive x4 <sup>(2)</sup>					1.4
			load = 30pF, pin drive x1 <sup>(2)</sup>					10.9
			load = 30pF, pin drive x2 <sup>(2)</sup>					5.1
			load = 30pF, pin drive x4 <sup>(2)</sup>					2.7
$I_{LEAK}$	Input leakage current	Pull-up resistors disabled			1.0	$\mu A$		
$C_{IN}$	Input capacitance	PA00-PA29, PB00-PB31, PC00-PC01, PC08-PC31, PD00-PD30		7.5		pF		
		PC02, PC03, PC04, PC05, PC06, PC07		2				

- Note:
- $V_{VDD}$  corresponds to either  $V_{VDDIO1}$ ,  $V_{VDDIO2}$ ,  $V_{VDDIO3}$ , or  $V_{VDDANA}$ , depending on the supply for the pin. Refer to [Section 3-1 on page 11](#) for details.
  - drive x1 capability pins are: PB00, PB01, PB02, PB03, PB30, PB31, PC02, PC03, PC04, PC05, PC06, PC07 - drive x2 /x4 capability pins are: PB06, PB21, PB26, PD02, PD06, PD13 - drive x1/x2 capability pins are the remaining PA, PB, PC, PD pins. The drive strength is programmable through ODCR0, ODCR0S, ODCR0C, ODCR0T registers of GPIO.
  - These values are based on simulation and characterization of other AVR microcontrollers manufactured in the same process technology. These values are not covered by test limits in production.

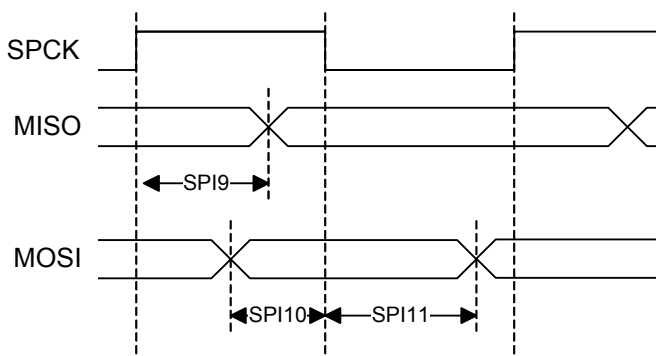


7.9.4.2 Slave mode

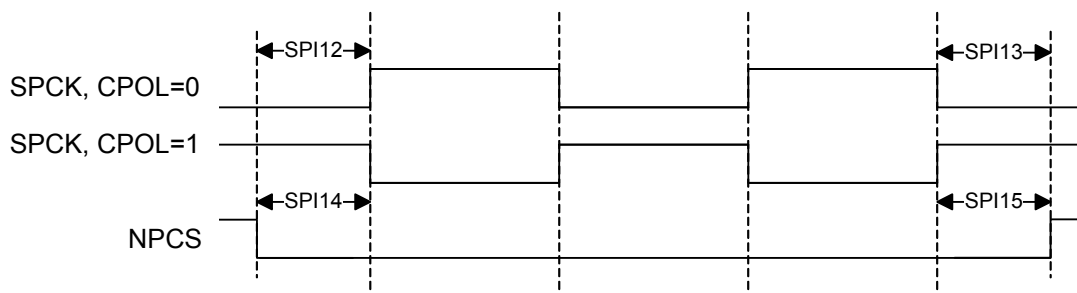
**Figure 7-13.** SPI Slave Mode With (CPOL= 0 and NCPHA= 1) or (CPOL= 1 and NCPHA= 0)



**Figure 7-14.** SPI Slave Mode With (CPOL= NCPHA= 0) or (CPOL= NCPHA= 1)



**Figure 7-15.** SPI Slave Mode NPCS Timing



**Table 7-54.** SMC Read Signals with no Hold Settings<sup>(1)</sup>

Symbol	Parameter	Conditions	Min	Units
<b>NRD Controlled (READ_MODE = 1)</b>				
SMC <sub>19</sub>	Data setup before NRD high	$V_{VDD} = 3.0V$ , drive strength of the pads set to the lowest, external capacitor = 40pF	32.5	ns
SMC <sub>20</sub>	Data hold after NRD high		0	
<b>NRD Controlled (READ_MODE = 0)</b>				
SMC <sub>21</sub>	Data setup before NCS high	$V_{VDD} = 3.0V$ , drive strength of the pads set to the lowest, external capacitor = 40pF	28.5	ns
SMC <sub>22</sub>	Data hold after NCS high		0	

Note: 1. These values are based on simulation and characterization of other AVR microcontrollers manufactured in the same process technology. These values are not covered by test limits in production.

**Table 7-55.** SMC Write Signals with Hold Settings<sup>(1)</sup>

Symbol	Parameter	Conditions	Min	Units
<b>NRD Controlled (READ_MODE = 1)</b>				
SMC <sub>23</sub>	Data Out valid before NWE high	$V_{VDD} = 3.0V$ , drive strength of the pads set to the lowest, external capacitor = 40pF	$(nwe\ pulse\ length - 1) * tcPSMC - 1.4$	ns
SMC <sub>24</sub>	Data Out valid after NWE high <sup>(2)</sup>		$nwe\ pulse\ length * tcPSMC - 4.7$	
SMC <sub>25</sub>	NWE high to NBS0/A0 change <sup>(2)</sup>		$nwe\ pulse\ length * tcPSMC - 2.7$	
SMC <sub>29</sub>	NWE high to NBS2/A1 change <sup>(2)</sup>		$nwe\ pulse\ length * tcPSMC - 0.7$	
SMC <sub>31</sub>	NWE high to A2 - A25 change <sup>(2)</sup>		$nwe\ pulse\ length * tcPSMC - 6.8$	
SMC <sub>32</sub>	NWE high to NCS inactive <sup>(2)</sup>		$(nwe\ hold\ pulse - ncs\ wr\ hold\ length) * tcPSMC - 2.5$	
SMC <sub>33</sub>	NWE pulse width		$nwe\ pulse\ length * tcPSMC - 0.2$	
<b>NRD Controlled (READ_MODE = 0)</b>				
SMC <sub>34</sub>	Data Out valid before NCS high	$V_{VDD} = 3.0V$ , drive strength of the pads set to the lowest, external capacitor = 40pF	$(ncs\ wr\ pulse\ length - 1) * tcPSMC - 2.2$	ns
SMC <sub>35</sub>	Data Out valid after NCS high <sup>(2)</sup>		$ncs\ wr\ hold\ length * tcPSMC - 5.1$	
SMC <sub>36</sub>	NCS high to NWE inactive <sup>(2)</sup>		$(ncs\ wr\ hold\ length - nwe\ hold\ length) * tcPSMC - 2$	

Note: 1. These values are based on simulation and characterization of other AVR microcontrollers manufactured in the same process technology. These values are not covered by test limits in production.

2. hold length = total cycle duration - setup duration - pulse duration. "hold length" is for "ncs wr hold length" or "nwe hold length"



Figure 7-19. SDRAMC Signals relative to SDCK.

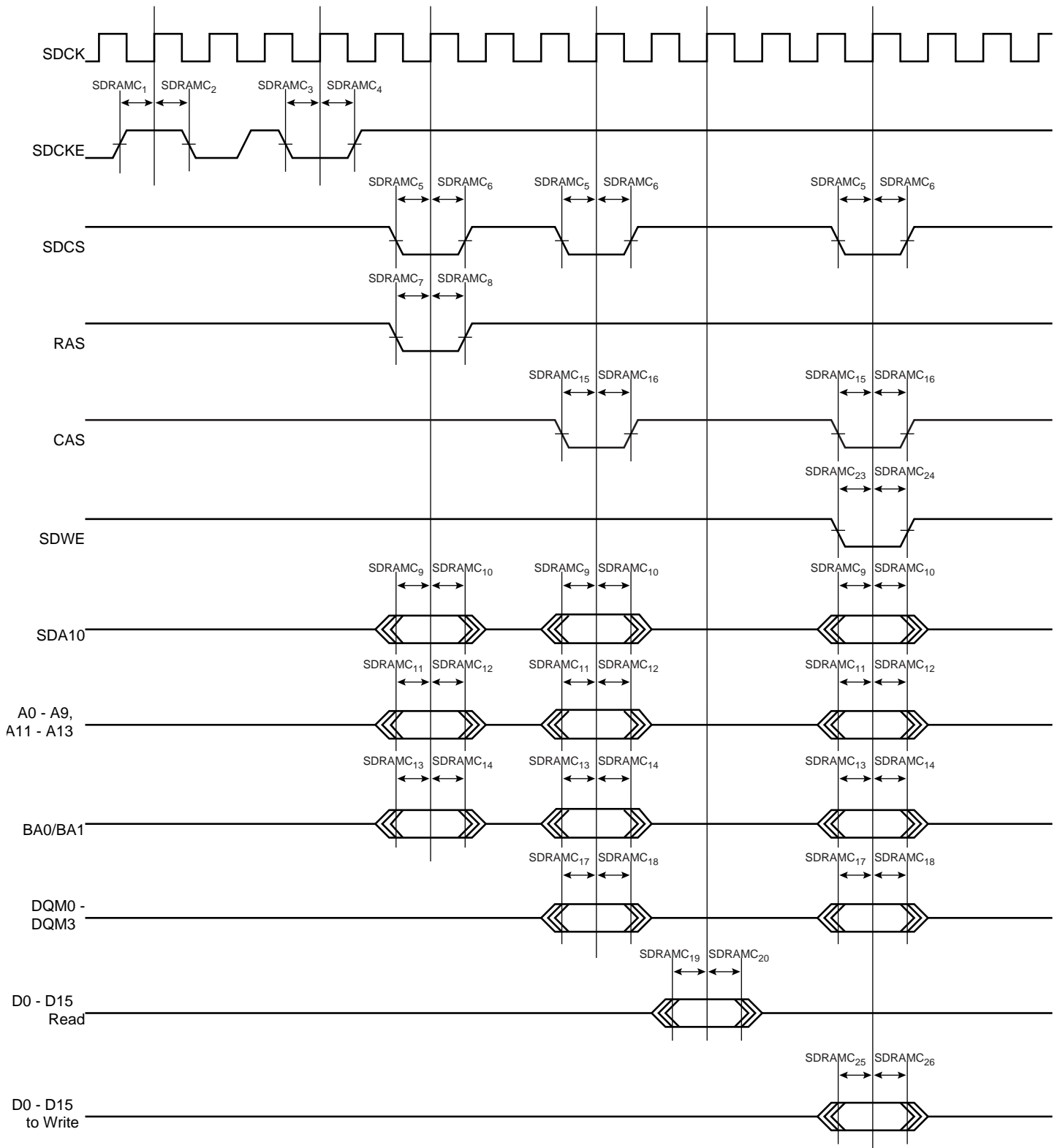
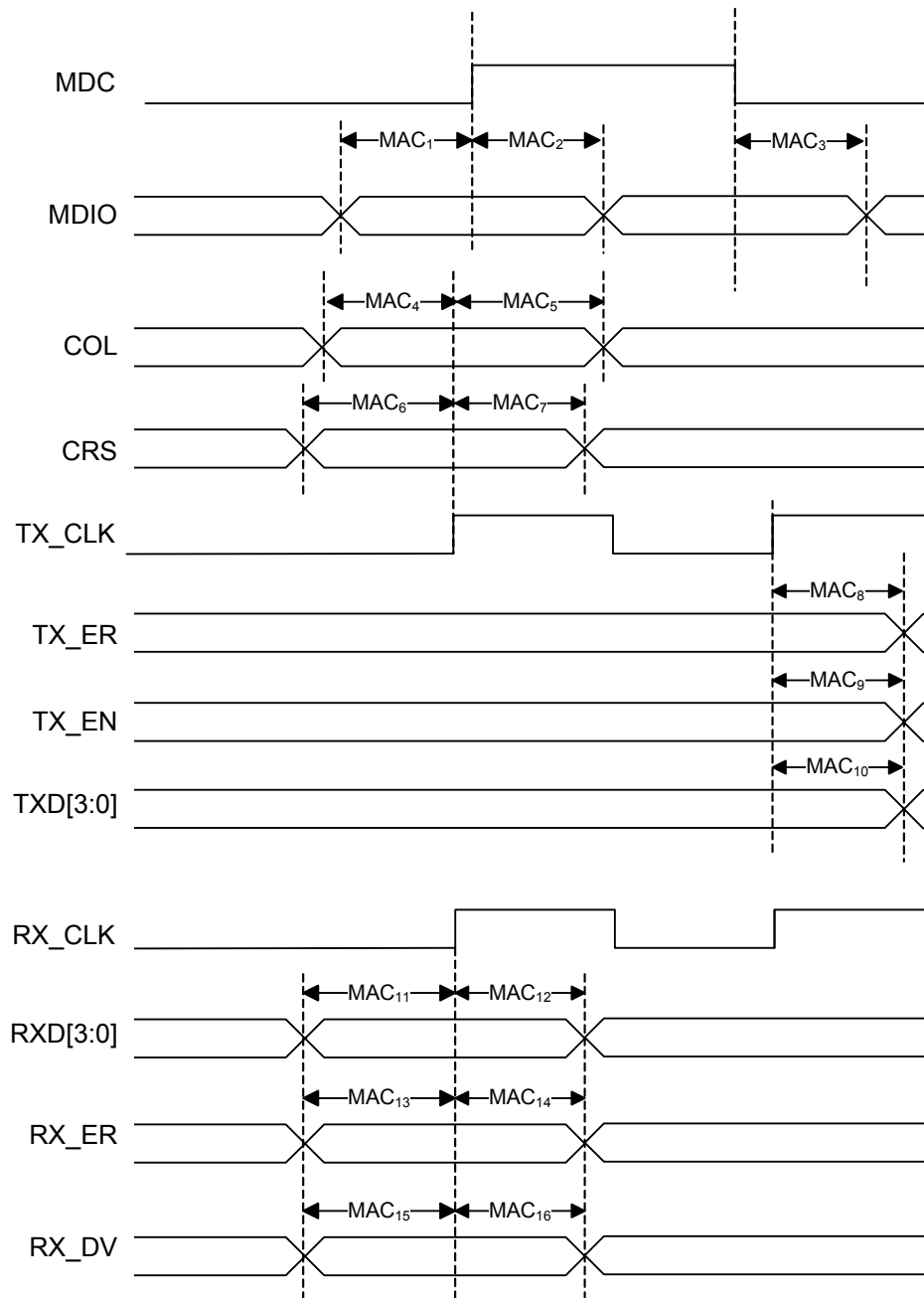


Figure 7-20. Ethernet MAC MII Mode





## 8. Mechanical Characteristics

### 8.1 Thermal Considerations

#### 8.1.1 Thermal Data

Table 8-1 summarizes the thermal resistance data depending on the package.

**Table 8-1.** Thermal Resistance Data

Symbol	Parameter	Condition	Package	Typ	Unit
$\theta_{JA}$	Junction-to-ambient thermal resistance	No air flow	QFN64	20.0	°C/W
$\theta_{JC}$	Junction-to-case thermal resistance		QFN64	0.8	
$\theta_{JA}$	Junction-to-ambient thermal resistance	No air flow	TQFP64	40.5	°C/W
$\theta_{JC}$	Junction-to-case thermal resistance		TQFP64	8.7	
$\theta_{JA}$	Junction-to-ambient thermal resistance	No air flow	TQFP100	39.3	°C/W
$\theta_{JC}$	Junction-to-case thermal resistance		TQFP100	8.5	
$\theta_{JA}$	Junction-to-ambient thermal resistance	No air flow	LQFP144	38.1	°C/W
$\theta_{JC}$	Junction-to-case thermal resistance		LQFP144	8.4	

#### 8.1.2 Junction Temperature

The average chip-junction temperature,  $T_J$ , in °C can be obtained from the following:

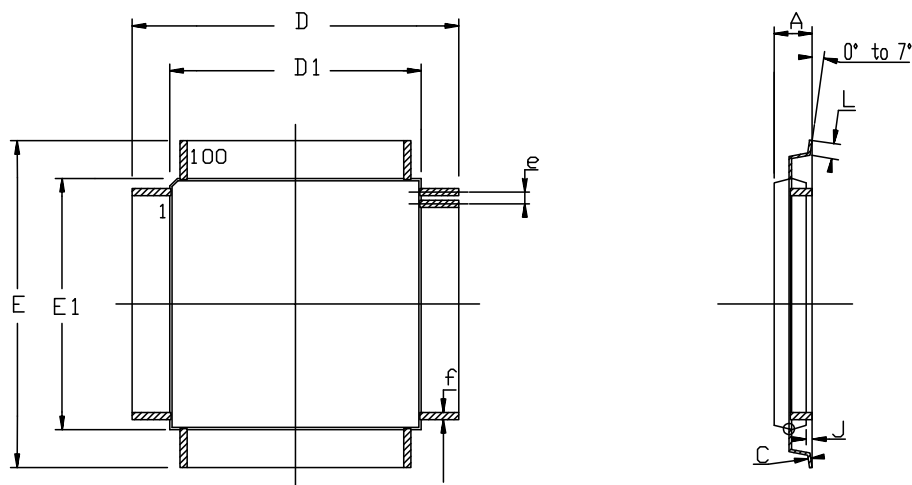
1.  $T_J = T_A + (P_D \times \theta_{JA})$
2.  $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

where:

- $\theta_{JA}$  = package thermal resistance, Junction-to-ambient (°C/W), provided in [Table 8-1 on page 90](#).
- $\theta_{JC}$  = package thermal resistance, Junction-to-case thermal resistance (°C/W), provided in [Table 8-1 on page 90](#).
- $\theta_{HEAT\ SINK}$  = cooling device thermal resistance (°C/W), provided in the device datasheet.
- $P_D$  = device power consumption (W) estimated from data provided in the section "Power Consumption" on page 51.
- $T_A$  = ambient temperature (°C).

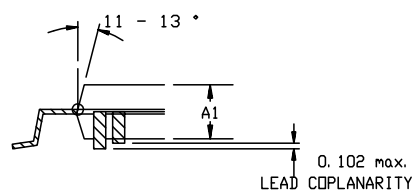
From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature  $T_J$  in °C.

**Figure 8-3.** TQFP-100 package drawing



COMMON DIMENSIONS IN MM

SYMBOL	Min	Max	NOTES
A	----	1.20	
A1	0.95	1.05	
C	0.09	0.20	
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
J	0.05	0.15	
L	0.45	0.75	
e	0.50 BSC		
f	0.17	0.27	



**Table 8-8.** Device and Package Maximum Weight

500	mg
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**Table 8-9.** Package Characteristics

Moisture Sensitivity Level	Jdec J-STD0-20D - MSL 3
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**Table 8-10.** Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

#### 4 **SPI bad serial clock generation on 2nd chip\_select when SCBR=1, CPOL=1, and NCPHA=0**

When multiple chip selects (CS) are in use, if one of the baudrates equal 1 while one (CSRn.SCBR=1) of the others do not equal 1, and CSRn.CPOL=1 and CSRn.NCPHA=0, then an additional pulse will be generated on SCK.

##### **Fix/Workaround**

When multiple CS are in use, if one of the baudrates equals 1, the others must also equal 1 if CSRn.CPOL=1 and CSRn.NCPHA=0.

### 10.1.7 TC

#### 1 **Channel chaining skips first pulse for upper channel**

When chaining two channels using the Block Mode Register, the first pulse of the clock between the channels is skipped.

##### **Fix/Workaround**

Configure the lower channel with RA = 0x1 and RC = 0x2 to produce a dummy clock cycle for the upper channel. After the dummy cycle has been generated, indicated by the SR.CPCS bit, reconfigure the RA and RC registers for the lower channel with the real values.

### 10.1.8 TWIM

#### 1 **SMBALERT bit may be set after reset**

For TWIM0 and TWIM1 modules, the SMBus Alert (SMBALERT) bit in the Status Register (SR) might be erroneously set after system reset.

##### **Fix/Workaround**

After system reset, clear the SR.SMBALERT bit before commencing any TWI transfer.

For TWIM2 module, the SMBus Alert (SMBALERT) is not implemented but the bit in the Status Register (SR) is erroneously set once TWIM2 is enabled.

##### **Fix/Workaround**

None.

### 10.1.9 TWIS

#### 1 **Clearing the NAK bit before the BTF bit is set locks up the TWI bus**

When the TWIS is in transmit mode, clearing the NAK Received (NAK) bit of the Status Register (SR) before the end of the Acknowledge/Not Acknowledge cycle will cause the TWIS to attempt to continue transmitting data, thus locking up the bus.

##### **Fix/Workaround**

Clear SR.NAK only after the Byte Transfer Finished (BTF) bit of the same register has been set.

### 10.1.10 USBC

#### 1 **UPINRQx.INRQ field is limited to 8-bits**

In Host mode, when using the UPINRQx.INRQ feature together with the multi-packet mode to launch a finite number of packet among multi-packet, the multi-packet size (located in the descriptor table) is limited to the UPINRQx.INRQ value multiply by the pipe size.

##### **Fix/Workaround**

UPINRQx.INRQ value shall be less than the number of configured multi-packet.

#### 2 **In USB host mode, downstream resume feature does not work (UHCON.RESUME=1).**

## 10.2.10 TWIS

- 1 **Clearing the NAK bit before the BTF bit is set locks up the TWI bus**  
When the TWIS is in transmit mode, clearing the NAK Received (NAK) bit of the Status Register (SR) before the end of the Acknowledge/Not Acknowledge cycle will cause the TWIS to attempt to continue transmitting data, thus locking up the bus.  
**Fix/Workaround**  
Clear SR.NAK only after the Byte Transfer Finished (BTF) bit of the same register has been set.
- 2 **TWIS stretch on Address match error**  
When the TWIS stretches TWCK due to a slave address match, it also holds TWD low for the same duration if it is to be receiving data. When TWIS releases TWCK, it releases TWD at the same time. This can cause a TWI timing violation.  
**Fix/Workaround**  
None.
- 3 **TWALM forced to GND**  
The TWALM pin is forced to GND when the alternate function is selected and the TWIS module is enabled.  
**Fix/Workaround**  
None.

## 10.2.11 USBC

- 1 **UPINRQx.INRQ field is limited to 8-bits**  
In Host mode, when using the UPINRQx.INRQ feature together with the multi-packet mode to launch a finite number of packet among multi-packet, the multi-packet size (located in the descriptor table) is limited to the UPINRQx.INRQ value multiply by the pipe size.  
**Fix/Workaround**  
UPINRQx.INRQ value shall be less than the number of configured multi-packet.
- 2 **In USB host mode, downstream resume feature does not work (UHCON.RESUME=1).**  
**Fix/Workaround**  
None.
- 3 **In host mode, the disconnection during OUT transition is not supported**  
In USB host mode, a pipe can not work if the previous USB device disconnection has occurred during a USB transfer.  
**Fix/Workaround**  
Reset the USBC (USBCON.USB=0 and =1) after a device disconnection (UHINT.DDISCI).
- 4 **In USB host mode, entering suspend mode can fail**  
In USB host mode, entering suspend mode can fail when UHCON.SOFE=0 is done just after a SOF reception (UHINT.HSOFI).  
**Fix/Workaround**  
Check that UHNUM.FLENHIGH is below 185 in Full speed and below 21 in Low speed before clearing UHCON.SOFE.
- 5 **In USB host mode, entering suspend mode for low speed device can fail when the USB freeze (USBCON.FRZCLK=1) is done just after UHCON.SOFE=0.**  
**Fix/Workaround**  
When entering suspend mode (UHCON.SOFE is cleared), check that USBFSM.DRDSTATE is not equal to three before freezing the clock (USBCON.FRZCLK=1).

- 5 AST: Updated digital tuner formula
- 6 SDRAMC: cleaned-up SDCS/NCS names. Added VERSION register
- 7 SAU: Updated SR.IDLE
- 8 USART: Updated
- 9 CANIF: Updated address map figure
- 10 USBC: Updated
- 11 DACIFB: Updated
- 12 Programming and Debugging: Added JTAG Data Registers section
- 13 Electrical Characteristics: Updated
- 14 Ordering Information: Updated
- 15 Errata: Updated

#### **11.4 Rev. A – 10/10**

- 1 Initial revision