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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | AVR |
| Core Size | 32-Bit Single-Core |
| Speed | 66MHz |
| Connectivity | CANbus, Ethernet, I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 45 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 11x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-TQFP |
| Supplier Device Package | 64-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/at32uc3c2512c-a2ur |

## 2.2 Configuration Summary

**Table 2-1.** Configuration Summary

| Feature | AT32UC3C0512C/ AT32UC3C0256C/ AT32UC3C0128C/ AT32UC3C064C | AT32UC3C1512C/ AT32UC3C1256C/ AT32UC3C1128C/ AT32UC3C164C | AT32UC3C2512C/ AT32UC3C2256C/ AT32UC3C2128C/ AT32UC3C264C |
|---|---|---|---|
| Flash | 512/256/128/64 KB | 512/256/128/64 KB | 512/256/128/64 KB |
| SRAM | 64/64/32/16 KB | 64/64/32/16 KB | 64/64/32/16 KB |
| HSB RAM | 4 KB | | |
| EBI | 1 | 0 | 0 |
| GPIO | 123 | 81 | 45 |
| External Interrupts | 8 | 8 | 8 |
| TWI | 3 | 3 | 2 |
| USART | 5 | 5 | 4 |
| Peripheral DMA Channels | 16 | 16 | 16 |
| Peripheral Event System | 1 | 1 | 1 |
| SPI | 2 | 2 | 1 |
| CAN channels | 2 | 2 | 2 |
| USB | 1 | 1 | 1 |
| Ethernet MAC 10/100 | 1<br>RMII/MII | 1<br>RMII/MII | 1<br>RMII only |
| I2S | 1 | 1 | 1 |
| Asynchronous Timers | 1 | 1 | 1 |
| Timer/Counter Channels | 6 | 6 | 3 |
| PWM channels | 4x2 | | |
| QDEC | 2 | 2 | 1 |
| Frequency Meter | 1 | | |
| Watchdog Timer | 1 | | |
| Power Manager | 1 | | |
| Oscillators | PLL 80-240 MHz (PLL0/PLL1)<br>Crystal Oscillator 0.4-20 MHz (OSC0)<br>Crystal Oscillator 32 KHz (OSC32K)<br>RC Oscillator 115 kHz (RCSYS)<br>RC Oscillator 8 MHz (RC8M)<br>RC Oscillator 120 MHz (RC120M) | | |
| | 0.4-20 MHz (OSC1) | | - |
| 12-bit ADC<br>number of channels | 1<br>16 | 1<br>16 | 1<br>11 |
| 12-bit DAC<br>number of channels | 1<br>4 | 1<br>4 | 1<br>2 |

**Table 3-1.** GPIO Controller Function Multiplexing

| TQFP / QFN 64 | TQFP 100 | LQFP 144 | PIN | GPIO | Supply | Pin Type (1) | GPIO function | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | A | B | C | D | E | F |
| | | 14 | PB11 | 43 | VDDIO1 | x1/x2 | USART1 - DSR | SPI0 - MISO | PWM - PWMH[1] | | | |
| | | 15 | PB12 | 44 | VDDIO1 | x1/x2 | USART1 - DCD | SPI0 - SCK | PWM - PWML[2] | | | |
| | | 16 | PB13 | 45 | VDDIO1 | x1/x2 | USART1 - RI | SPI0 - NPCS[0] | PWM - PWMH[2] | | MACB - RX_ER | |
| | | 17 | PB14 | 46 | VDDIO1 | x1/x2 | USART1 - RTS | SPI0 - NPCS[1] | PWM - PWML[3] | | MACB - MDC | |
| | | 18 | PB15 | 47 | VDDIO1 | x1/x2 | USART1 - CTS | USART1 - CLK | PWM - PWMH[3] | | MACB - MDIO | |
| | | 19 | PB16 | 48 | VDDIO1 | x1/x2 | USART1 - RXD | SPI0 - NPCS[2] | PWM - EXT_ FAULTS[0] | | CANIF - RXLINE[0] | |
| | | 20 | PB17 | 49 | VDDIO1 | x1/x2 | USART1 - TXD | SPI0 - NPCS[3] | PWM - EXT_ FAULTS[1] | | CANIF - TXLINE[0] | |
| | | 57 | PB18 | 50 | VDDIO2 | x1/x2 | TC0 - CLK2 | | EIC - EXTINT[4] | | | |
| | 42 | 58 | PB19 | 51 | VDDIO2 | x1/x2 | TC0 - A0 | SPI1 - MOSI | IISC - ISDO | | MACB - CRS | |
| | 43 | 59 | PB20 | 52 | VDDIO2 | x1/x2 | TC0 - B0 | SPI1 - MISO | IISC - ISDI | ACIFA1 - ACAOUT | MACB - COL | |
| | 44 | 60 | PB21 | 53 | VDDIO2 | x2/x4 | TC0 - CLK1 | SPI1 - SCK | IISC - IMCK | ACIFA1 - ACBOUT | MACB - RXD[2] | |
| | 45 | 61 | PB22 | 54 | VDDIO2 | x1/x2 | TC0 - A1 | SPI1 - NPCS[3] | IISC - ISCK | SCIF - GCLK[0] | MACB - RXD[3] | |
| | 46 | 62 | PB23 | 55 | VDDIO2 | x1/x2 | TC0 - B1 | SPI1 - NPCS[2] | IISC - IWS | SCIF - GCLK[1] | MACB - RX_CLK | |
| | | 63 | PB24 | 56 | VDDIO2 | x1/x2 | TC0 - CLK0 | SPI1 - NPCS[1] | | | | |
| | | 64 | PB25 | 57 | VDDIO2 | x1/x2 | TC0 - A2 | SPI1 - NPCS[0] | PEVC - PAD_EVT [8] | | | |
| | | 65 | PB26 | 58 | VDDIO2 | x2/x4 | TC0 - B2 | SPI1 - SCK | PEVC - PAD_EVT [9] | | MACB - TX_EN | |
| | | 66 | PB27 | 59 | VDDIO2 | x1/x2 | QDEC0 - QEPA | SPI1 - MISO | PEVC - PAD_EVT [10] | TC1 - CLK0 | MACB - TXD[0] | |
| | | 67 | PB28 | 60 | VDDIO2 | x1/x2 | QDEC0 - QEPB | SPI1 - MOSI | PEVC - PAD_EVT [11] | TC1 - B0 | MACB - TXD[1] | |
| | | 68 | PB29 | 61 | VDDIO2 | x1/x2 | QDEC0 - QEPI | SPI0 - NPCS[0] | PEVC - PAD_EVT [12] | TC1 - A0 | | |
| 31 | 47 | 69 | PB30 | 62 | VDDIO2 | x1 | | | | | | |
| 32 | 48 | 70 | PB31 | 63 | VDDIO2 | x1 | | | | | | |
| | 49 | 71 | PC00 | 64 | VDDIO2 | x1/x2 | USBC - ID | SPI0 - NPCS[1] | USART2 - CTS | TC1 - B2 | CANIF - TXLINE[1] | |
| | 50 | 72 | PC01 | 65 | VDDIO2 | x1/x2 | USBC - VBOF | SPI0 - NPCS[2] | USART2 - RTS | TC1 - A2 | CANIF - RXLINE[1] | |

depending on the configuration of the OCD AXS register. For details, see the AVR32UC Technical Reference Manual.

**Table 3-5.** Nexus OCD AUX port connections

| Pin | AXS=0 | AXS=1 | AXS=2 |
|---|---|---|---|
| EVTI_N | PA08 | PB19 | PA10 |
| MDO[5] | PC05 | PC31 | PB06 |
| MDO[4] | PC04 | PC12 | PB15 |
| MDO[3] | PA23 | PC11 | PB14 |
| MDO[2] | PA22 | PB23 | PA27 |
| MDO[1] | PA19 | PB22 | PA26 |
| MDO[0] | PA09 | PB20 | PA19 |
| EVTO_N | PD29 | PD29 | PD29 |
| MCKO | PD13 | PB21 | PB26 |
| MSEO[1] | PD30 | PD08 | PB25 |
| MSEO[0] | PD14 | PD07 | PB18 |

### 3.2.6 Other Functions

The functions listed in Table 3-6 are not mapped to the normal GPIO functions. The aWire DATA pin will only be active after the aWire is enabled. The aWire DATAOUT pin will only be active after the aWire is enabled and the 2_PIN_MODE command has been sent.

**Table 3-6.** Other Functions

| QFN64/ TQFP64 pin | TQFP100 pin | LQFP144 pin | Pad | Oscillator pin |
|---|---|---|---|---|
| 64 | 98 | 142 | RESET_N | aWire DATA |
| 3 | 3 | 3 | PA02 | aWire DATAOUT |

## 3.3 Signals Description

The following table give details on the signal name classified by peripherals.

**Table 3-7.** Signal Description List

| Signal Name | Function | Type | Active Level | Comments |
|---|---|---|---|---|
| **Power** | | | | |
| VDDIO1<br>VDDIO2<br>VDDIO3 | I/O Power Supply | Power Input | | 4.5V to 5.5V<br>or<br>3.0V to 3.6 V |
| VDDANA | Analog Power Supply | Power Input | | 4.5V to 5.5V<br>or<br>3.0V to 3.6 V |

**Table 3-7.** Signal Description List

| Signal Name | Function | Type | Active Level | Comments |
|---|---|---|---|---|
| VDDIN_5 | 1.8V Voltage Regulator Input | Power Input | | Power Supply:<br>4.5V to 5.5V<br>or<br>3.0V to 3.6 V |
| VDDIN_33 | USB I/O power supply | Power Output/ Input | | Capacitor Connection for the 3.3V voltage regulator<br>or power supply:<br>3.0V to 3.6 V |
| VDDCORE | 1.8V Voltage Regulator Output | Power output | | Capacitor Connection for the 1.8V voltage regulator |
| GNDIO1<br>GNDIO2<br>GNDIO3 | I/O Ground | Ground | | |
| GNDANA | Analog Ground | Ground | | |
| GNDCORE | Ground of the core | Ground | | |
| GNDPLL | Ground of the PLLs | Ground | | |
| **Analog Comparator Interface - ACIFA0/1** | | | | |
| AC0AN1/AC0AN0 | Negative inputs for comparator AC0A | Analog | | |
| AC0AP1/AC0AP0 | Positive inputs for comparator AC0A | Analog | | |
| AC0BN1/AC0BN0 | Negative inputs for comparator AC0B | Analog | | |
| AC0BP1/AC0BP0 | Positive inputs for comparator AC0B | Analog | | |
| AC1AN1/AC1AN0 | Negative inputs for comparator AC1A | Analog | | |
| AC1AP1/AC1AP0 | Positive inputs for comparator AC1A | Analog | | |
| AC1BN1/AC1BN0 | Negative inputs for comparator AC1B | Analog | | |
| AC1BP1/AC1BP0 | Positive inputs for comparator AC1B | Analog | | |
| ACAOUT/ACBOUT | analog comparator outputs | output | | |
| **ADC Interface - ADCIFA** | | | | |
| ADCIN[15:0] | ADC input pins | Analog | | |
| ADCREF0 | Analog positive reference 0 voltage input | Analog | | |
| ADCREF1 | Analog positive reference 1 voltage input | Analog | | |
| ADCVREFP | Analog positive reference connected to external capacitor | Analog | | |

**Table 3-7.** Signal Description List

| Signal Name | Function | Type | Active Level | Comments |
|---|---|---|---|---|
| DP | USB Device Port Data + | Analog | | |
| VBUS | USB VBUS Monitor and OTG Negociation | Analog Input | | |
| ID | ID Pin of the USB Bus | Input | | |
| VBOF | USB VBUS On/off: bus power control port | output | | |

## 3.4 I/O Line Considerations

### 3.4.1 JTAG pins

The JTAG is enabled if TCK is low while the RESET_N pin is released. The TCK, TMS, and TDI pins have pull-up resistors when JTAG is enabled. The TCK pin always have pull-up enabled during reset. The TDO pin is an output, driven at VDDIO1, and has no pull-up resistor. The JTAG pins can be used as GPIO pins and muxed with peripherals when the JTAG is disabled. Please refer to Section 3.2.4 for the JTAG port connections.

### 3.4.2 RESET_N pin

The RESET_N pin integrates a pull-up resistor to VDDIO1. As the product integrates a power-on reset cell, the RESET_N pin can be left unconnected in case no reset from the system needs to be applied to the product.

The RESET_N pin is also used for the aWire debug protocol. When the pin is used for debugging, it must not be driven by external circuitry.

### 3.4.3 TWI pins

When these pins are used for TWI, the pins are open-drain outputs with slew-rate limitation and inputs with inputs with spike-filtering. When used as GPIO-pins or used for other peripherals, the pins have the same characteristics as GPIO pins.

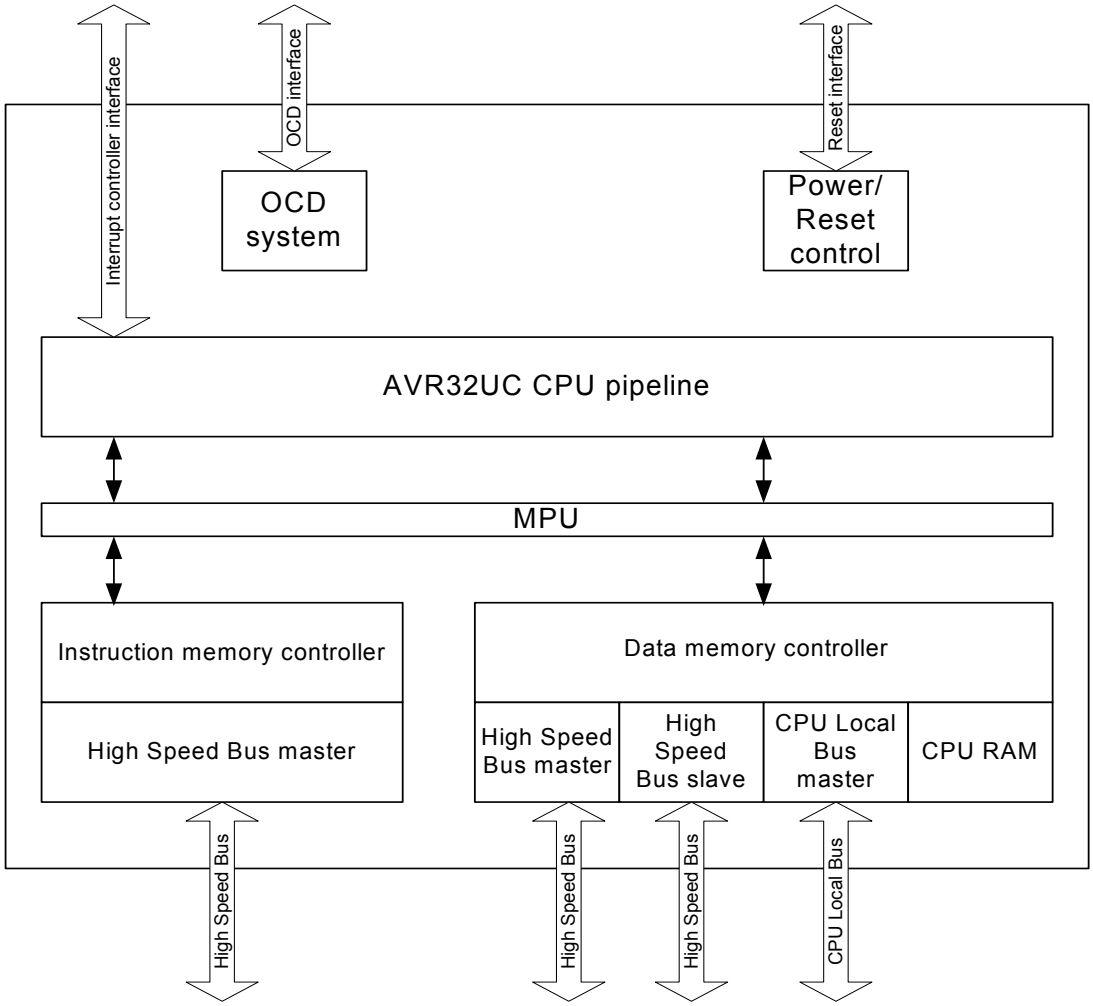
### 3.4.4 GPIO pins

All I/O lines integrate programmable pull-up and pull-down resistors. Most I/O lines integrate drive strength control, see Table 3-1. Programming of this pull-up and pull-down resistor or this drive strength is performed independently for each I/O line through the GPIO Controllers.

After reset, I/O lines default as inputs with pull-up/pull-down resistors disabled. After reset, output drive strength is configured to the lowest value to reduce global EMI of the device.

When the I/O line is configured as analog function (ADC I/O, AC inputs, DAC I/O), the pull-up and pull-down resistors are automatically disabled.

**Figure 4-1.** Overview of the AVR32UC CPU




### 4.3.1 Pipeline Overview

AVR32UC has three pipeline stages, Instruction Fetch (IF), Instruction Decode (ID), and Instruction Execute (EX). The EX stage is split into three parallel subsections, one arithmetic/logic (ALU) section, one multiply (MUL) section, and one load/store (LS) section.

Instructions are issued and complete in order. Certain operations require several clock cycles to complete, and in this case, the instruction resides in the ID and EX stages for the required number of clock cycles. Since there is only three pipeline stages, no internal data forwarding is required, and no data dependencies can arise in the pipeline.

Figure 4-2 on page 28 shows an overview of the AVR32UC pipeline stages.

**Table 4-3.** System Registers (Continued)

| Reg # | Address | Name | Function |
|---|---|---|---|
| 90 | 360 | MPUPSR2 | MPU Privilege Select Register region 2 |
| 91 | 364 | MPUPSR3 | MPU Privilege Select Register region 3 |
| 92 | 368 | MPUPSR4 | MPU Privilege Select Register region 4 |
| 93 | 372 | MPUPSR5 | MPU Privilege Select Register region 5 |
| 94 | 376 | MPUPSR6 | MPU Privilege Select Register region 6 |
| 95 | 380 | MPUPSR7 | MPU Privilege Select Register region 7 |
| 96 | 384 | MPUCRA | Unused in this version of AVR32UC |
| 97 | 388 | MPUCRB | Unused in this version of AVR32UC |
| 98 | 392 | MPUBRA | Unused in this version of AVR32UC |
| 99 | 396 | MPUBRB | Unused in this version of AVR32UC |
| 100 | 400 | MPUAPRA | MPU Access Permission Register A |
| 101 | 404 | MPUAPRB | MPU Access Permission Register B |
| 102 | 408 | MPUCR | MPU Control Register |
| 103 | 412 | SS_STATUS | Secure State Status Register |
| 104 | 416 | SS_ADRF | Secure State Address Flash Register |
| 105 | 420 | SS_ADRR | Secure State Address RAM Register |
| 106 | 424 | SS_ADR0 | Secure State Address 0 Register |
| 107 | 428 | SS_ADR1 | Secure State Address 1 Register |
| 108 | 432 | SS_SP_SYS | Secure State Stack Pointer System Register |
| 109 | 436 | SS_SP_APP | Secure State Stack Pointer Application Register |
| 110 | 440 | SS_RAR | Secure State Return Address Register |
| 111 | 444 | SS_RSR | Secure State Return Status Register |
| 112-191 | 448-764 | Reserved | Reserved for future use |
| 192-255 | 768-1020 | IMPL | IMPLEMENTATION DEFINED |

## 4.5 Exceptions and Interrupts

In the AVR32 architecture, events are used as a common term for exceptions and interrupts. AVR32UC incorporates a powerful event handling scheme. The different event sources, like Illegal Op-code and interrupt requests, have different priority levels, ensuring a well-defined behavior when multiple events are received simultaneously. Additionally, pending events of a higher priority class may preempt handling of ongoing events of a lower priority class.

When an event occurs, the execution of the instruction stream is halted, and execution is passed to an event handler at an address specified in Table 4-4 on page 38. Most of the handlers are placed sequentially in the code space starting at the address specified by EVBA, with four bytes between each handler. This gives ample space for a jump instruction to be placed there, jumping to the event routine itself. A few critical handlers have larger spacing between them, allowing the entire event routine to be placed directly at the address specified by the EVBA-relative offset generated by hardware. All interrupt sources have autovectored interrupt service routine (ISR) addresses. This allows the interrupt controller to directly specify the ISR address as an address

than the oldest instruction. An instruction B is younger than an instruction A if it was sent down the pipeline later than A.

The addresses and priority of simultaneous events are shown in Table 4-4 on page 38. Some of the exceptions are unused in AVR32UC since it has no MMU, coprocessor interface, or floating-point unit.

**Table 5-4.** Local bus mapped GPIO registers

| Port | Register | Mode | Local Bus Address | Access |
|---|---|---|---|---|
| D | Output Driver Enable Register (ODER) | WRITE | 0x40000340 | Write-only |
| | | SET | 0x40000344 | Write-only |
| | | CLEAR | 0x40000348 | Write-only |
| | | TOGGLE | 0x4000034C | Write-only |
| | Output Value Register (OVR) | WRITE | 0x40000350 | Write-only |
| | | SET | 0x40000354 | Write-only |
| | | CLEAR | 0x40000358 | Write-only |
| | | TOGGLE | 0x4000035C | Write-only |
| | Pin Value Register (PVR) | - | 0x40000360 | Read-only |

# 7. Electrical Characteristics

## 7.1 Absolute Maximum Ratings*

| | |
|---|---|
| Operating temperature | -40°C to +85°C |
| Storage temperature | -60°C to +150°C |
| Voltage on any pin except DM/DP/VBUS with respect to ground | -0.3V to $V_{VDD}$[1]+0.3V |
| Voltage on DM/DP with respect to ground | -0.3V to +3.6V |
| Voltage on VBUS with respect to ground | -0.3V to +5.5V |
| Maximum operating voltage (VDDIN_5) | 5.5V |
| Maximum operating voltage (VDDIO1, VDDIO2, VDDIO3, VDDANA) | 5.5V |
| Maximum operating voltage (VDDIN_33) | 3.6V |
| Total DC output current on all I/O pins- VDDIO1 | 120 mA |
| Total DC output current on all I/O pins- VDDIO2 | 120 mA |
| Total DC output current on all I/O pins- VDDIO3 | 120 mA |
| Total DC output current on all I/O pins- VDDANA | 120 mA |

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes: 1. $V_{VDD}$ corresponds to either $V_{VDDIO1}$, $V_{VDDIO2}$, $V_{VDDIO3}$, or $V_{VDDANA}$, depending on the supply for the pin. Refer to Section 3-1 on page 11 for details.

## 7.2 Supply Characteristics

The following characteristics are applicable to the operating temperature range: $T_A$ = -40°C to 85°C, unless otherwise specified and are valid for a junction temperature up to $T_J$ = 100°C. Please refer to Section 6. ”Supply and Startup Considerations” on page 46.

**Table 7-1.** Supply Characteristics

| Symbol | Parameter | Condition | Voltage | | |
|---|---|---|---|---|---|
| | | | Min | Max | Unit |
| $V_{VDDIN\_5}$ | DC supply internal regulators | 3V range | 3.0 | 3.6 | V |
| | | 5V range | 4.5 | 5.5 | |
| $V_{VDDIN\_33}$ | DC supply USB I/O | only in 3V range | 3.0 | 3.6 | V |
| $V_{VDDANA}$ | DC supply peripheral I/O and analog part | 3V range | 3.0 | 3.6 | V |
| | | 5V range | 4.5 | 5.5 | |
| $V_{VDDIO1}$ $V_{VDDIO2}$ $V_{VDDIO2}$ | DC supply peripheral I/O | 3V range | 3.0 | 3.6 | V |
| | | 5V range | 4.5 | 5.5 | |

  - PLL1 stopped
- Clocks
  - External clock on XIN0 as main clock source.
  - CPU, HSB, and PB clocks undivided

Consumption active is the added current consumption when the module clock is turned on and when the module is doing a typical set of operations.

**Table 7-5.** Typical Current Consumption by Peripheral[2]

| Peripheral | Typ Consumption Active | Unit |
|---|---|---|
| ACIFA[1] | 3 | µA/MHz |
| ADCIFA[1] | 7 | |
| AST | 3 | |
| CANIF | 25 | |
| DACIFB[1] | 3 | |
| EBI | 23 | |
| EIC | 0.5 | |
| FREQM | 0.5 | |
| GPIO | 37 | |
| INTC | 3 | |
| MDMA | 4 | |
| PDCA | 24 | |
| PEVC | 15 | |
| PWM | 40 | |
| QDEC | 3 | |
| SAU | 3 | |
| SDRAMC | 2 | |
| SMC | 9 | |
| SPI | 5 | |
| TC | 8 | |
| TWIM | 2 | |
| TWIS | 2 | |
| USART | 10 | |
| USBC | 5 | |
| WDT | 2 | |

Notes: 1. Includes the current consumption on VDDANA.
2. These numbers are valid for the measured condition only and must not be extrapolated to other frequencies.

### 7.8.6 Analog to Digital Converter (ADC) and sample and hold (S/H) Characteristics

**Table 7-27.** ADC and S/H characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{ADC}$ | ADC clock frequency | 12-bit resolution mode, $V_{VDDANA}$ = 3V | | | 1.2 | MHz |
| | | 10-bit resolution mode, $V_{VDDANA}$ = 3V | | | 1.6 | |
| | | 8-bit resolution mode, $V_{VDDANA}$ = 3V | | | 2.2 | |
| | | 12-bit resolution mode, $V_{VDDANA}$ = 4.5V | | | 1.5 | |
| | | 10-bit resolution mode, $V_{VDDANA}$ = 4.5V | | | 2 | |
| | | 8-bit resolution mode, $V_{VDDANA}$ = 4.5V | | | 2.4 | |
| $t_{STARTUP}$ | Startup time | ADC cold start-up | | | 1 | ms |
| | | ADC hot start-up | | | 24 | ADC clock cycles |
| $t_{CONV}$ | Conversion time (latency) | (ADCIFA.SEQCFGn.SRES)/2 + 2, ADCIFA.CFG.SHD = 1 | 6 | | 8 | ADC clock cycles |
| | | (ADCIFA.SEQCFGn.SRES)/2 + 3, ADCIFA.CFG.SHD = 0 | 7 | | 9 | |
| | Throughput rate | 12-bit resolution, ADC clock = 1.2 MHz, $V_{VDDANA}$ = 3V | | | 1.2 | MSPS |
| | | 10-bit resolution, ADC clock = 1.6 MHz, $V_{VDDANA}$ = 3V | | | 1.6 | |
| | | 12-bit resolution, ADC clock = 1.5 MHz, $V_{VDDANA}$ = 4.5V | | | 1.5 | |
| | | 10-bit resolution, ADC clock = 2 MHz, $V_{VDDANA}$ = 4.5V | | | 2 | |

**Table 7-28.** ADC Reference Voltage

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{ADCREF0}$ | ADCREF0 input voltage range | 5V Range | 1 | | 3.5 | V |
| | | 3V Range | 1 | | $V_{VDDANA}$-0.7 | |
| $V_{ADCREF1}$ | ADCREF1 input voltage range | 5V Range | 1 | | 3.5 | V |
| | | 3V Range | 1 | | $V_{VDDANA}$-0.7 | |
| $V_{ADCREFP}$ | ADCREFP input voltage | 5V Range - Voltage reference applied on ADCREFP | 1 | | 3.5 | V |
| | | 3V Range - Voltage reference applied on ADCREFP | 1 | | $V_{VDDANA}$-0.7 | |
| $V_{ADCREFN}$ | ADCREFN input voltage | Voltage reference applied on ADCREFN | | GNDANA | | V |
| | Internal 1V reference | | | 1.0 | | V |
| | Internal 0.6*VDDANA reference | | | 0.6*$V_{VDDANA}$ | | V |

### 7.9.3 USART in SPI Mode Timing

#### *7.9.3.1 Master mode*

**Figure 7-6.** USART in SPI Master Mode With (CPOL= CPHA= 0) or (CPOL= CPHA= 1)

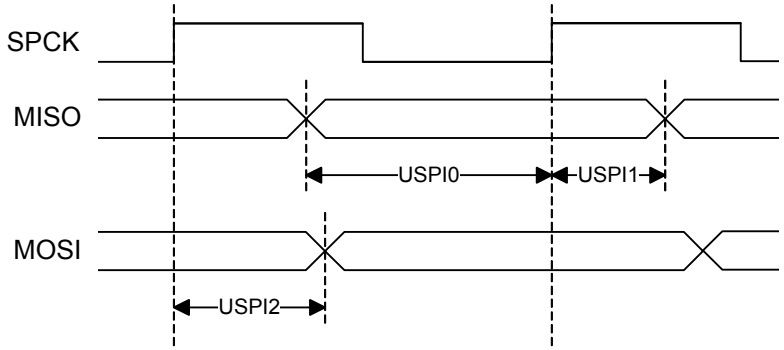



**Figure 7-7.** USART in SPI Master Mode With (CPOL= 0 and CPHA= 1) or (CPOL= 1 and CPHA= 0)

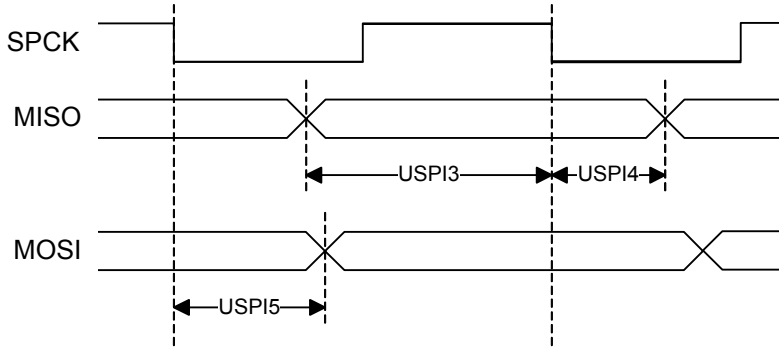



**Table 7-46.** USART in SPI Mode Timing, Master Mode[1]

| Symbol | Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| USPI0 | MISO setup time before SPCK rises | external capacitor = 40pF | 26+ $t_{SAMPLE}$[2] | | ns |
| USPI1 | MISO hold time after SPCK rises | | 0 | | ns |
| USPI2 | SPCK rising to MOSI delay | | | 11 | ns |
| USPI3 | MISO setup time before SPCK falls | | 26+ $t_{SAMPLE}$[2] | | ns |
| USPI4 | MISO hold time after SPCK falls | | 0 | | ns |
| USPI5 | SPCK falling to MOSI delay | | | 11.5 | ns |

Note: 1. These values are based on simulation and characterization of other AVR microcontrollers manufactured in the same process technology. These values are not covered by test limits in production.

2. Where: $t_{SAMPLE} = t_{SPCK} - \left( \left\lfloor \frac{t_{SPCK}}{2 \times t_{CLKUSART}} \right\rfloor \frac{1}{2} \right) \times t_{CLKUSART}$

**Maximum SPI Frequency, Master Output**

The maximum SPI master output frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(f_{PINMAX}, \frac{1}{SPIn}, \frac{f_{CLKSPI} \times 2}{9})$$

Where $SPIn$ is the MOSI delay, USPI2 or USPI5 depending on CPOL and NCPHA. $f_{PINMAX}$ is the maximum frequency of the SPI pins. Please refer to the I/O Pin Characteristics section for the maximum frequency of the pins. $f_{CLKSPI}$ is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock.

**Maximum SPI Frequency, Master Input**

The maximum SPI master input frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(\frac{1}{SPIn + t_{VALID}}, \frac{f_{CLKSPI} \times 2}{9})$$

Where $SPIn$ is the MISO setup and hold time, USPI0 + USPI1 or USPI3 + USPI4 depending on CPOL and NCPHA. $T_{VALID}$ is the SPI slave response time. Please refer to the SPI slave datasheet for $T_{VALID}$ . $f_{CLKSPI}$ is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock.

*7.9.3.2 Slave mode*

**Figure 7-8.** USART in SPI Slave Mode With (CPOL= 0 and CPHA= 1) or (CPOL= 1 and CPHA= 0)

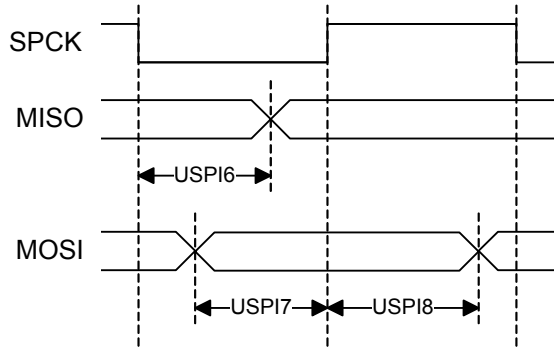


**Figure 7-9.** USART in SPI Slave Mode With (CPOL= CPHA= 0) or (CPOL= CPHA= 1)

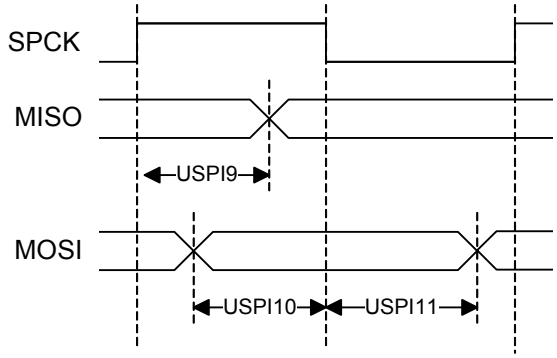



**Figure 7-10.** USART in SPI Slave Mode NPCS Timing

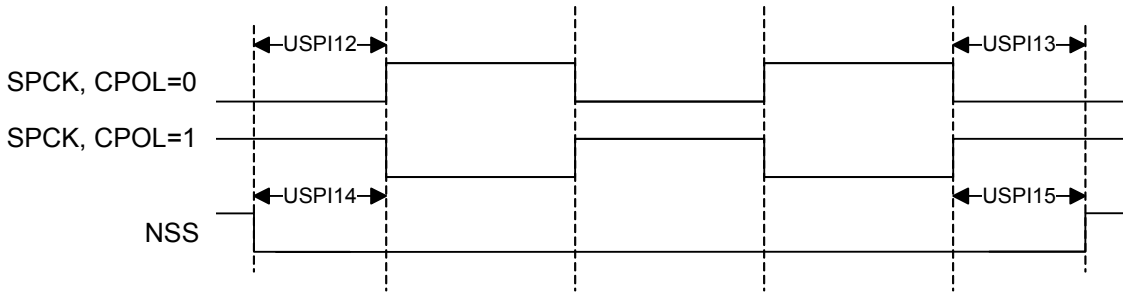



**Table 7-47.** USART in SPI mode Timing, Slave Mode[1]

| Symbol | Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| USPI6 | SPCK falling to MISO delay | external capacitor = 40pF | | 27 | ns |
| USPI7 | MOSI setup time before SPCK rises | | $t_{SAMPLE}$[2] + $t_{CLK\_USART}$ | | ns |
| USPI8 | MOSI hold time after SPCK rises | | 0 | | ns |
| USPI9 | SPCK rising to MISO delay | | | 28 | ns |
| USPI10 | MOSI setup time before SPCK falls | | $t_{SAMPLE}$[2] + $t_{CLK\_USART}$ | | ns |
| USPI11 | MOSI hold time after SPCK falls | | 0 | | ns |
| USPI12 | NSS setup time before SPCK rises | | 33 | | ns |
| USPI13 | NSS hold time after SPCK falls | | 0 | | ns |
| USPI14 | NSS setup time before SPCK falls | | 33 | | ns |
| USPI15 | NSS hold time after SPCK rises | | 0 | | ns |

Note: 1. These values are based on simulation and characterization of other AVR microcontrollers manufactured in the same process technology. These values are not covered by test limits in production.

2. Where: $t_{SAMPLE} = t_{SPCK} - \left( \left\lfloor \frac{t_{SPCK}}{2 \times t_{CLKUSART}} \right\rfloor + \frac{1}{2} \right) \times t_{CLKUSART}$

*7.9.4.2 Slave mode*

**Figure 7-13.** SPI Slave Mode With (CPOL= 0 and NCPHA= 1) or (CPOL= 1 and NCPHA= 0)

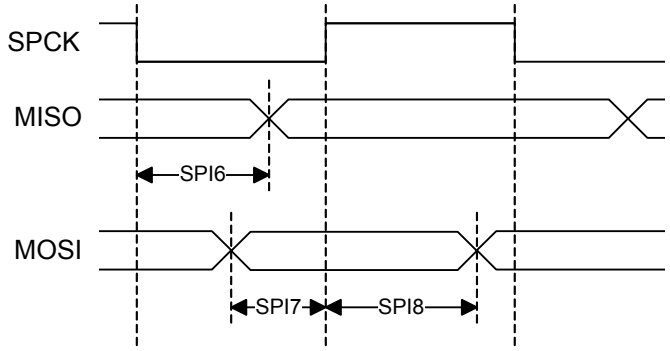



**Figure 7-14.** SPI Slave Mode With (CPOL= NCPHA= 0) or (CPOL= NCPHA= 1)

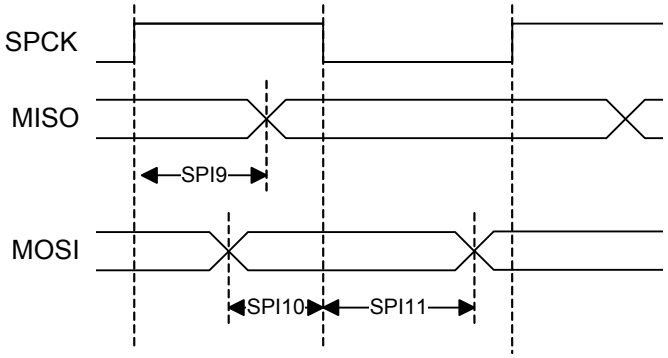



**Figure 7-15.** SPI Slave Mode NPCS Timing

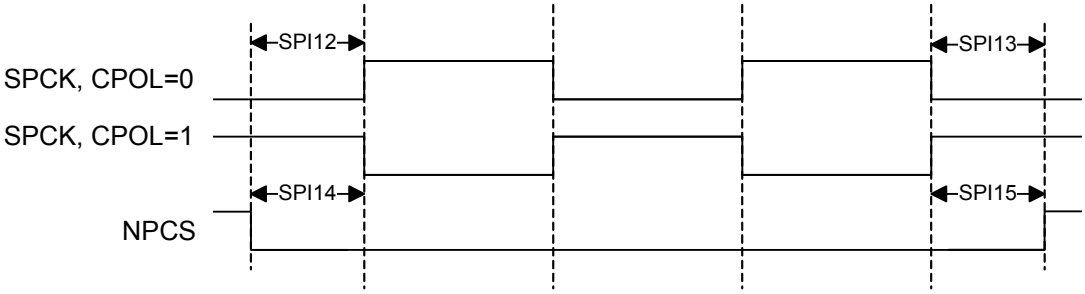
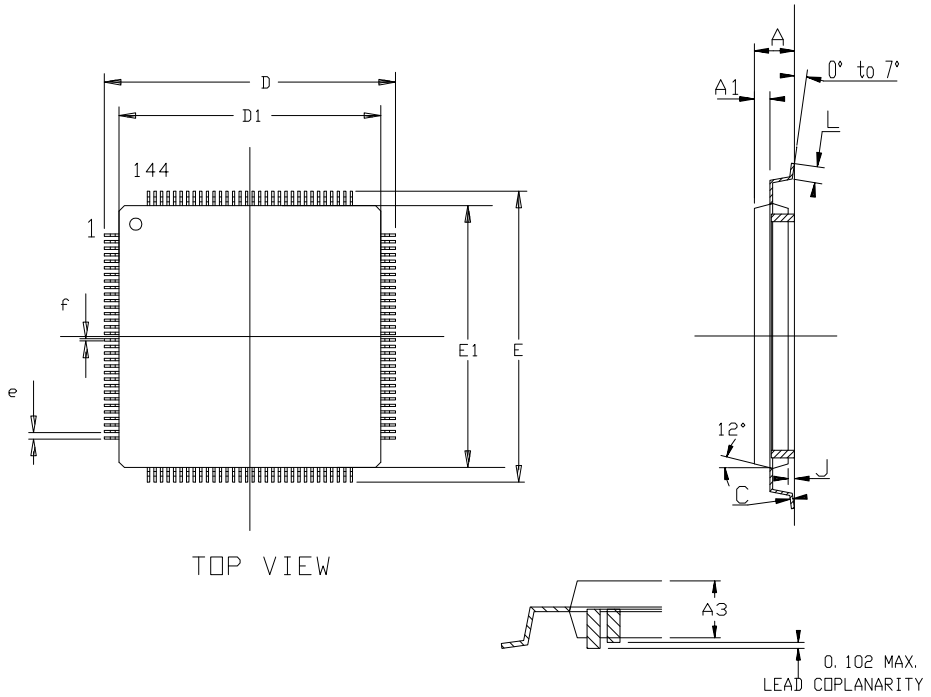


**Table 7-58.** SDRAM Signal[1]

| Symbol | Parameter | Conditions | Min | Units |
|---|---|---|---|---|
| $SDRAMC_1$ | SDCKE high before SDCK rising edge | $V_{VDD}$ = 3.0V, drive strength of the pads set to the highest, external capacitor = 40 pF on SDRAM pins except 8 pF on SDCK pins | 5.6 | ns |
| $SDRAMC_2$ | SDCKE low after SDCK rising edge | | 7.3 | |
| $SDRAMC_3$ | SDCKE low before SDCK rising edge | | 6.8 | |
| $SDRAMC_4$ | SDCKE high after SDCK rising edge | | 8.3 | |
| $SDRAMC_5$ | SDCS low before SDCK rising edge | | 6.1 | |
| $SDRAMC_6$ | SDCS high after SDCK rising edge | | 8.4 | |
| $SDRAMC_7$ | RAS low before SDCK rising edge | | 7 | |
| $SDRAMC_8$ | RAS high after SDCK rising edge | | 7.7 | |
| $SDRAMC_9$ | SDA10 change before SDCK rising edge | | 6.4 | |
| $SDRAMC_{10}$ | SDA10 change after SDCK rising edge | | 7.1 | |
| $SDRAMC_{11}$ | Address change before SDCK rising edge | | 4.7 | |
| $SDRAMC_{12}$ | Address change after SDCK rising edge | | 4.4 | |
| $SDRAMC_{13}$ | Bank change before SDCK rising edge | | 6.2 | |
| $SDRAMC_{14}$ | Bank change after SDCK rising edge | | 6.9 | |
| $SDRAMC_{15}$ | CAS low before SDCK rising edge | | 6.6 | |
| $SDRAMC_{16}$ | CAS high after SDCK rising edge | | 7.8 | |
| $SDRAMC_{17}$ | DQM change before SDCK rising edge | | 6 | |
| $SDRAMC_{18}$ | DQM change after SDCK rising edge | | 6.7 | |
| $SDRAMC_{19}$ | D0-D15 in setup before SDCK rising edge | | 6.4 | |
| $SDRAMC_{20}$ | D0-D15 in hold after SDCK rising edge | | 0 | |
| $SDRAMC_{23}$ | SDWE low before SDCK rising edge | | 7 | |
| $SDRAMC_{24}$ | SDWE high after SDCK rising edge | | 7.4 | |
| $SDRAMC_{25}$ | D0-D15 Out valid before SDCK rising edge | | 5.2 | |
| $SDRAMC_{26}$ | D0-D15 Out valid after SDCK rising edge | | 5.6 | |

Note: 1. These values are based on simulation and characterization of other AVR microcontrollers manufactured in the same process technology. These values are not covered by test limits in production.

**Figure 8-4.** LQFP-144 package drawing




| | MM | | | INCH | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | – | – | 1.60 | – | – | .063 |
| C | 0.09 | – | 0.20 | .004 | – | .008 |
| A3 | 1.35 | 1.40 | 1.45 | .053 | .055 | .057 |
| D | 21.90 | 22.00 | 22.10 | .862 | .866 | .870 |
| D1 | 19.90 | 20.00 | 20.10 | .783 | .787 | .791 |
| E | 21.90 | 22.00 | 22.10 | .862 | .866 | .870 |
| E1 | 19.90 | 20.00 | 20.10 | .783 | .787 | .791 |
| J | 0.05 | – | 0.15 | .002 | – | .006 |
| L | 0.45 | 0.60 | 0.75 | .018 | .024 | .030 |
| e | 0.50 BSC | | | .0197 BSC | | |
| f | 0.22 BSC | | | .009 BSC | | |

**Table 8-11.** Device and Package Maximum Weight

| | |
|---|---|
| 1300 | mg |

**Table 8-12.** Package Characteristics

| | |
|---|---|
| Moisture Sensitivity Level | Jdec J-STD0-20D - MSL 3 |

**Table 8-13.** Package Reference

| | |
|---|---|
| JEDEC Drawing Reference | MS-026 |
| JESD97 Classification | E3 |

# 9. Ordering Information

**Table 9-1.** Ordering Information

| Device | Ordering Code | Carrier Type | Package | Temperature Operating Range |
|---|---|---|---|---|
| **AT32UC3C0512C** | AT32UC3C0512C-ALUT | Tray | LQFP 144 | Industrial (-40°C to 85°C) |
| | AT32UC3C0512C-ALUR | Tape & Reel | | |
| **AT32UC3C0256C** | AT32UC3C0256C-ALUT | Tray | | |
| | AT32UC3C0256C-ALUR | Tape & Reel | | |
| **AT32UC3C0128C** | AT32UC3C0128C-ALUT | Tray | | |
| | AT32UC3C0128C-ALUR | Tape & Reel | | |
| **AT32UC3C064C** | AT32UC3C064C-ALUT | Tray | | |
| | AT32UC3C064C-ALUR | Tape & Reel | | |
| **AT32UC3C1512C** | AT32UC3C1512C-AUT | Tray | TQFP 100 | |
| | AT32UC3C1512C-AUR | Tape & Reel | | |
| **AT32UC3C1256C** | AT32UC3C1256C-AUT | Tray | | |
| | AT32UC3C1256C-AUR | Tape & Reel | | |
| **AT32UC3C1128C** | AT32UC3C1128C-AUT | Tray | | |
| | AT32UC3C1128C-AUR | Tape & Reel | | |
| **AT32UC3C164C** | AT32UC3C164C-AUT | Tray | | |
| | AT32UC3C164C-AUR | Tape & Reel | | |
| **AT32UC3C2512C** | AT32UC3C2512C-A2UT | Tray | TQFP 64 | |
| | AT32UC3C2512C-A2UR | Tape & Reel | | |
| | AT32UC3C2512C-Z2UT | Tray | QFN 64 | |
| | AT32UC3C2512C-Z2UR | Tape & Reel | | |
| **AT32UC3C2256C** | AT32UC3C2256C-A2UT | Tray | TQFP 64 | |
| | AT32UC3C2256C-A2UR | Tape & Reel | | |
| | AT32UC3C2256C-Z2UT | Tray | QFN 64 | |
| | AT32UC3C2256C-Z2UR | Tape & Reel | | |
| **AT32UC3C2128C** | AT32UC3C2128C-A2UT | Tray | TQFP 64 | |
| | AT32UC3C2128C-A2UR | Tape & Reel | | |
| | AT32UC3C2128C-Z2UT | Tray | QFN 64 | |
| | AT32UC3C2128C-Z2UR | Tape & Reel | | |
| **AT32UC3C264C** | AT32UC3C264C-A2UT | Tray | TQFP 64 | |
| | AT32UC3C264C-A2UR | Tape & Reel | | |
| | AT32UC3C264C-Z2UT | Tray | QFN 64 | |
| | AT32UC3C264C-Z2UR | Tape & Reel | | |

**4 SPI bad serial clock generation on 2nd chip_select when SCBR=1, CPOL=1, and NCPHA=0**

When multiple chip selects (CS) are in use, if one of the baudrates equal 1 while one (CSRn.SCBR=1) of the others do not equal 1, and CSRn.CPOL=1 and CSRn.NCPHA=0, then an additional pulse will be generated on SCK.

**Fix/Workaround**

When multiple CS are in use, if one of the baudrates equals 1, the others must also equal 1 if CSRn.CPOL=1 and CSRn.NCPHA=0.

### 10.1.7 TC

**1 Channel chaining skips first pulse for upper channel**

When chaining two channels using the Block Mode Register, the first pulse of the clock between the channels is skipped.

**Fix/Workaround**

Configure the lower channel with RA = 0x1 and RC = 0x2 to produce a dummy clock cycle for the upper channel. After the dummy cycle has been generated, indicated by the SR.CPCS bit, reconfigure the RA and RC registers for the lower channel with the real values.

### 10.1.8 TWIM

**1 SMBALERT bit may be set after reset**

For TWIM0 and TWIM1 modules, the SMBus Alert (SMBALERT) bit in the Status Register (SR) might be erroneously set after system reset.

**Fix/Workaround**

After system reset, clear the SR.SMBALERT bit before commencing any TWI transfer.

For TWIM2 module, the SMBus Alert (SMBALERT) is not implemented but the bit in the Status Register (SR) is erroneously set once TWIM2 is enabled.

**Fix/Workaround**

None.

### 10.1.9 TWIS

**1 Clearing the NAK bit before the BTF bit is set locks up the TWI bus**

When the TWIS is in transmit mode, clearing the NAK Received (NAK) bit of the Status Register (SR) before the end of the Acknowledge/Not Acknowledge cycle will cause the TWIS to attempt to continue transmitting data, thus locking up the bus.

**Fix/Workaround**

Clear SR.NAK only after the Byte Transfer Finished (BTF) bit of the same register has been set.

### 10.1.10 USBC

**1 UPINRQx.INRQ field is limited to 8-bits**

In Host mode, when using the UPINRQx.INRQ feature together with the multi-packet mode to launch a finite number of packet among multi-packet, the multi-packet size (located in the descriptor table) is limited to the UPINRQx.INRQ value multiply by the pipe size.

**Fix/Workaround**

UPINRQx.INRQ value shall be less than the number of configured multi-packet.

**2 In USB host mode, downstream resume feature does not work (UHCON.RESUME=1).**