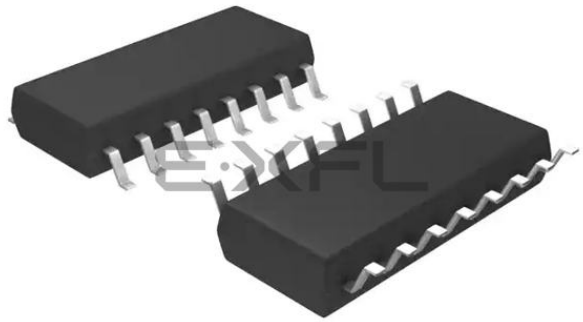

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	LINbus, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	496 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 5x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.209", 5.30mm Width)
Supplier Device Package	16-SOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f223kpf-g-sne1

(Continued)

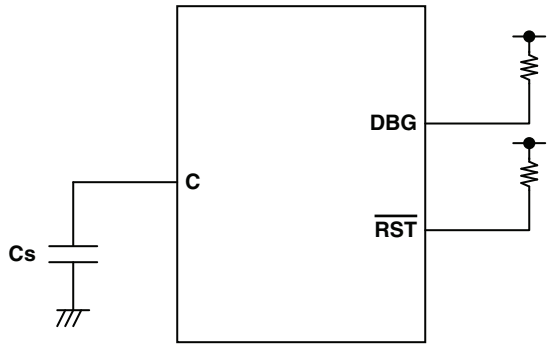
Pin no.	Pin name	I/O circuit type*	Function
13	P05	E	General-purpose I/O port High-current port
	INT05		External interrupt input pin
	AN05		A/D converter analog input pin
	TO00		8/16-bit composite timer ch. 0 clock input pin
	HCLK2		External clock input pin
14	P06	G	General-purpose I/O port High-current port
	INT06		External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 clock input pin
15	P07	G	General-purpose I/O port
	INT07		External interrupt input pin
16	P12	H	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
	DBG		DBG input pin

*: For the I/O circuit types, see “6. I/O Circuit Type”.

C pin

Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the V_{CC} pin must have a capacitance larger than C_S. For the connection to a smoothing capacitor C_S, see the diagram below. To prevent the device from unintentionally entering a mode to which the device is not set to transit due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

DBG/$\overline{\text{RST}}$/C pin connection diagram



13. Electrical Characteristics

13.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS}-0.3	V_{SS} + 6	V	
Input voltage*1	V_{I1}	V_{SS}-0.3	V_{CC} + 0.3	V	Other than PF2*2
	V_{I2}	V_{SS}-0.3	10.5	V	PF2
Output voltage*1	V_O	V_{SS}-0.3	V_{SS} + 6	V	*2
Maximum clamp current	I_{CLAMP}	-2	+ 2	mA	Applicable to specific pins*3
Total maximum clamp current	$S\|I_{CLAMP}\|$	—	20	mA	Applicable to specific pins*3
"L" level maximum output current	I_{OL1}	—	15	mA	Other than P05, P06
	I_{OL2}		15		P05, P06
"L" level average current	I_{OLAV1}	—	4	mA	Other than P05, P06 Average output current = operating current × operating ratio (1 pin)
	I_{OLAV2}		12		P05, P06 Average output current = operating current × operating ratio (1 pin)
"L" level total maximum output current	SI_{OL}	—	100	mA	
"L" level total average output current	SI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (Total number of pins)
"H" level maximum output current	I_{OH1}	—	-15	mA	Other than P05, P06
	I_{OH2}		-15		P05, P06
"H" level average current	I_{OHAV1}	—	-4	mA	Other than P05, P06 Average output current = operating current × operating ratio (1 pin)
	I_{OHAV2}		-8		P05, P06 Average output current = operating current × operating ratio (1 pin)
"H" level total maximum output current	SI_{OH}	—	-100	mA	
"H" level total average output current	SI_{OHAV}	—	-50	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	Pd	—	320	mW	
Operating temperature	T_A	-40	+ 85	°C	
Storage temperature	Tstg	-55	+ 150	°C	

(Continued)

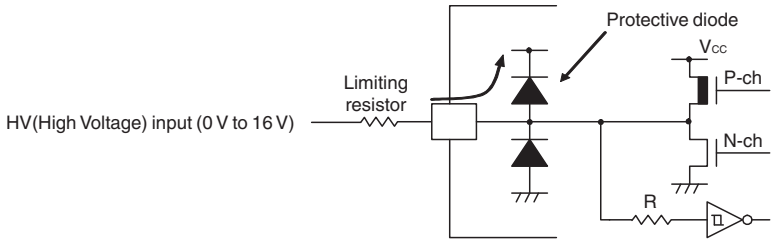
(Continued)

*1: The parameter is based on V_{SS} = 0.0 V.

*2: V_I and V_O must not exceed V_{CC}+0.3 V. V_I must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_I rating.

*3: Applicable to the following pins: P01 to P07, PG1, PG2, PF0, PF1
- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the V_{CC} voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.
- The value of the limiting resistor should be set to a value at which the current to be input to the microcontroller pin when the HV (High Voltage) signal is input is below the standard value, irrespective of whether the current is transient current or stationary current.
- When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the V_{CC} pin, affecting other devices.
- If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
- If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
- Do not leave the HV (High Voltage) input pin unconnected.
- Example of a recommended circuit:

Input/Output equivalent circuit



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

13.2 Recommended Operating Conditions

(V_{SS} = 0.0 V)

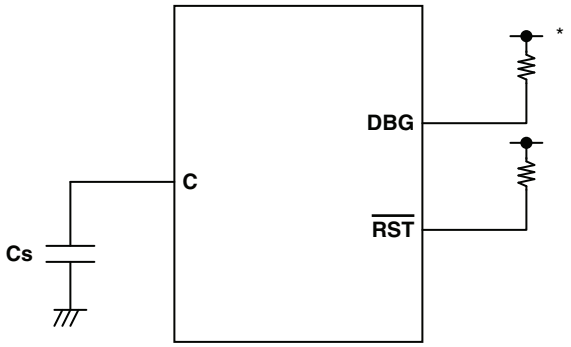
Parameter	Symbol	Value		Unit	Remarks	
		Min	Max			
Power supply voltage	V_{CC}	2.4*1*2	5.5*1	V	In normal operation	Other than on-chip debug mode
		2.3	5.5		Hold condition in stop mode	
		2.9	5.5		In normal operation	On-chip debug mode
		2.3	5.5		Hold condition in stop mode	
Smoothing capacitor	C_S	0.022	1	µF	*3	
Operating temperature	T_A	-40	+85	°C	Other than on-chip debug mode	
		+5	+35		On-chip debug mode	

*1: The value varies depending on the operating frequency, the machine clock and the analog guaranteed range.

*2: The value is 2.88 V when the low-voltage detection reset is used.

*3: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the V_{CC} pin must have a capacitance larger than C_S. For the connection to a smoothing capacitor C_S, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

DBG / $\overline{\text{RST}}$ / C pin connection diagram



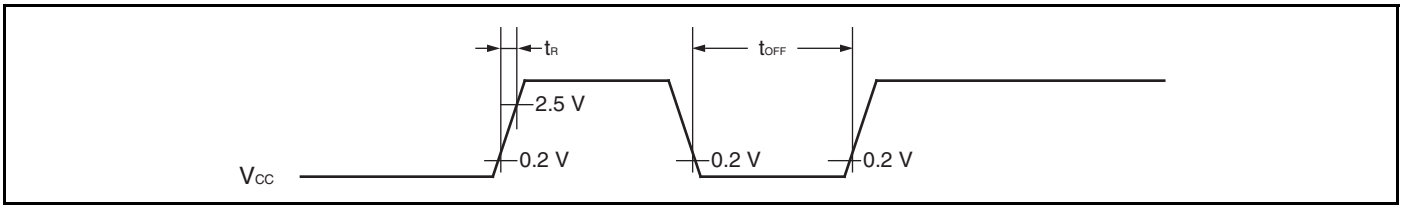
*: Since the DBG pin becomes a communication pin in on-chip debug mode, set a pull-up resistor value suiting the input/output specifications of P12/DBG.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

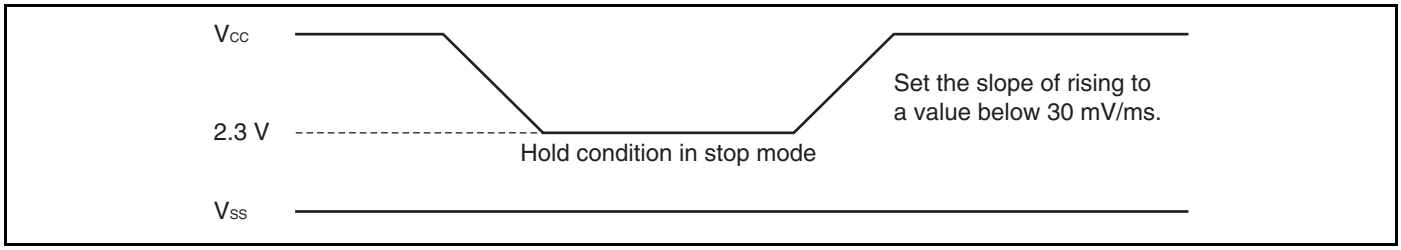
13.4.4 Power-on Reset

(V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Wait time until power-on



Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 30 mV/ms as shown below.

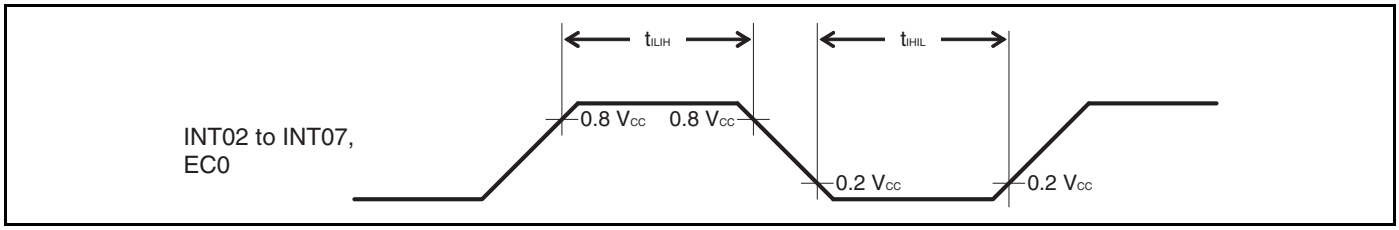


13.4.5 Peripheral Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse width	t_{ILIH}	INT02 to INT07, EC0	2 t_{MCLK}*	—	ns
Peripheral input “L” pulse width	t_{IHIL}		2 t_{MCLK}*	—	ns

* See “13.4.2. Source Clock/Machine Clock” for t_{MCLK}.



13.4.6 LIN-UART Timing (Available only in MB95F222H/F222K/F223H/F223K)

*Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is disabled*2.*
(ESCR register:SCES bit = 0, ECCR register:SCDE bit = 0)

(V_{CC} = 5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = -40°C to +85°C)

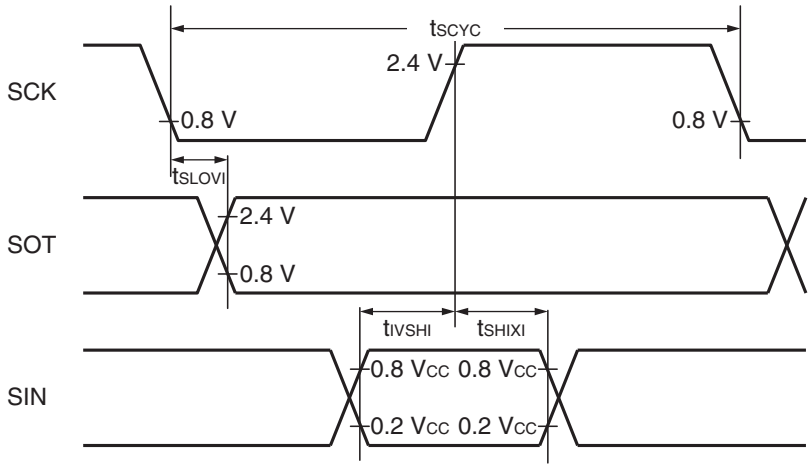
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF+1 TTL	5 t_{MCLK}*3	—	ns
SCK ↓→SOT delay time	t_{SLOVI}	SCK, SOT		-95	+95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3+190	—	ns
SCK ↑→ valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK	External clock operation output pin: C_L = 80 pF+1 TTL	3 t_{MCLK}*3-t_R	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK		t_{MCLK}*3+95	—	ns
SCK ↓→SOT delay time	t_{SLOVE}	SCK, SOT		—	2 t_{MCLK}*3+95	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK, SIN		190	—	ns
SCK ↑→valid SIN hold time	t_{SHIXE}	SCK, SIN		t_{MCLK}*3+95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

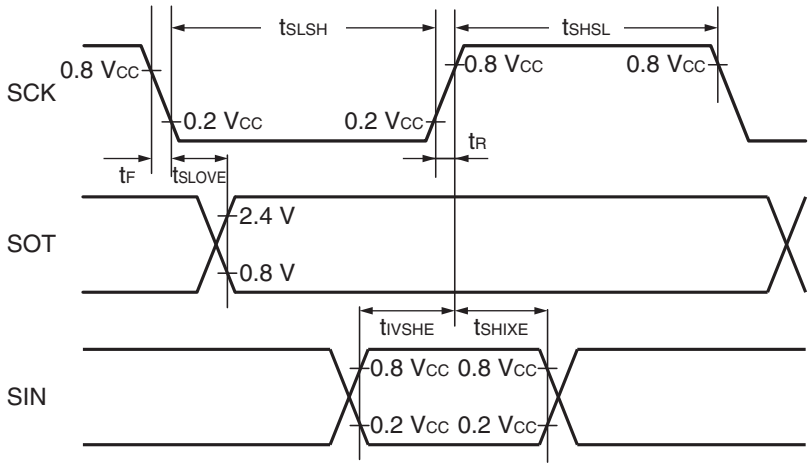
*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “13.4.2. Source Clock/Machine Clock” for t_{MCLK}.

Internal shift clock mode



External shift clock mode



*Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is disabled*2.*
(ESCR register:SCES bit = 1, ECCR register:SCDE bit = 0)

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF+1 TTL	5 t_{MCLK}*3	—	ns
SCK ↑→ SOT delay time	t_{SHOVI}	SCK, SOT		-95	+95	ns
Valid SIN → SCK↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3+190	—	ns
SCK ↓→ valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK	External clock operation output pin: C_L = 80 pF+1 TTL	3 t_{MCLK}*3-t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK		t_{MCLK}*3+95	—	ns
SCK ↑→ SOT delay time	t_{SHOVE}	SCK, SOT		—	2 t_{MCLK}*3+95	ns
Valid SIN → SCK ↓	t_{IVSLE}	SCK, SIN		190	—	ns
SCK↓→ valid SIN hold time	t_{SLIXE}	SCK, SIN		t_{MCLK}*3+95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “13.4.2. Source Clock/Machine Clock” for t_{MCLK}.

*Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is enabled*2.*
(ESCR register:SCES bit = 1, ECCR register:SCDE bit = 1)

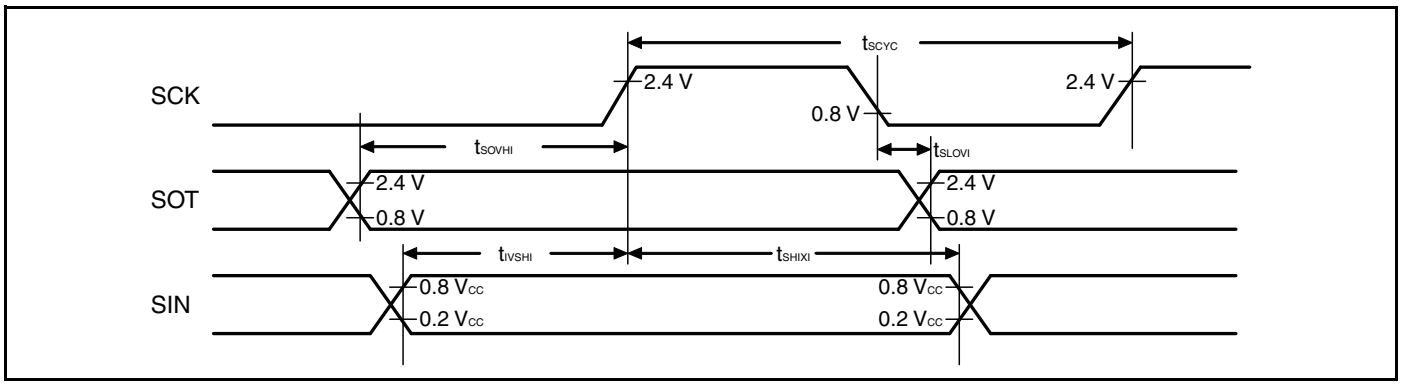
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF+1 TTL	5 t_{MCLK}*3	—	ns
SCK ↓→ SOT delay time	t_{SLOVI}	SCK, SOT		-95	+95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3+190	—	ns
SCK ↑→ valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1:There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

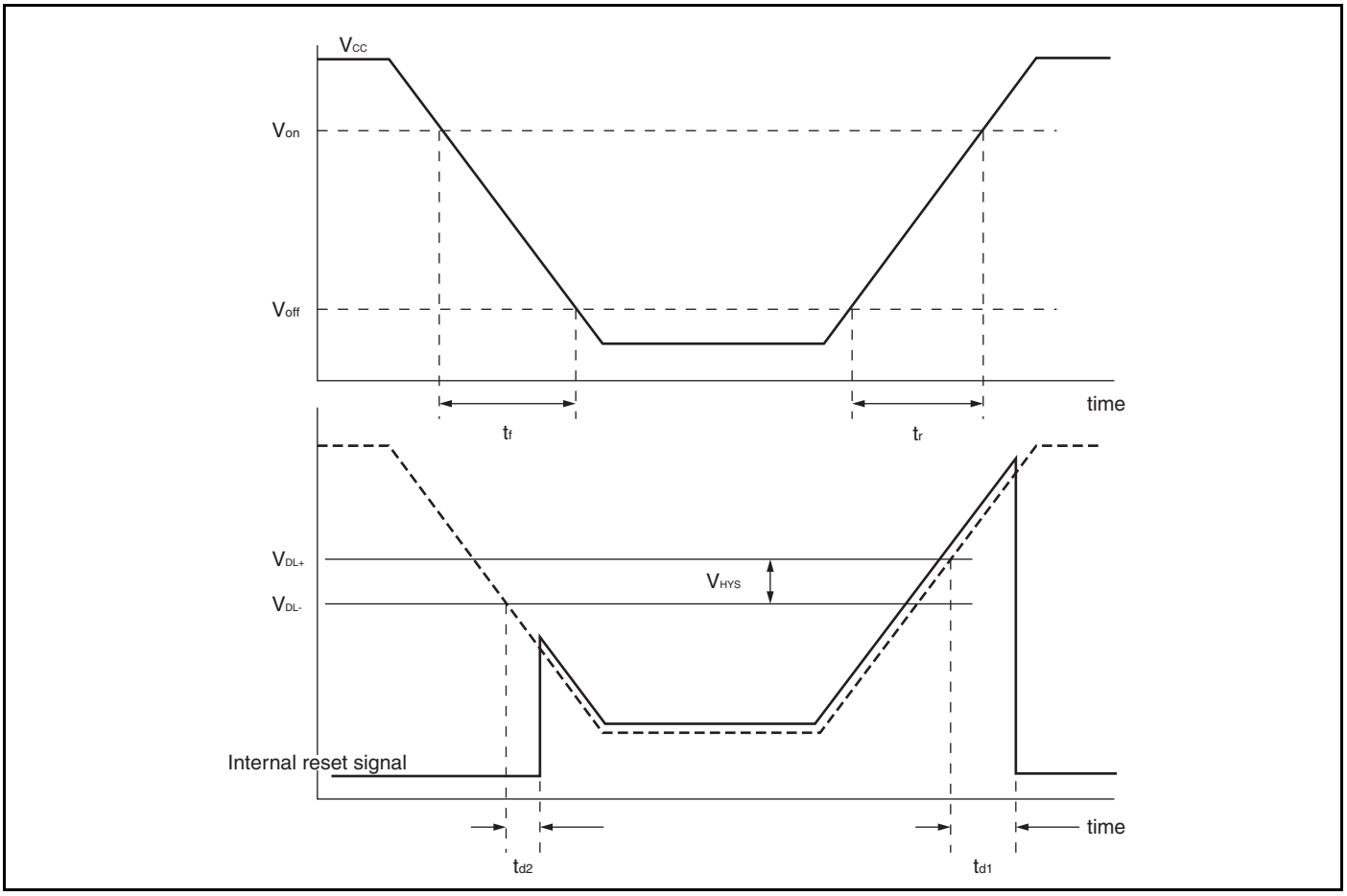
*3: See “13.4.2. Source Clock/Machine Clock” for t_{MCLK}.



13.4.7 Low-voltage Detection

(V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Release voltage	V_{DL+}	2.52	2.7	2.88	V	At power supply rise
Detection voltage	V_{DL-}	2.42	2.6	2.78	V	At power supply fall
Hysteresis width	V_{HYS}	70	100	—	mV	
Power supply start voltage	V_{off}	—	—	2.3	V	
Power supply end voltage	V_{on}	4.9	—	—	V	
Power supply voltage change time (at power supply rise)	t_r	1	—	—	µs	Slope of power supply that the reset release signal generates
		—	3000	—	µs	Slope of power supply that the reset release signal generates within the rating (V_{DL+})
Power supply voltage change time (at power supply fall)	t_f	300	—	—	µs	Slope of power supply that the reset detection signal generates
		—	300	—	µs	Slope of power supply that the reset detection signal generates within the rating (V_{DL-})
Reset release delay time	t_{d1}	—	—	300	µs	
Reset detection delay time	t_{d2}	—	—	20	µs	


V_{CC}
V_{on}
V_{off}
time
t_f
t_r
V_{DL+}
V_{DL-}
V_{HYS}
Internal reset signal
time
t_{d2}
t_{d1}

13.5 A/D Converter

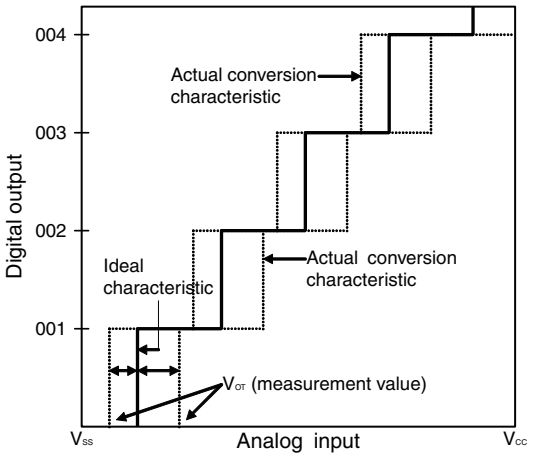
13.5.1 A/D Converter Electrical Characteristics

(V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = -40°C to +85°C)

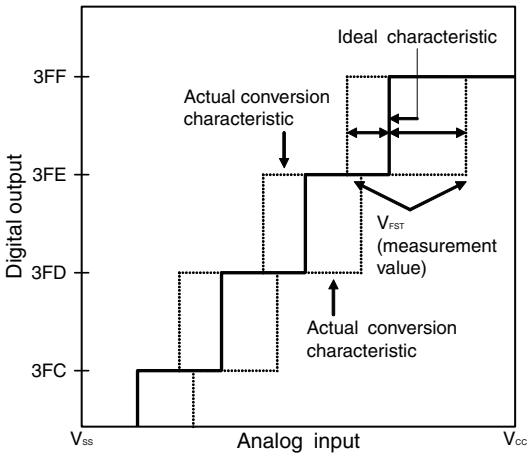
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		-3	—	+3	LSB	
Linearity error		-2.5	—	+2.5	LSB	
Differential linear error		-1.9	—	+1.9	LSB	
Zero transition voltage	V_{OT}	V_{SS}-1.5 LSB	V_{SS}+0.5 LSB	V_{SS}+2.5 LSB	V	
Full-scale transition voltage	V_{FST}	V_{CC}-4.5 LSB	V_{CC}-2 LSB	V_{CC}+0.5 LSB	V	
Compare time	—	0.9	—	16500	µs	4.5 V ≤ V_{CC} ≤ 5.5 V
		1.8	—	16500	µs	4.0 V≤ V_{CC} < 4.5 V
Sampling time	—	0.6	—	∞	µs	4.5 V ≤ V_{CC} ≤ 5.5 V, with external impedance < 5.4 kΩ
		1.2	—	∞	µs	4.0 V ≤ V_{CC} ≤ 4.5 V, with external impedance < 2.4 kΩ
Analog input current	I_{AIN}	-0.3	—	+0.3	µA	
Analog input voltage	V_{AIN}	V_{SS}	—	V_{CC}	V	

(Continued)

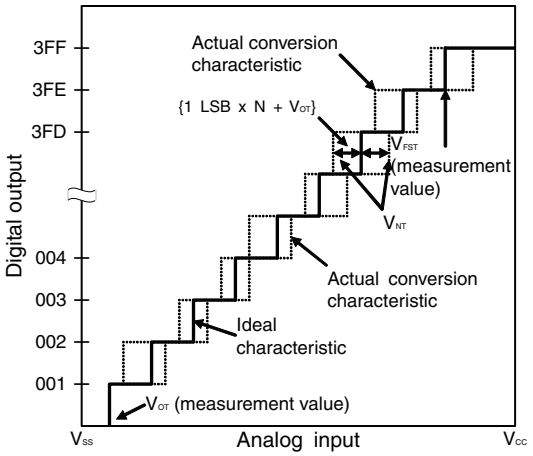
Zero transition error



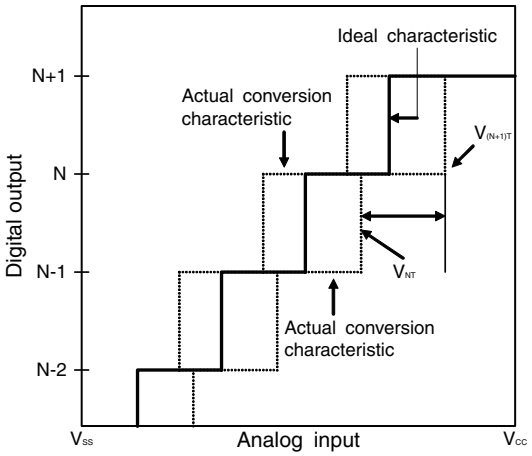
Full-scale transition error



Linearity error



Differential linearity error



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

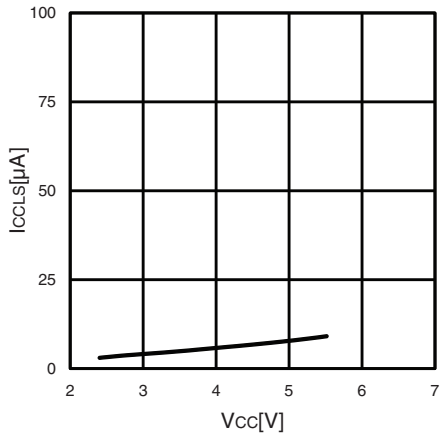
N : A/D converter digital output value

V_{NT}: Voltage at which the digital output transits from (N - 1) to N

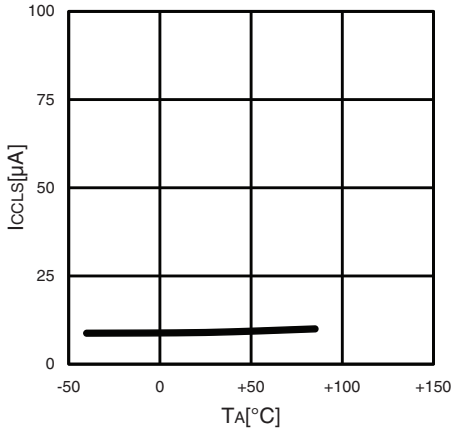
V_{OT} (ideal value) = V_{SS} + 0.5 LSB [V]

V_{FST} (ideal value) = V_{CC} - 2 LSB [V]

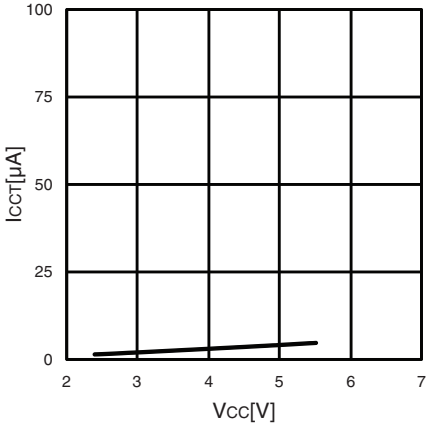
I_{CCLS} - V_{CC}
T_A=+25°C, F_{MPL}=16 kHz (divided by 2)
Subsleep mode with the external clock operating



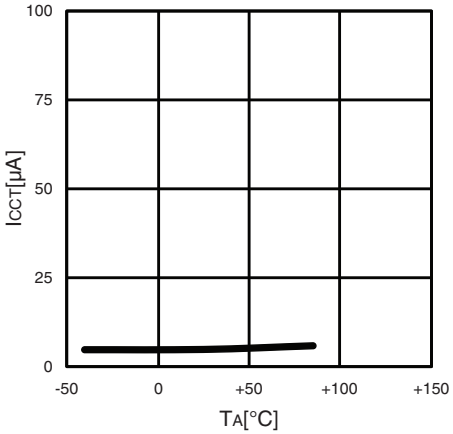
I_{CCLS} - T_A
V_{CC}=5.5 V, F_{MPL}=16 kHz (divided by 2)
Subsleep mode with the external clock operating



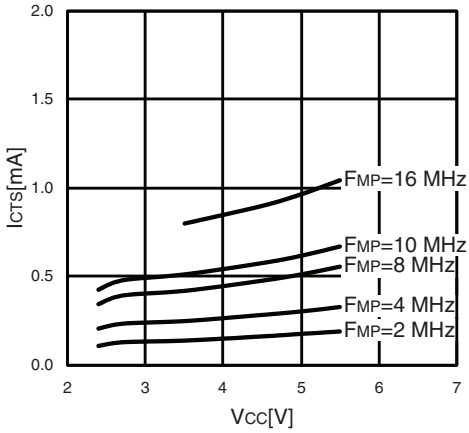
I_{CCT} - V_{CC}
T_A=+25°C, F_{MPL}=16 kHz (divided by 2)
Clock mode with the external clock operating



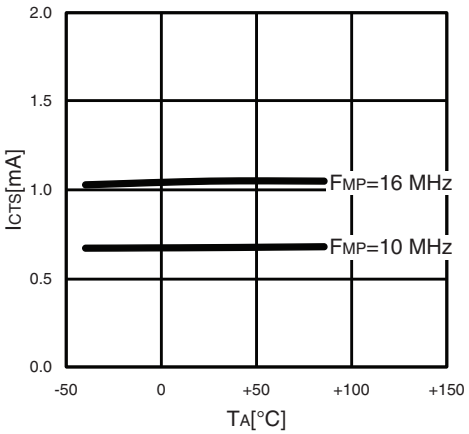
I_{CCT} - T_A
V=5.5 V, F_{MPL}=16 kHz (divided by 2)
Clock mode with the external clock operating



I_{CTS} - V_{CC}
T_A=+25°C, F_{MP}=2, 4, 8, 10, 16 MHz (divided by 2)
Timebase timer mode with the external clock operating

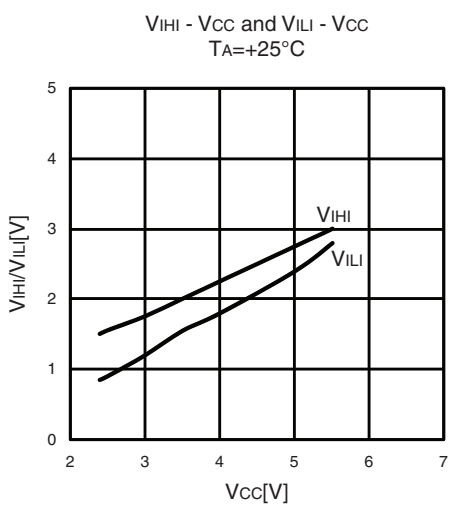


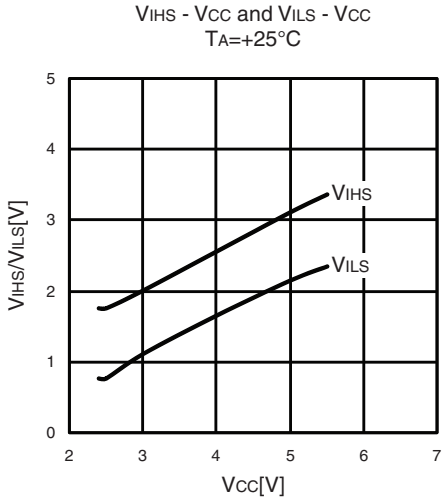
I_{CTS} - T_A
V=5.5 V, F_{MP}=10, 16 MHz (divided by 2)
Timebase timer mode with the external clock operating

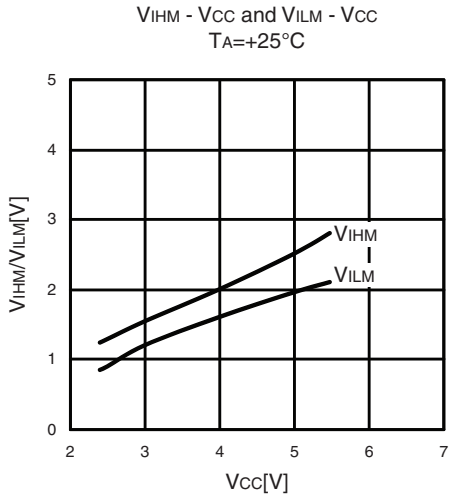


(Continued)

Input voltage







18. Major Changes

Spansion Publication Number: DS07-12626-3E

Page	Section	Change Results
21	Electrical Characteristics 1. Absolute Maximum Ratings	Changed the characteristics of Input voltage.
24	3. DC Characteristics	Corrected the maximum value of “H” level input voltage for PF2 pin. V_{CC} + 0.3 → 10.5
		Corrected the maximum value of Open-drain output application voltage. 0.2Vcc → Vss + 5.5
26		Added the footnote *3.
29	4. AC Characteristics (1) Clock Timing	Added a figure of HCLK1/HCLK2.
32	(2) Source Clock/Machine Clock	Corrected the graph of Operating voltage - Operating frequency (with the on-chip debug function). (Corrected the pitch)
33	(3) External Reset	Added and power on to the remarks column.
48	6. Flash Memory Program/ Erase Characteristics	Added the row of Current drawn on PF2.
		Corrected the minimum value of Power supply voltage at erase/program. 4.5 → 3.0

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: MB95220H Series F^{2}MC-8FX 8-bit Microcontroller Document Number: 002-07513				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	07/26/2010	Migrated to Cypress and assigned document number 002-07513. No change to document contents or format.
*A	5198887	AKIH	03/31/2016	Updated to Cypress format.

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