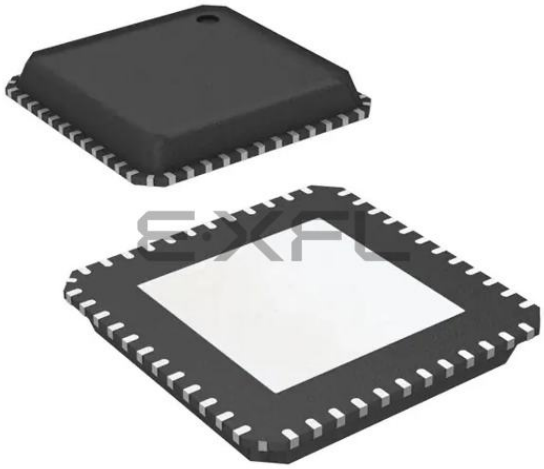

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Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Automotive
Core Processor	ARM® Cortex®-M3
Program Memory Type	FLASH (48kB)
Controller Series	-
RAM Size	3K x 8
Interface	LIN, SSI, UART
Number of I/O	10
Voltage - Supply	5.5V ~ 28V
Operating Temperature	-40°C ~ 175°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-29
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9873qxw40xuma1

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State[1)]	Function
GH2	7	P	–	Gate High Side FET 2
SH1	8	P	–	Source High Side FET 1
GH1	9	P	–	Gate High Side FET 1
SL	10	P	–	Source Low Side FET
GL2	12	P	–	Gate Low Side FET 2
GL1	13	P	–	Gate Low Side FET 1
GH3	5	P	–	Gate High Side FET 3
GL3	11	P	–	Gate Low Side FET 3
Others				
GND_REF	33	P	–	GND for VAREF
VAREF	34	I/O	–	5V ADC1 reference voltage, optional buffer or input
OP1	37	I	–	Negative operational amplifier input
OP2	36	I	–	Positive operational amplifier input
TMS	20	I I/O	I/PD	TMS Test Mode Select input SWD Serial Wire Debug input/output
RESET	22	I/O	–	Reset input, not available during Sleep Mode
EP	–	–	–	Exposed Pad, connect to GND

1) Only valid for digital IOs
2) Also named VDD5V.
3) Also named VDD1V5.

Sleep Mode is activated after 5 consecutive watchdog failures or in case of supply failure (5 times). In this case, MON is enabled as the wake source and Cyclic Wake-Up is activated with 1s of wake time.

Sleep Mode with Cyclic Wake-Up

The Cyclic Wake-Up Mode is a special operating mode of the Sleep Mode. The transition to Cyclic Wake-Up Mode is performed by first setting the corresponding bits in the mode control register followed by the Sleep and Stop Mode command. In addition to the cyclic wake-up behavior (wake-up after a programmable time period), asynchronous wake events via the activated sources (LIN and/or MON) are available, as in normal Sleep Mode.

When using Sleep Mode with cyclic wake-up the voltage regulator is switched off and started again with the wake. A limited number of registers is buffered during sleep, and can be used by SW e.g. for counting sleep/wake cycles.

MCU Slow Down Mode

In MCU Slow Down Mode the MCU frequency is reduced for saving power during operation. LIN communication is still possible. LS MOSFET can be activated.

Wake-Up Source Prioritization

All wake-up sources have the same priority. In order to handle the asynchronous nature of the wake-up sources, the first wake-up signal will initiate the wake-up sequence. Nevertheless all wake-up sources are latched in order to provide all wake-up events to the application software. The software can clear the wake-up source flags. This is to ensure that no wake-up event is lost.

As default wake-up source, the MON input is activated after power-on reset only. Additionally, the device is in Cyclic Wake-Up Mode with the max. configurable dead time setting.

The following table shows the possible power mode configurations including the Stop Mode.

Table 3 Power Mode Configurations

Module/Function	Active Mode	Stop Mode	Sleep Mode	Comment
VDDEXT	ON/OFF	ON (no dynamic load)/OFF	OFF	–
Bridge Driver	ON/OFF	OFF	OFF	
LIN TRx	ON/OFF	wake-up only/ OFF	wake-up only/ OFF	–
VS sense	ON/OFF brownout detection	brownout detection	POR on VS	brownout det. done in PCU
GPIO 5V (wake-up)	n.a.	disabled/static	OFF	–
GPIO 5V (active)	ON	ON	OFF	–
WDT1	ON	OFF	OFF	–
CYCLIC WAKE	n.a.	cyclic wake-up/ cyclic sense/OFF	cyclic wake-up/ OFF	–
Measurement	ON[1)]	OFF	OFF	–
MCU	ON/slow-down/STOP	STOP[2)]	OFF	–
CLOCK GEN (MC)	ON	OFF	OFF	–
LP_CLK (18 MHz)	ON	OFF	OFF	WDT1
LP_CLK2 (100 kHz)	ON/OFF	ON/OFF	ON/OFF	for cyclic wake-up

5 Power Management Unit (PMU)

5.1 Features

- System modes control (startup, sleep, stop and active)
- Power management (cyclic wake-up)
- Control of system voltage regulators with diagnosis (overload, short, overvoltage)
- Fail safe mode detection and operation in case of system errors (watchdog fail)
- Wake-up sources configuration and management (LIN, MON, GPIOs)
- System error logging

5.2 Introduction

The power management unit is responsible for generating all required voltage supplies for the embedded MCU (VDDC, VDDP) and the external supply (VDDEXT). The power management unit is designed to ensure fail-safe behavior of the system IC by controlling all system modes including the corresponding transitions. Additionally, the PMU provides well defined sequences for the system mode transitions and generates hierarchical reset priorities. The reset priorities control the reset behavior of all system functionalities especially the reset behavior of the embedded MCU. All these functions are controlled by a state machine. The system master functionality of the PMU make use of an independent logic supply and system clock. For this reason, the PMU has an "Internal logic supply and system clock" module which works independently of the MCU clock.

- f_{MI_CLK} Measurement interface clock
- f_{TFILT_CLK} Analog module filter clock
- LP_CLK Clock source for all PMU submodules and WDT1

ICU (Interrupt Control Unit)

- NMI (Non-Maskable Interrupt)
- INTISR<15,13:4,1,0> External interrupt signals

RCU (Reset Control Unit)

- PMU_1V5DidPOR Undervoltage reset of power down supply
- PMU_PIN Reset generated by reset pin
- PMU_ExtWDT WDT1 reset
- PMU_IntWDT WDT (SCU) reset
- PMU_SOFT Software reset
- PMU_Wake Sleep Mode/Stop Mode exit with reset
- RESET_TYPE_3 Peripheral reset (contains all resets)
- RESET_TYPE_4 Peripheral reset (without SOFT and WDT reset)

Port Control

- P0_POCONy.PDMx driver strength control
- P1_POCONy.PDMx driver strength control

MISC Control

- MODPISELx Mode selection registers for UART (source section) and Timer (trigger or count selection)

6.3 Clock Generation Unit

The Clock Generation Unit (CGU) enables a flexible clock generation for TLE9873QXW40. During user program execution, the frequency can be modified to optimize the performance/power consumption ratio, allowing power consumption to be adapted to the actual application state.

The CGU in the TLE9873QXW40 consists of one oscillator circuit (OSC_HP), a Phase-Locked Loop (PLL) module with an internal oscillator (OSC_PLL), and a Clock Control Unit (CCU). The CGU can convert a low-frequency input/external clock signal to a high-frequency internal clock.

The system clock f_{SYS} is generated from of the following selectable clocks:

- PLL clock output f_{PLL}
- Direct clock from oscillator OSC_HP f_{OSC}
- Low precision clock f_{LP_CLK} (HW-enabled for startup after reset and during power-down wake-up sequence)

9.2 Introduction

Please also refer to **Chapter 9.3**, **Functional Description**.

9.2.1 Block Diagram

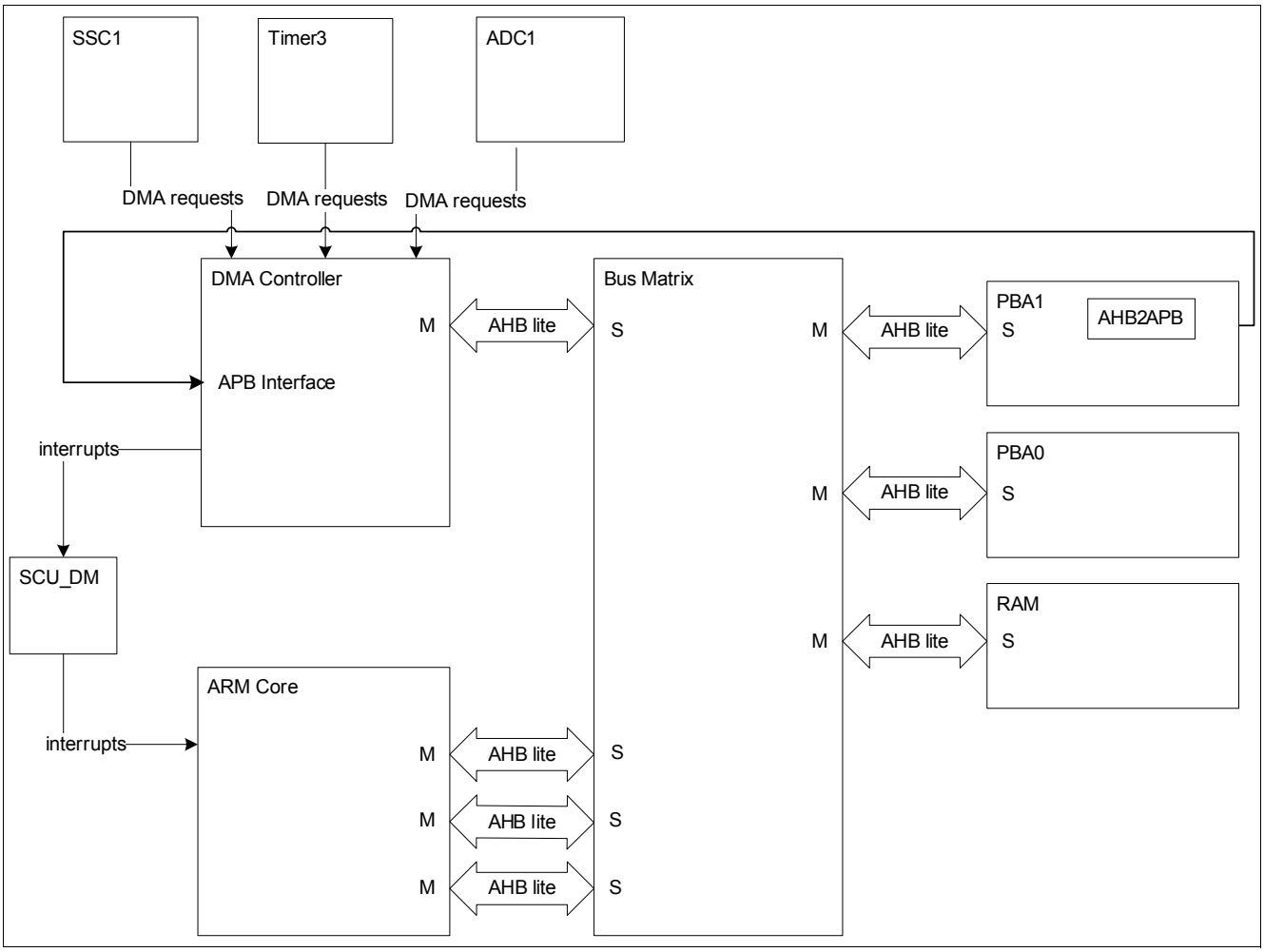

Figure 13 DMA Controller Top Level Block Diagram

11.3 NVM Module (Flash Memory)

The Flash Memory provides an embedded user-programmable non-volatile memory, allowing fast and reliable storage of user code and data.

Features

- In-system programming via LIN (Flash Mode) and SWD
- Error Correction Code (ECC) for detection of single-bit and double-bit errors and dynamic correction of single Bit errors.
- Interrupts and signals double-bit error by NMI
- Program width of 128 byte (page)
- Minimum erase width of 128 bytes (page)
- Integrated hardware support for EEPROM emulation
- 8 byte read access
- Physical read access time: 75 ns
- Code read access acceleration integrated; read buffer and automatic pre-fetch
- Page program time: 3 ms
- Page erase (128 bytes) and sector erase (4K bytes) time: 4ms

Note: The user has to ensure that no flash operations which change the content of the flash get interrupted at any time.

The clock for the NVM is supplied with the system frequency fsys. Integrated firmware routines are provided to erase NVM, and other operations including EEPROM emulation are provided as well.

14.2.2 Port 2

Figure 18 shows the structure of an input-only port pin. Each P2 pin can only function in input mode. Register P2_DIR is provided to enable or disable the input driver. When the input driver is enabled, the actual voltage level present at the port pin is translated into a logic 0 or 1 via a Schmitt trigger device and can be read via register P2_DATA. Each pin can also be programmed to activate an internal weak pull-up or pull-down device. Register P2_PUDSEL selects whether a pull-up or the pull-down device is activated while register P2_PUDEN enables or disables the pull device. The analog input (AnalogIn) bypasses the digital circuitry and Schmitt trigger device for direct feed-through to the ADC input channels.

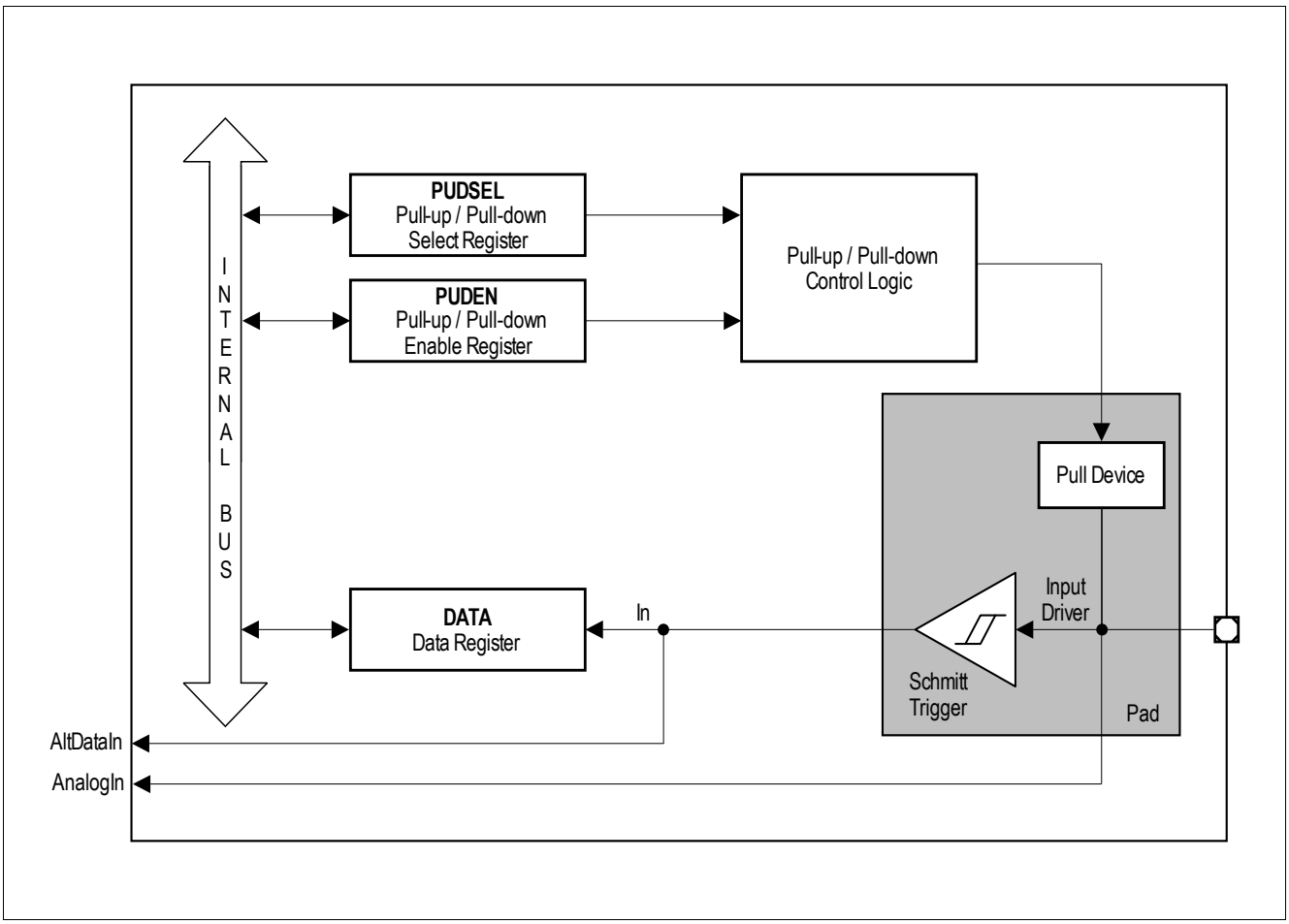

Figure 18 General Structure of Input Port (P2)

18 Capture/Compare Unit 6 (CCU6)

18.1 Feature Set Overview

This section gives an overview over the different building blocks and their main features.

Timer 12 Block Features

- Three capture/compare channels, each channel can be used either as capture or as compare channel
- Generation of a three-phase PWM supported (six outputs, individual signals for high-side and low-side switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short-circuits in the power stage
- Concurrent update of T12 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Start can be controlled by external events
- Capability of counting external events
- Multiple interrupt request sources
- Hysteresis-like control mode

Timer 13 Block Features

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Concurrent update of T13 registers
- Can be synchronized to T12
- Interrupt generation at period-match and compare-match
- Single-shot mode supported
- Start can be controlled by external events
- Capability of counting external events

Additional Specific Functions

- Block commutation for brushless DC-drives implemented
- Position detection via hall-sensor pattern
- Noise filter supported for position input signals
- Automatic rotational speed measurement and commutation control for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC-drives
- Output levels can be selected and adapted to the power stage

18.2 Introduction

The CCU6 unit is made up of a Timer T12 block with three capture/compare channels and a Timer T13 block with one compare channel. The T12 channels can independently generate PWM signals or accept capture triggers, or they can jointly generate control signal patterns to drive DC-motors or inverters.

A rich set of status bits, synchronized updating of parameter values via shadow registers, and flexible generation of interrupt request signals provide efficient software-control.

23.2.2 Measurement Core Module Modes Overview

The basic function of this unit, is the digital signal processing of several analog digitized measurement signals by means of filtering, level comparison and interrupt generation. The Measurement Core module processes ten channels in a quasi parallel process.

As shown in the figure above, the ADC2 postprocessing unit consists of a channel controller (Sequencer), an 10-channel demultiplexer and the signal processing block, which filters and compares the sampled ADC2 values for each channel individually. The channel control block controls the multiplexer sequencing on the analog side before the ADC2 and on the digital domain after the ADC2. As described in the following section, the channel sequence can be controlled in a flexible way, which allows a certain degree of channel prioritization.

This capability can be used e.g. to set a higher priority to supply voltage channels compared to the other channel measurements. The Measurement Core Module offers additionally two different post-processing measurement modes for over-/undervoltage detection and for two-level threshold detection.

The channel controller (sequencer) runs in one of the following modes:

“Normal Sequencer Mode” – channels are selected according to the 10 sequence registers which contain individual enablers for each of the 10 channels.

“Exceptional Interrupt Measurement” – following a hardware event, a high priority channel is inserted into the current sequence. The current actual measurement is not destroyed.

“Exceptional Sequence Measurement” – following a hardware event, a complete sequence is inserted after the current measurement is finished. The current sequence is interrupted by the exception sequence.

25 High-Voltage Monitor Input

25.1 Features

- High-voltage input with V_S/2 threshold voltage
- Integrated selectable pull-up and pull-down current sources
- Wake capability for power saving modes
- Level change sensitivity configurable for transitions from low to high, high to low or both directions

25.2 Introduction

This module is dedicated to monitor external voltage levels above or below a specified threshold or it can be used to detect a wake-up event at the high-voltage MON pin in low-power mode. The input is sensitive to a input level monitoring, this is available when the module is switched to active mode with the SFR bit EN.

To use the Wake function during low power mode of the IC, the monitoring pin is switched to Sleep Mode via the SFR bit EN.

25.2.1 Block Diagram

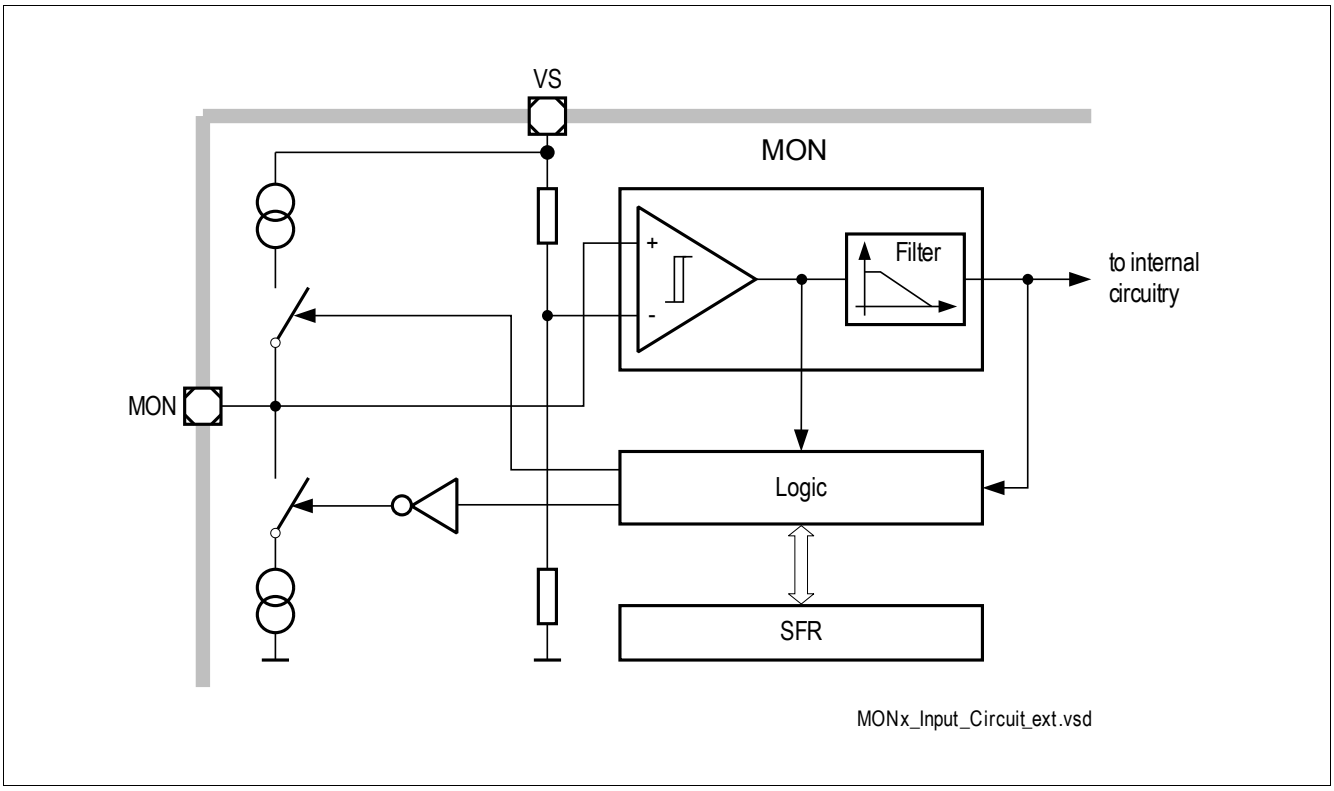

Figure 29 Monitoring Input Block Diagram

28.2 ESD Immunity According to IEC61000-4-2

Note: Tests for ESD immunity according to IEC61000-4-2 “Gun test” (150pF, 330Ω) has been performed. The results and test condition will be available in a test report.

Table 16 ESD “Gun Test”

Performed Test	Result	Unit	Remarks
ESD at pin LIN, versus GND[1)]	> 6	kV	[2)]positive pulse
ESD at pin LIN, versus GND[1)]	< -6	kV	[2)]negative pulse

1) ESD test “ESD GUN” is specified with external components; see application diagram: C_{MON} = 100 nF, R_{MON} = 1 kΩ, C_{LIN} = 220 pF, C_{VS} = >20 µF ELCO + 100 nF ESR < 1 Ω, C_{VSD} = 1 µF, R_{VSD} = 2 Ω.

2) ESD susceptibility “ESD GUN” according to LIN EMC Test Specification, Section 4.3 (IEC 61000-4-2). To be tested by external test house (IBEE Zwickau)

29.4 Flash Memory

This chapter includes the parameters for the 48 kByte embedded flash module.

29.4.1 Flash Parameters

Table 29 Flash Characteristics[1)]

V_S = 3.0 V to 28 V, T_j = -40 °C to +175 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Programming time per 128 byte page	t_{PR}	–	3[2)]	3.5	ms	3V < V_S < 28V	P_4.1.1
Erase time per sector/page	t_{ER}	–	4[2)]	4.5	ms	3V < V_S < 28V	P_4.1.2
Data retention time	t_{RET}	20	–	–	years	1,000 erase / program cycles	P_4.1.3
Data retention time	t_{RET}	50	–	–	years	1,000 erase / program cycles T_j = 30°C[3)]	P_4.1.9
Flash erase endurance for user sectors	N_{ER}	30	–	–	kcycles	Data retention time 5 years	P_4.1.4
Flash erase endurance for security pages	N_{SEC}	10	–	–	cycles	[4)]Data retention time 20 years	P_4.1.5
Drain disturb limit	N_{DD}	32	–	–	kcycles	[5)]	P_4.1.6
Junction temperature range 1	$T_{j\_extend\_1}$	-40	–	150	°C		P_4.1.10
Junction temperature range 2	$T_{j\_extend\_2}$	-40	–	165	°C	[1)]incl. Flash erase/write/read	P_4.1.11
Junction temperature range 3	$T_{j\_extend\_3}$	165	–	175	°C	[1)]incl. Flash read	P_4.1.12

1) Not subject for production test, specified by design.

2) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. The requirement is only relevant for extremely low system frequencies.

3) Derived by extrapolation of lifetime tests.

4) T_j = 25 °C.

5) This parameter limits the number of subsequent programming operations within a physical sector without a given page in this sector being (re-)programmed. The drain disturb limit is applicable if wordline erase is used repeatedly. For normal sector erase/program cycles this limit will not be violated. For data sectors the integrated EEPROM emulation firmware routines handle this limit automatically, for wordline erases in code sectors (without EEPROM emulation) it is recommended to execute a software based refresh, which may make use of the integrated random number generator NVMBRNG to statistically start a refresh.

Table 33 Electrical Characteristics LIN Transceiver (cont'd)

V_s = 5.5V to 18V, T_j = -40 °C to +175 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Duty cycle D2 Normal Slope Mode (for worst case at 20 kbit/s)	t_{duty2}	–	–	0.581		[4] duty cycle 2 TH_{Rec}(min) = 0.422 × V_S; TH_{Dom}(min) = 0.284 × V_S; V_S = 5.5 … 18 V; t_{bit} = 50 µs; D2 = $t_{bus\_rec(max)}$/2 t_{bit}; LIN Spec 2.2 (Par. 28)	P_6.1.20
AC Characteristics - Transceiver Low Slope Mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	–	6	µs	LIN Spec 2.2 (Param. 31)	P_6.1.21
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	–	6	µs	LIN Spec 2.2 (Param. 31)	P_6.1.22
Receiver delay symmetry	$t_{sym,R}$	-2	–	2	µs	$t_{sym,R}$ = $t_{d(L),R}$ - $t_{d(H),R}$; LIN Spec 2.2 (Par. 32)	P_6.1.23
Duty cycle D3 (for worst case at 10,4 kbit/s)	t_{duty1}	0.417	–	–		[4] duty cycle 3 TH_{Rec}(max) = 0.778 × V_S; TH_{Dom}(max) = 0.616 × V_S; V_S = 5.5 … 18 V; t_{bit} = 96 µs; D3 = $t_{bus\_rec(min)}$/2 t_{bit}; LIN Spec 2.2 (Par. 29)	P_6.1.24
Duty cycle D4 (for worst case at 10,4 kbit/s)	t_{duty2}	–	–	0.590		[4] duty cycle 4 TH_{Rec}(min) = 0.389 × V_S; TH_{Dom}(min) = 0.251 × V_S; V_S = 5.5 … 18 V; t_{bit} = 96 µs; D4 = $t_{bus\_rec(max)}$/2 t_{bit}; LIN Spec 2.2 (Par. 30)	P_6.1.25
AC Characteristics - Transceiver Fast Slope Mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	–	6	µs	–	P_6.1.26
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	–	6	µs	–	P_6.1.27
Receiver delay symmetry	$t_{sym,R}$	-1.5	–	1.5	µs	$t_{sym,R}$ = $t_{d(L),R}$ - $t_{d(H),R}$; -40°C ≤ T_j ≤ 150°C;	P_6.1.28
Receiver delay symmetry- Extended temperature range	t_{sym,R_HT}	-2.0	–	2.0	µs	$t_{sym,R}$ = $t_{d(L),R}$ - $t_{d(H),R}$; 150°C < T_j ≤ 175°C;	P_6.1.74

29.7 High-Speed Synchronous Serial Interface

29.7.1 SSC Timing Parameters

The table below provides the SSC timing in the TLE9873QXW40.

Table 34 SSC Master Mode Timing (Operating Conditions apply; CL = 50 pF)

V_S = 5.5 V to 28 V, T_j = -40 °C to +175 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
SCLK clock period	t_0	1) 2 * T_{SSC}	–	–		2) V_{DDP} > 2.7 V	P_7.1.1
MTSR delay from SCLK	t_1	10	–	–	ns	2) V_{DDP} > 2.7 V	P_7.1.2
MRST setup to SCLK	t_2	10	–	–	ns	2) V_{DDP} > 2.7 V	P_7.1.3
MRST hold from SCLK	t_3	15	–	–	ns	2) V_{DDP} > 2.7 V	P_7.1.4

1) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. If f_{CPU} = 20 MHz, t_0 = 100 ns. T_{CPU} is the CPU clock period.
2) Not subject to production test, specified by design.

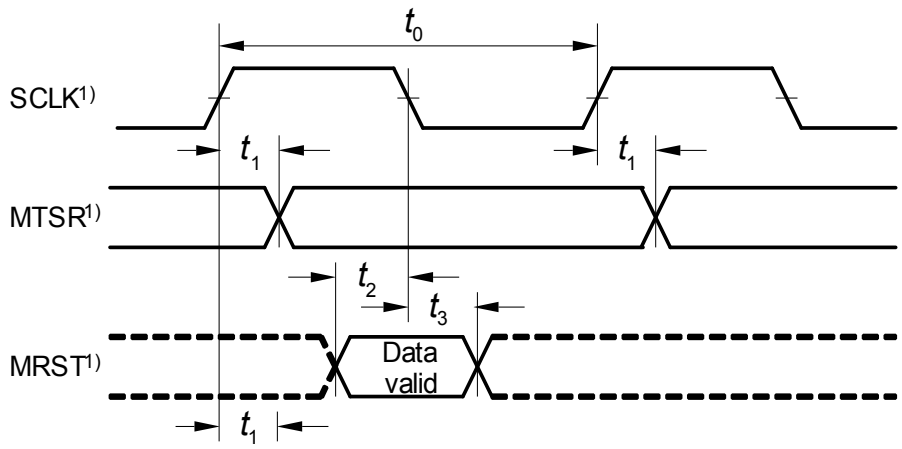

Figure 37 SSC Master Mode Timing

29.8.3 ADC2-VBG

29.8.3.1 ADC2 Reference Voltage VBG

Table 37 DC Specifications

V_S = 3.0 V to 28 V, T_j = -40 °C to +175 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Reference Voltage	V_{BG}	1.199	1.211	1.223	V	1)	P_8.3.1

1) Not subject to production test, specified by design.

29.8.3.2 ADC2 Specifications

Table 38 DC Specifications

V_S = 5.5 V to 28 V, T_j = -40 °C to +175 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Resolution	RES	–	8	–	Bits	Full	P_8.3.18
Guaranteed offset error	EA_{OFF_8Bit}	-2.0	±0.3	2.0	LSB	not calibrated	P_8.3.19
Gain error	EA_{Gain_8Bit}	-2.0	±0.5	2.0	%FSR	not calibrated	P_8.3.20
Differential non-linearity (DNL)	EA_{DNL_8Bit}	-0.8	±0	0.8	LSB	Full; -40°C ≤ T_j ≤ 150°C	P_8.3.21
Differential non-linearity (DNL)-Extended temperature range	$EA_{DNL\_8Bit\_HT}$	-1.2	±0	1.2	LSB	Full; 150°C < T_j ≤ 175°C	P_8.3.28
Integral non-linearity (INL)	EA_{INL_8Bit}	-1.2	±0	1.2	LSB	Full; -40°C ≤ T_j ≤ 150°C	P_8.3.22
Integral non-linearity (INL)-Extended temperature range	$EA_{INL\_8Bit\_HT}$	-1.50	±0	1.50	LSB	Full; 150°C < T_j ≤ 175°C	P_8.3.29

29.12 MOSFET Driver

29.12.1 Electrical Characteristics

Table 42 Electrical Characteristics MOSFET Driver

V_S = 5.5 V to 28 V, T_j = -40 °C to +175 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
MOSFET Driver Output							
Maximum total charge driver capability	Q_{tot_max}	–	–	100	nC	[1]Due to Charge Pump currrent capability only 3 x MOSFETs + additional external capacitors with a total charge of max. 100nC can be driven simultaneous at a PWM frequency of 25 kHz.	P_12.1.20
Source current - Charge current (low gate voltage)- High Side Driver	I_{Soumax_HS}	230	345	450	mA	V_{SD} ≥ 8 V, C_{Load} = 10 nF, I_{Sou} = C_{Load} * slew rate (= 20%-50% of V_{GHx1}), I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.78
Sink current - Discharge current-High Side Driver	$I_{Sinkmax\_HS}$	230	330	450	mA	V_{SD} ≥ 8 V, C_{Load} = 10 nF, I_{Sink} = C_{Load} * slew rate (= 50%-20% of V_{GHx1}), I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.79
Source current - Charge current (low gate voltage)- Low Side Driver	I_{Soumax_LS}	200	295	375	mA	V_{SD} ≥ 8 V, C_{Load} = 10 nF, I_{Sou} = C_{Load} * slew rate (= 20%-50% of V_{GLx1}), I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.80
Sink current - Discharge current-Low Side Driver	$I_{Sinkmax\_LS}$	200	314	375	mA	V_{SD} ≥ 8 V, C_{Load} = 10 nF, I_{Sink} = C_{Load} * slew rate (= 50%-20% of V_{GLx1}), I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.81
High level output voltage Gxx vs. Sxx	V_{Gxx1}	10	–	14	V	V_{SD} ≥ 8V, C_{Load} = 10 nF, I_{CP}=2.5 mA[2].	P_12.1.3
High level output voltage GHx vs. SHx	V_{Gxx2}	8	–	–	V	V_{SD} = 6.4 V[1], C_{Load} = 10 nF, I_{CP}=2.5 mA[2]	P_12.1.4
High level output voltage GHx vs. SHx	V_{Gxx3}	7	–	–	V	V_{SD} = 5.4 V, C_{Load} = 10 nF, I_{CP}=2.5 mA[2]	P_12.1.5

Table 42 Electrical Characteristics MOSFET Driver (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +175 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input propagation time (HS on)	$t_{P(IHN)max}$	–	200	350	ns	C_{Load} = 10 nF, I_{Charge} =31(max), 25% of V_{Gxx1}	P_12.1.28
Input propagation time (HS off)	$t_{P(IHF)max}$	–	200	300	ns	C_{Load} = 10 nF, $I_{Discharge}$ =31(max), 75% of V_{Gxx1}	P_12.1.29
Absolute input propagation time difference between propagation times for all LSx (LSx on)	$t_{Pon(diff)LSx}$	–	–	100	ns	C_{Load} = 10 nF, I_{Charge} =31(max), 25% of V_{Gxx1}	P_12.1.30
Absolute input propagation time difference between propagation times for all LSx (LSx off)	$t_{Poff(diff)LSx}$	–	–	100	ns	C_{Load} = 10 nF, $I_{Discharge}$ =31(max), 75% of V_{Gxx1}	P_12.1.41
Absolute input propagation time difference between propagation times for all HSx (HSx on)	$t_{Pon(diff)HSx}$	–	–	100	ns	C_{Load} = 10 nF, I_{Charge} =31(max), 25% of V_{Gxx1}	P_12.1.42
Absolute input propagation time difference between propagation times for all HSx (HSx off)	$t_{Poff(diff)HSx}$	–	–	100	ns	C_{Load} = 10 nF, $I_{Discharge}$ =31(max), 75% of V_{Gxx1}	P_12.1.43
Drain source monitoring							
Drain source monitoring threshold	$V_{DSMONVTH}$	– 0.07 0.35 0.55 0.65 0.90 1.00 1.20 1.40	– 0.25 0.50 0.75 1.00 1.25 1.5 1.75 2.00	– 0.40 0.650 0.90 1.25 1.45 1.80 2.10 2.40	V	DRV_CTRL3.DSMONVTH<2:0> xxx 000 001 010 011 100 101 110 111	P_12.1.46
Open load diagnosis currents							
Pull-up diagnosis current	I_{PUDiag}	-220	-370	-520	µA	I_{DISCHG} = 1; V_{SHx} = 5.0 V	P_12.1.47
Pull-down diagnosis current	I_{PDDiag}	650	900	1100	µA	I_{DISCHG} = 1; V_{SHx} = 5.0 V	P_12.1.48
Charge pump							
Output voltage VCP vs. VSD	V_{CPmin1}	8.5	–	–	V	V_{VSD} = 5.4V, I_{CP}=5 mA, C_{CP1}, C_{CP2} = 220 nF, Bridge Driver enabled -40°C ≤ T_j ≤ 150°C	P_12.1.53

Table 42 Electrical Characteristics MOSFET Driver (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +175 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output voltage VCP vs. VSD-Extended temperature range	V_{CPmin1_HT}	8.4	–	–	V	V_{VSD} = 5.4V, I_{CP}=5 mA, C_{CP1}, C_{CP2} = 220 nF, Bridge Driver enabled 150°C < T_j ≤ 175°C	P_12.1.85
Regulated output voltage VCP vs. VSD	V_{CP}	12	14	16	V	8 V ≤ V_{VSD} ≤ 28, I_{CP}=10mA, C_{CP1}, C_{CP2}=220 nF, f_{CP}=250kHz	P_12.1.49
Turn ON Time	t_{ON_VCP}	10	24	40	us	8 V ≤ V_{VSD} ≤ 28, (25%) of V_{CP} 1)4), C_{CP1}, C_{CP2}=220 nF, f_{CP}=250kHz	P_12.1.59
Rise time	t_{rise_VCP}	20	60	88	us	8 V ≤ V_{VSD} ≤ 28, (25-75%) of V_{CP} 1)5), C_{CP1}, C_{CP2}=220 nF, f_{CP}=250kHz	P_12.1.60

1) Not subject to production test.
2) The condition I_{CP} = 2.5 mA emulates an BLDC Driver with 6 MOSFET switching at 20 KHz with a C_{Load}=3.3nF. Test condition: I_{Gx} = - 100 µA, ICHARGE = IDISCHARGE = 31(max), IDISCHARGEDIV2_N = 1 and ICHARGEDIV2_N = 1.
3) This resistance is connected through a diode between SHx and GHx to ground.
4) This time applies when Bit DRV_CP_CTRL_STS.bit.CP_EN is set
5) This time applies when Bit DRV_CP_CLK_CTRL.bit.CPCLK_EN is set

29.13 Operational Amplifier

29.13.1 Electrical Characteristics

Table 43 Electrical Characteristics Operational Amplifier

V_S = 5.5 V to 28 V, T_j = -40 °C to +175 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Differential gain (uncalibrated)	G	 9.5 19 38 57	 10 20 40 60	 10.5 21 42 63		Gain settings GAIN<1:0>: 00 01 10 11	P_13.1.6
Differential input operating voltage range OP2 - OP1	V_{IX}	-1.5 / G	–	1.5 / G	V	G is the Gain specified below	P_13.1.1
Operating. common mode input voltage range (referred to GND (OP2 - GND) or (OP1 - GND)	V_{CM}	-2.0	–	2.0	V	Input common mode has to be checked in evaluation if it fits the required range	P_13.1.2
Max. input voltage range (referred to GND (OP_2 - GND) or (OP1 - GND)	V_{IX_max}	-7.0	–	7.0	V	Max. rating of operational amplifier inputs, where measurement is not done	P_13.1.3
Single ended output voltage range (linear range)	V_{OUT}	V_{ZERO} - 1.5	–	V_{ZERO} + 1.5	V	[1)2)] Offset output voltage 2 V ± 1.5V	P_13.1.4
Linearity error	E_{PWM}	-15	–	15	mV	Maximum deviation from best fit straight line divided by max. value of differential output voltage range (0.5V - 3.5V); this parameter is determined at G = 10.	P_13.1.5
Linearity error	$E_{PWM\_\%}$	-1.0	–	1.0	%	Maximum deviation from best fit straight line divided by max. value of differential output voltage range (0.5V - 3.5V); this parameter is determined at G = 10.	P_13.1.24
Gain drift		-1	–	1	%	Gain drift after calibration at G = 10.	P_13.1.7
Adjusted output offset voltage	V_{OOS}	-40	10	40	mV	V_{AIP}= V_{AIN} = 0 V and G = 40, -40°C < T_j ≤ 150°C	P_13.1.17