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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | DMA, I²S, POR, PWM, WDT |
| Number of I/O | 37 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 9x12b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f302cbt6 |

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# 2 Description

The STM32F302xB/STM32F302xC family is based on the high-performance ARM® Cortex®-M4 32-bit RISC core with FPU operating at a frequency of up to 72 MHz, and embedding a floating point unit (FPU), a memory protection unit (MPU) and an embedded trace macrocell (ETM). The family incorporates high-speed embedded memories (up to 256 Kbytes of Flash memory, up to 40 Kbytes of SRAM) and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The devices offer up to two fast 12-bit ADCs (5 Msps), four comparators, two operational amplifiers, up to one DAC channel, a low-power RTC, up to five general-purpose 16-bit timers, one general-purpose 32-bit timer, and one timer dedicated to motor control. They also feature standard and advanced communication interfaces: up to two $I^2Cs$, up to three SPIs (two SPIs are with multiplexed full-duplex I2Ss), three USARTs, up to two UARTs, CAN and USB. To achieve audio class accuracy, the I2S peripherals can be clocked via an external PLL.

The STM32F302xB/STM32F302xC family operates in the -40 to +85 °C and -40 to +105 °C temperature ranges from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F302xB/STM32F302xC family offers devices in four packages ranging from 48 pins to 100 pins.

The set of included peripherals changes with the device chosen.

## 3.4 Embedded SRAM

STM32F302xB/STM32F302xC devices feature up to 40 Kbytes of embedded SRAM with hardware parity check on first 16 Kbytes of SRAM. The memory can be accessed in read/write at CPU clock speed with 0 wait states.

## 3.5 Boot modes

At startup, Boot0 pin and Boot1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in the system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART2 (PD5/PD6) or USB (PA11/PA12) through DFU (device firmware upgrade).

## 3.6 Cyclic redundancy check (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

### 3.7.4 Low-power modes

The STM32F302xB/STM32F302xC supports three low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- Sleep mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- Stop mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the USB wakeup, the RTC alarm, COMPx, I2Cx or U(S)ARTx.

- Standby mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin or an RTC alarm occurs.

*Note: The RTC, the IWDG and the corresponding clock sources are not stopped by entering Stop or Standby mode.*

## 3.8 Interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

**Table 4. STM32F302xB/STM32F302xC peripheral interconnect matrix**

| Interconnect source | Interconnect destination | Interconnect action |
|---|---|---|
| TIMx | TIMx | Timers synchronization or chaining |
| | ADCx<br>DAC1 | Conversion triggers |
| | DMA | Memory to memory transfer trigger |
| | Compx | Comparator output blanking |
| COMPx | TIMx | Timer input: OCREF_CLR input, input capture |
| ADCx | TIMx | Timer triggered by analog watchdog |

### 3.17.1 Advanced timer (TIM1)

The advanced-control timer, TIM1, can be seen as a three-phase PWM multiplexed on six channels. It has a complementary PWM output with programmable inserted dead-times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIM timers (described in *Section 3.17.2* using the same architecture, so the advanced-control timers can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

### 3.17.2 General-purpose timers (TIM2, TIM3, TIM4, TIM15, TIM16, TIM17)

There are up to six synchronizable general-purpose timers embedded in the STM32F302xB/STM32F302xC (see *Table 5* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, 3, and TIM4

  These are full-featured general-purpose timers:

  – TIM2 has a 32-bit auto-reload up/downcounter and 32-bit prescaler

  – TIM3 and 4 have 16-bit auto-reload up/downcounters and 16-bit prescalers.

  These timers all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

  The counters can be frozen in debug mode.

  All have independent DMA request generation and support quadrature encoders.

- TIM15, 16 and 17

  These three timers general-purpose timers with mid-range features:

  They have 16-bit auto-reload upcounters and 16-bit prescalers.

  – TIM15 has 2 channels and 1 complementary channel

  – TIM16 and TIM17 have 1 channel and 1 complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output.

  The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

  The counters can be frozen in debug mode.

### 3.17.3 Basic timer (TIM6)

This timer is mainly used for DAC trigger generation. It can also be used as a generic 16-bit time base.

Table 7. STM32F302xB/STM32F302xC I²C implementation (continued)

| I2C features[1] | I2C1 | I2C2 |
|---|---|---|
| SMBus | X | X |
| Wakeup from STOP | X | X |

1. X = supported.

## 3.20 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F302xB/STM32F302xC devices have three embedded universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

The USART interfaces are able to communicate at speeds of up to 9 Mbits/s.

They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART interfaces can be served by the DMA controller.

## 3.21 Universal asynchronous receiver transmitter (UART)

The STM32F302xB/STM32F302xC devices have 2 embedded universal asynchronous receiver transmitters (UART4, and UART5). The UART interfaces support IrDA SIR ENDEC, multiprocessor communication mode and single-wire half-duplex communication mode. The UART4 interface can be served by the DMA controller.

Refer to *Table 8* for the features available in all U(S)ART interfaces.

Table 8. USART features

| USART modes/features[1] | USART1 | USART2 | USART3 | UART4 | UART5 |
|---|---|---|---|---|---|
| Hardware flow control for modem | X | X | X | - | - |
| Continuous communication using DMA | X | X | X | X | - |
| Multiprocessor communication | X | X | X | X | X |
| Synchronous mode | X | X | X | - | - |
| Smartcard mode | X | X | X | - | - |
| Single-wire half-duplex communication | X | X | X | X | X |
| IrDA SIR ENDEC block | X | X | X | X | X |
| LIN mode | X | X | X | X | X |
| Dual clock domain and wakeup from Stop mode | X | X | X | X | X |
| Receiver timeout interrupt | X | X | X | X | X |
| Modbus communication | X | X | X | X | X |
| Auto baud rate detection | X | X | X | - | - |
| Driver Enable | X | X | X | - | - |

1. X = supported.

**Table 10. Capacitive sensing GPIOs available on STM32F302xB/STM32F302xC devices**

| Group | Capacitive sensing signal name | Pin name | Group | Capacitive sensing signal name | Pin name |
|---|---|---|---|---|---|
| 1 | TSC_G1_IO1 | PA0 | 5 | TSC_G5_IO1 | PB3 |
| | TSC_G1_IO2 | PA1 | | TSC_G5_IO2 | PB4 |
| | TSC_G1_IO3 | PA2 | | TSC_G5_IO3 | PB6 |
| | TSC_G1_IO4 | PA3 | | TSC_G5_IO4 | PB7 |
| 2 | TSC_G2_IO1 | PA4 | 6 | TSC_G6_IO1 | PB11 |
| | TSC_G2_IO2 | PA5 | | TSC_G6_IO2 | PB12 |
| | TSC_G2_IO3 | PA6 | | TSC_G6_IO3 | PB13 |
| | TSC_G2_IO4 | PA7 | | TSC_G6_IO4 | PB14 |
| 3 | TSC_G3_IO1 | PC5 | 7 | TSC_G7_IO1 | PE2 |
| | TSC_G3_IO2 | PB0 | | TSC_G7_IO2 | PE3 |
| | TSC_G3_IO3 | PB1 | | TSC_G7_IO3 | PE4 |
| | TSC_G3_IO4 | PB2 | | TSC_G7_IO4 | PE5 |
| 4 | TSC_G4_IO1 | PA9 | 8 | TSC_G8_IO1 | PD12 |
| | TSC_G4_IO2 | PA10 | | TSC_G8_IO2 | PD13 |
| | TSC_G4_IO3 | PA13 | | TSC_G8_IO3 | PD14 |
| | TSC_G4_IO4 | PA14 | | TSC_G8_IO4 | PD15 |

**Table 11. No. of capacitive sensing channels available on STM32F302xB/STM32F302xC devices**

| Analog I/O group | Number of capacitive sensing channels | | |
|---|---|---|---|
| | STM32F302Vx | STM32F302Rx | STM32F302Cx |
| G1 | 3 | 3 | 3 |
| G2 | 3 | 3 | 3 |
| G3 | 3 | 3 | 2 |
| G4 | 3 | 3 | 3 |
| G5 | 3 | 3 | 3 |
| G6 | 3 | 3 | 3 |
| G7 | 3 | 0 | 0 |
| G8 | 3 | 0 | 0 |
| Number of capacitive sensing channels | 24 | 18 | 17 |

## 3.27 Development support

### 3.27.1 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

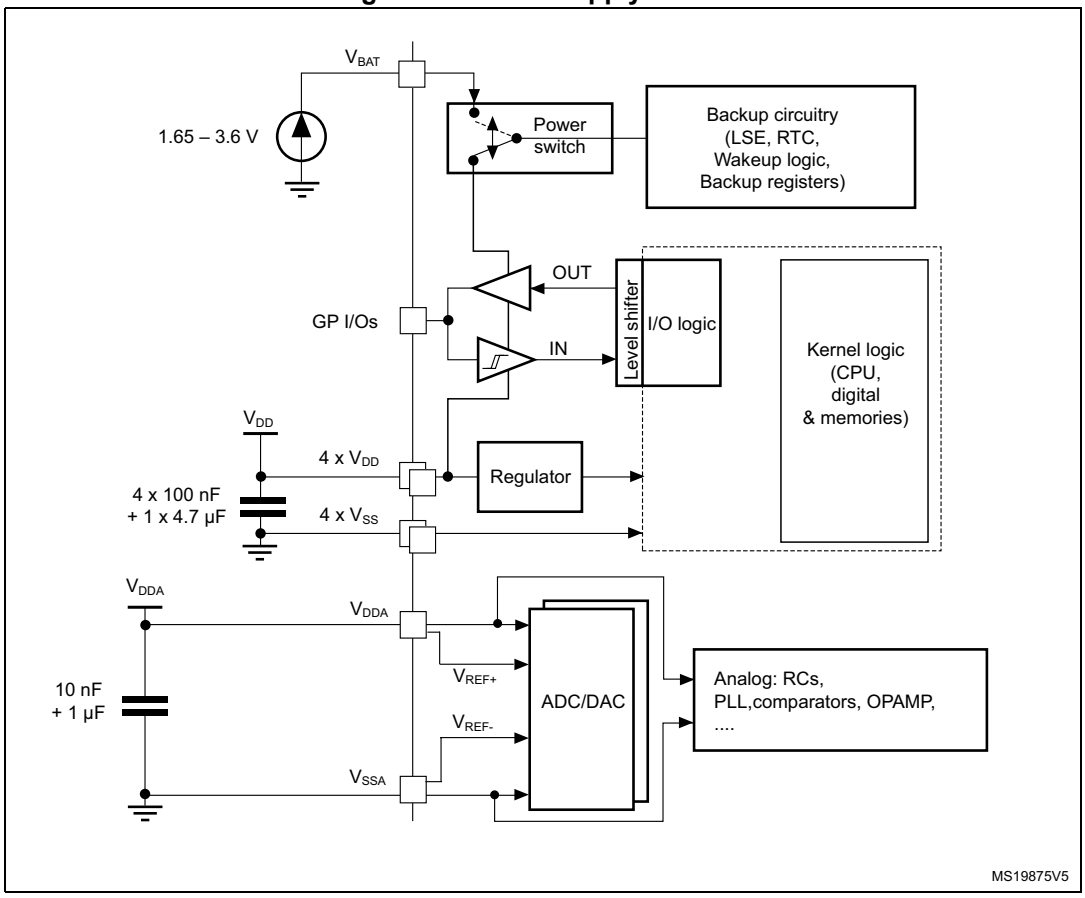
The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

### 3.27.2 Embedded trace macrocell™

The ARM embedded trace macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F302xB/STM32F302xC through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using a high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

### 6.1.6 Power supply scheme

**Figure 11. Power supply scheme**




1. Dotted lines represent the internal connections on low pin count packages, joining the dedicated supply pins.

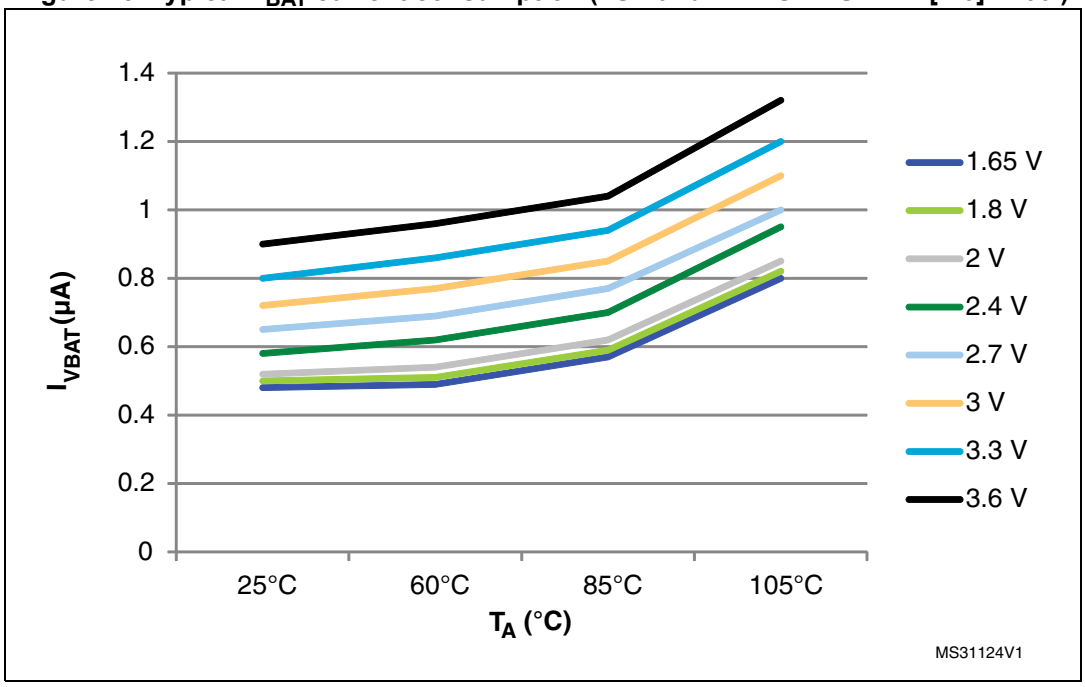
**Caution:** Each power supply pair ($V_{DD}/V_{SS}$, $V_{DDA}/V_{SSA}$ etc..) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

**Table 34. Typical and maximum current consumption from $V_{BAT}$ supply**

| Symbol | Para meter | Conditions (1) | Typ @$V_{BAT}$ | | | | | | | | Max @$V_{BAT}$ = 3.6 V(2) | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.65V | 1.8V | 2V | 2.4V | 2.7V | 3V | 3.3V | 3.6V | $T_A$ = 25°C | $T_A$ = 85°C | $T_A$ = 105°C | |
| $I_{DD\_VBAT}$ | Backup domain supply current | LSE & RTC ON; "Xtal mode" lower driving capability; LSEDRV[1:0] = '00' | 0.48 | 0.50 | 0.52 | 0.58 | 0.65 | 0.72 | 0.80 | 0.90 | 1.1 | 1.5 | 2.0 | µA |
| | | LSE & RTC ON; "Xtal mode" higher driving capability; LSEDRV[1:0] = '11' | 0.83 | 0.86 | 0.90 | 0.98 | 1.03 | 1.10 | 1.20 | 1.30 | 1.5 | 2.2 | 2.9 | |

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a CL of 6 pF for typical values.
2. Guaranteed by characterization results.

**Figure 13. Typical $V_{BAT}$ current consumption (LSE and RTC ON/LSEDRV[1:0] = '00')**



### Typical current consumption

The MCU is placed under the following conditions:

- $V_{DD} = V_{DDA} = 3.3$ V
- All I/O pins available on each package are in analog input configuration
- The Flash access time is adjusted to $f_{HCLK}$ frequency (0 wait states from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz), and Flash prefetch is ON
- When the peripherals are enabled, $f_{APB1} = f_{AHB/2}$, $f_{APB2} = f_{AHB}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8,16 and 64 is used for the frequencies 4 MHz, 2 MHz, 1 MHz, 500 kHz and 125 kHz respectively.

**Table 35. Typical current consumption in Run mode, code with data processing running from Flash**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typ | | Unit |
|---|---|---|---|---|---|---|
| | | | | Peripherals enabled | Peripherals disabled | |
| $I_{DD}$ | Supply current in Run mode from $V_{DD}$ supply | Running from HSE crystal clock 8 MHz, code executing from Flash | 72 MHz | 61.3 | 28.0 | mA |
| | | | 64 MHz | 54.8 | 25.4 | |
| | | | 48 MHz | 41.9 | 19.3 | |
| | | | 32 MHz | 28.5 | 13.3 | |
| | | | 24 MHz | 21.8 | 10.4 | |
| | | | 16 MHz | 14.9 | 7.2 | |
| | | | 8 MHz | 7.7 | 3.9 | |
| | | | 4 MHz | 4.5 | 2.5 | |
| | | | 2 MHz | 2.8 | 1.7 | |
| | | | 1 MHz | 1.9 | 1.3 | |
| | | | 500 kHz | 1.4 | 1.1 | |
| | | | 125 kHz | 1.1 | 0.9 | |
| $I_{DDA}$ (1) (2) | Supply current in Run mode from $V_{DDA}$ supply | | 72 MHz | 240.3 | 239.5 | µA |
| | | | 64 MHz | 210.9 | 210.3 | |
| | | | 48 MHz | 155.8 | 155.6 | |
| | | | 32 MHz | 105.7 | 105.6 | |
| | | | 24 MHz | 82.1 | 82.0 | |
| | | | 16 MHz | 58.8 | 58.8 | |
| | | | 8 MHz | 2.4 | 2.4 | |
| | | | 4 MHz | 2.4 | 2.4 | |
| | | | 2 MHz | 2.4 | 2.4 | |
| | | | 1 MHz | 2.4 | 2.4 | |
| | | | 500 kHz | 2.4 | 2.4 | |
| | | | 125 kHz | 2.4 | 2.4 | |

1. $V_{DDA}$ monitoring is ON.
2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 19* and *Figure 20* for standard I/Os.

**Figure 19. TC and TTa I/O input characteristics - CMOS port**

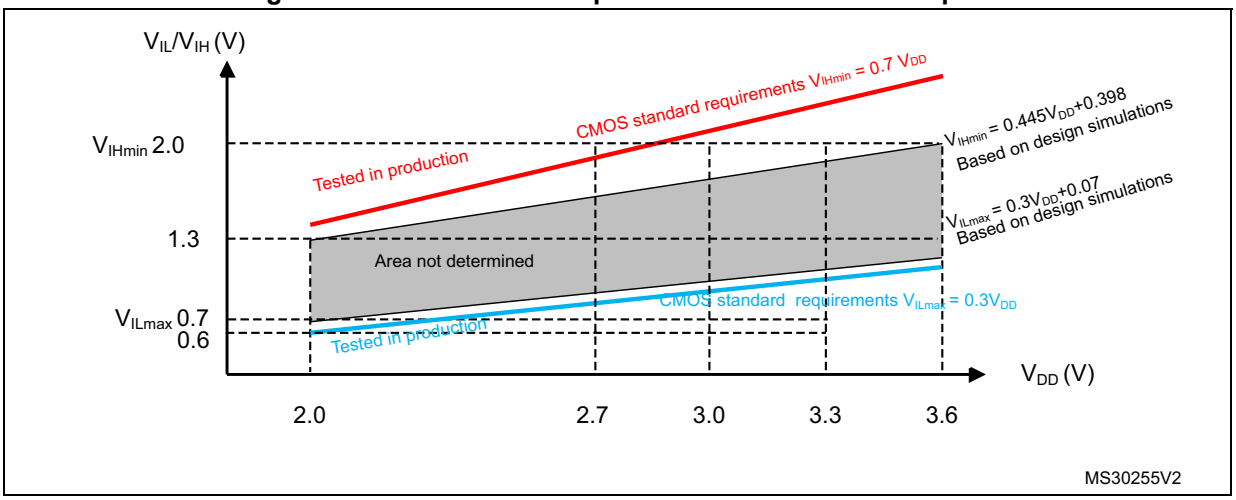



**Figure 20. TC and TTa I/O input characteristics - TTL port**

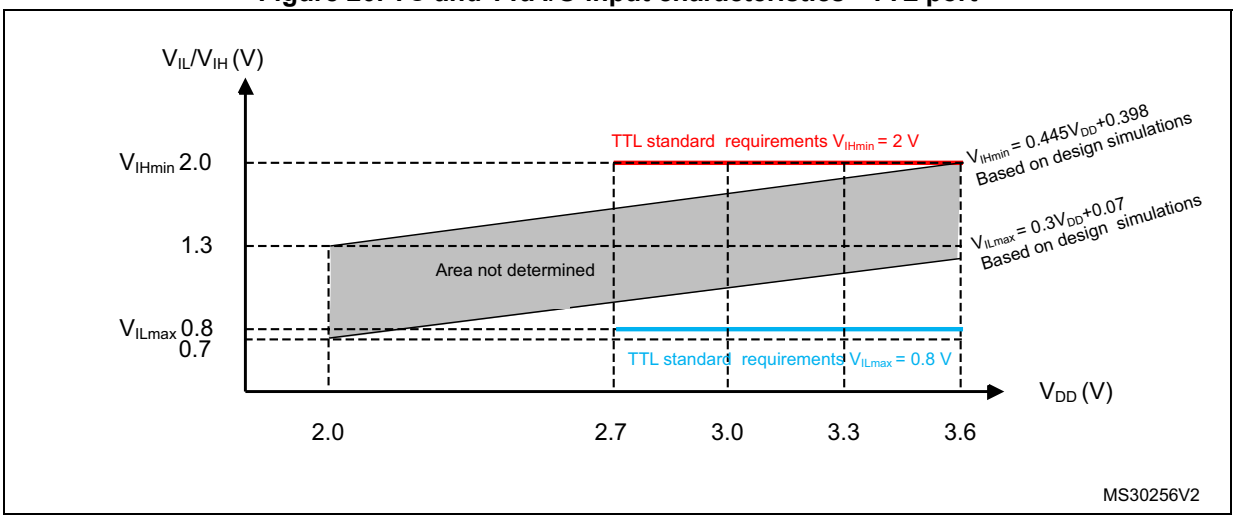


**Table 64. $I^2S$ characteristics(1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{CK}$ $1/t_{c(CK)}$ | $I^2S$ clock frequency | Master data: 16 bits, audio freq=48 kHz | 1.496 | 1.503 | MHz |
| | | Slave | 0 | 12.288 | |
| $t_{r(CK)}$ $t_{f(CK)}$ | $I^2S$ clock rise and fall time | Capacitive load $C_L$ = 30 pF | - | 8 | ns |
| $t_{w(CKH)}$ | $I^2S$ clock high time | Master $f_{PCLK}$= 36 MHz, audio frequency = 48 kHz | 331 | - | |
| $t_{w(CKL)}$ | $I^2S$ clock low time | | 332 | - | |
| $t_{v(WS)}$ | WS valid time | Master mode | 4 | - | |
| $t_{h(WS)}$ | WS hold time | Master mode | 4 | - | |
| $t_{su(WS)}$ | WS setup time | Slave mode | 4 | - | |
| $t_{h(WS)}$ | WS hold time | Slave mode | 0 | - | |
| Duty Cycle | $I^2S$ slave input clock duty cycle | Slave mode | 30 | 70 | % |
| $t_{su(SD\_MR)}$ | Data input setup time | Master receiver | 9 | - | ns |
| $t_{su(SD\_SR)}$ | Data input setup time | Slave receiver | 2 | - | |
| $t_{h(SD\_MR)}$ | Data input hold time | Master receiver | 0 | - | |
| $t_{h(SD\_SR)}$ | | Slave receiver | 0 | - | |
| $t_{v(SD\_ST)}$ | Data output valid time | Slave transmitter (after enable edge) | - | 29 | |
| $t_{h(SD\_ST)}$ | Data output hold time | Slave transmitter (after enable edge) | 12 | - | |
| $t_{v(SD\_MT)}$ | Data output valid time | Master transmitter (after enable edge) | - | 3 | |
| $t_{h(SD\_MT)}$ | Data output hold time | Master transmitter (after enable edge) | 2 | - | |

1. Guaranteed by characterization results.

**Table 68. ADC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_S$(1) | Sampling time | $f_{ADC}$ = 72 MHz | 0.021 | - | 8.35 | µs |
| | | - | 1.5 | - | 601.5 | $1/f_{ADC}$ |
| $T_{ADCVREG\_STUP}$(1) | ADC Voltage Regulator Start-up time | - | - | - | 10 | µs |
| $t_{CONV}$(1) | Total conversion time (including sampling time) | $f_{ADC}$ = 72 MHz Resolution = 12 bits | 0.19 | - | 8.52 | µs |
| | | Resolution = 12 bits | 14 to 614 ($t_S$ for sampling + 12.5 for successive approximation) | | | $1/f_{ADC}$ |
| CMIR(1) | Common Mode Input signal Range | ADC differential mode | $(V_{SSA}+V_{REF+})/2$ -10% | $(V_{SSA}+V_{REF+})/2$ | $(V_{SSA}+V_{REF+})/2$ + 10% | V |

1. Data guaranteed by design.
2. $V_{REF+}$ can be internally connected to $V_{DDA}$ and $V_{REF-}$ can be internally connected to $V_{SSA}$, depending on the package. Refer to *Section 4: Pinouts and pin description* for further details.

**Figure 32. ADC typical current consumption on VDDA pin**

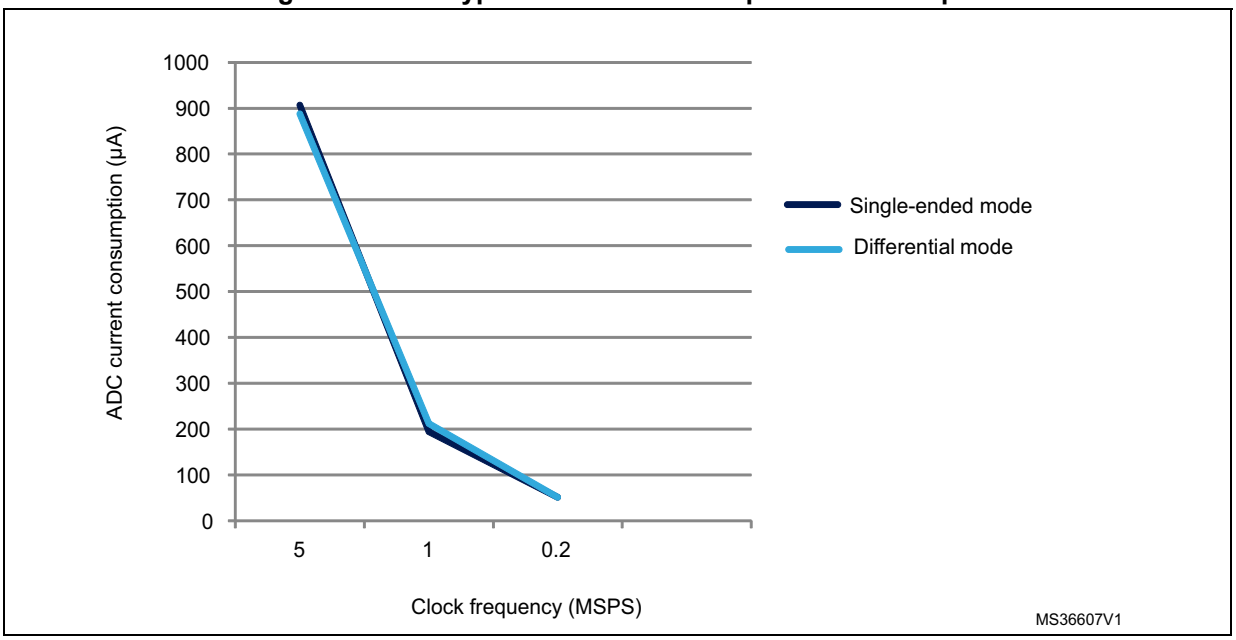
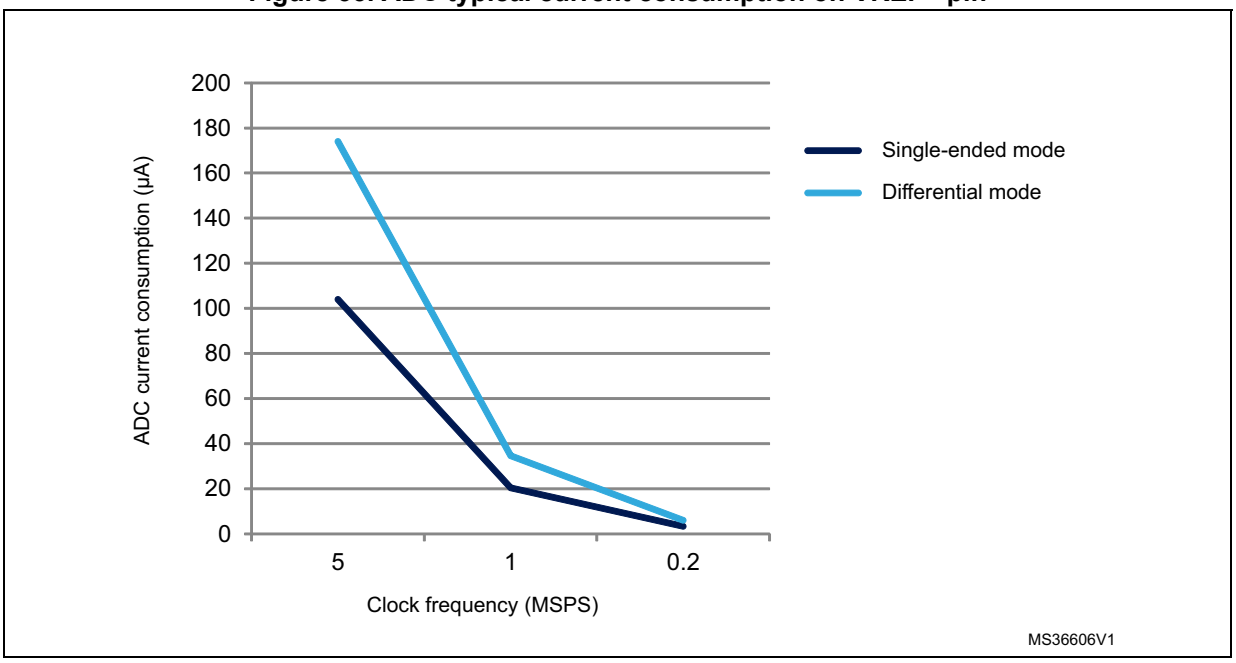



**Figure 33. ADC typical current consumption on VREF+ pin**



### 6.3.19 DAC electrical specifications

**Table 75. DAC characteristics**

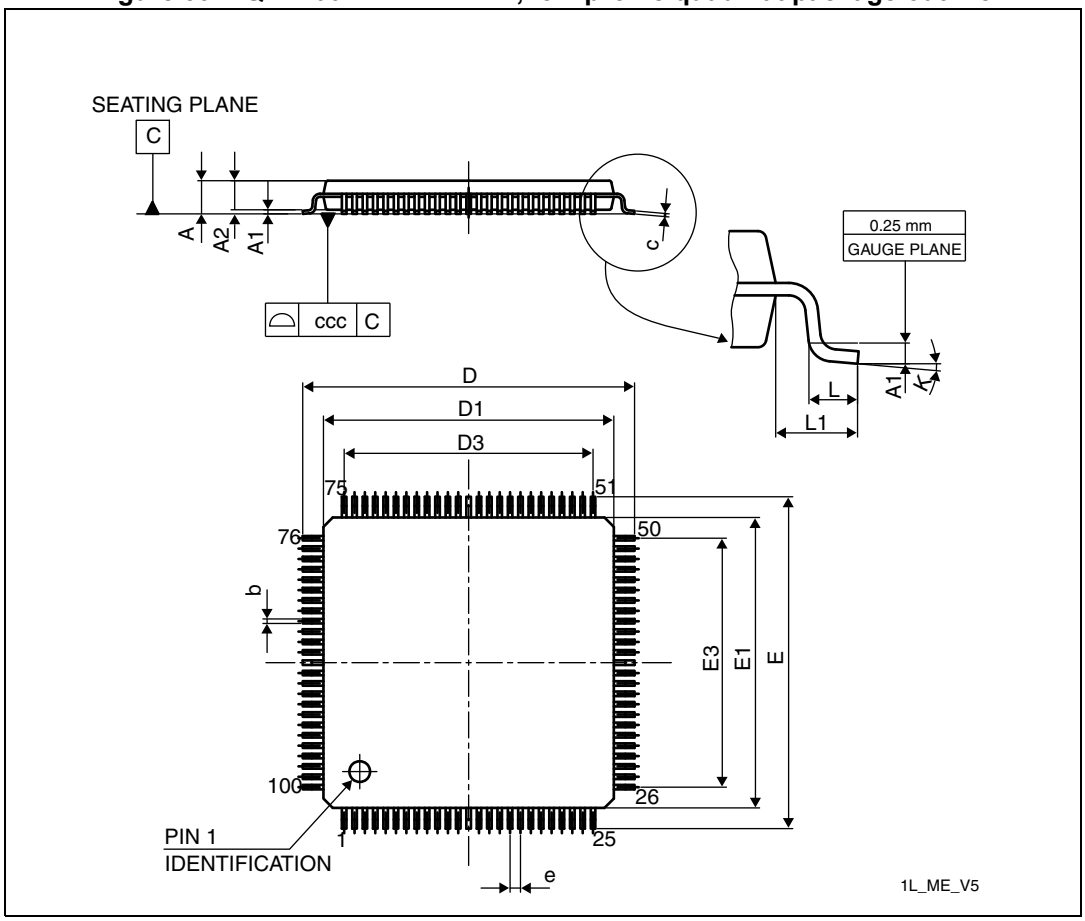
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | | 2.4 | - | 3.6 | V |
| $R_{LOAD}$ (1) | Resistive load | DAC output buffer ON | Connected to $V_{SSA}$ | 5 | - | - | kΩ |
| | | | Connected to $V_{DDA}$ | 25 | - | - | |
| $R_O$ (1) | Output impedance | DAC output buffer OFF | | - | - | 15 | kΩ |
| $C_{LOAD}$ (1) | Capacitive load | DAC output buffer ON | | - | - | 50 | pF |
| $V_{DAC\_OUT}$ (1) | Voltage on DAC_OUT output | Corresponds to 12-bit input code (0x0E0) to (0xF1C) at $V_{DDA}$ = 3.6 V and (0x155) and (0xEAB) at $V_{DDA}$ = 2.4 V DAC output buffer ON. | | 0.2 | - | $V_{DDA}$ – 0.2 | V |
| | | DAC output buffer OFF | | - | 0.5 | $V_{DDA}$ - 1LSB | mV |
| $I_{DDA}$ (3) | DAC DC current consumption in quiescent mode (Standby mode)(2) | With no load, middle code (0x800) on the input. | | - | - | 380 | µA |
| | | With no load, worst code (0xF1C) on the input. | | - | - | 480 | µA |
| DNL (3) | Differential non linearity Difference between two consecutive code-1LSB) | Given for a 10-bit input code | | - | - | ±0.5 | LSB |
| | | Given for a 12-bit input code | | - | - | ±2 | LSB |
| INL (3) | Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095) | Given for a 10-bit input code | | - | - | ±1 | LSB |
| | | Given for a 12-bit input code | | - | - | ±4 | LSB |
| Offset (3) | Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{DDA}$/2) | - | | - | - | ±10 | mV |
| | | Given for a 10-bit input code at $V_{DDA}$ = 3.6 V | | - | - | ±3 | LSB |
| | | Given for a 12-bit input code at $V_{DDA}$ = 3.6 V | | - | - | ±12 | LSB |
| Gain error (3) | Gain error | Given for a 12-bit input code | | - | - | ±0.5 | % |
| $t_{SETTLING}$ (3) | Settling time (full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB | $C_{LOAD} \leq$50 pF, $R_{LOAD} \geq$ 5 kΩ | | - | 3 | 4 | µs |
| Update rate (3) | Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB) | $C_{LOAD} \leq$50 pF, $R_{LOAD} \geq$ 5 kΩ | | - | - | 1 | MS/s |

# 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

## 7.1 LQFP100 – 14 x 14 mm, low-profile quad flat package information

**Figure 39. LQFP100 – 14 x 14 mm, low-profile quad flat package outline**




1. Drawing is not to scale.

**Table 81. LQPF100 – 14 x 14 mm, low-profile quad flat package mechanical data**

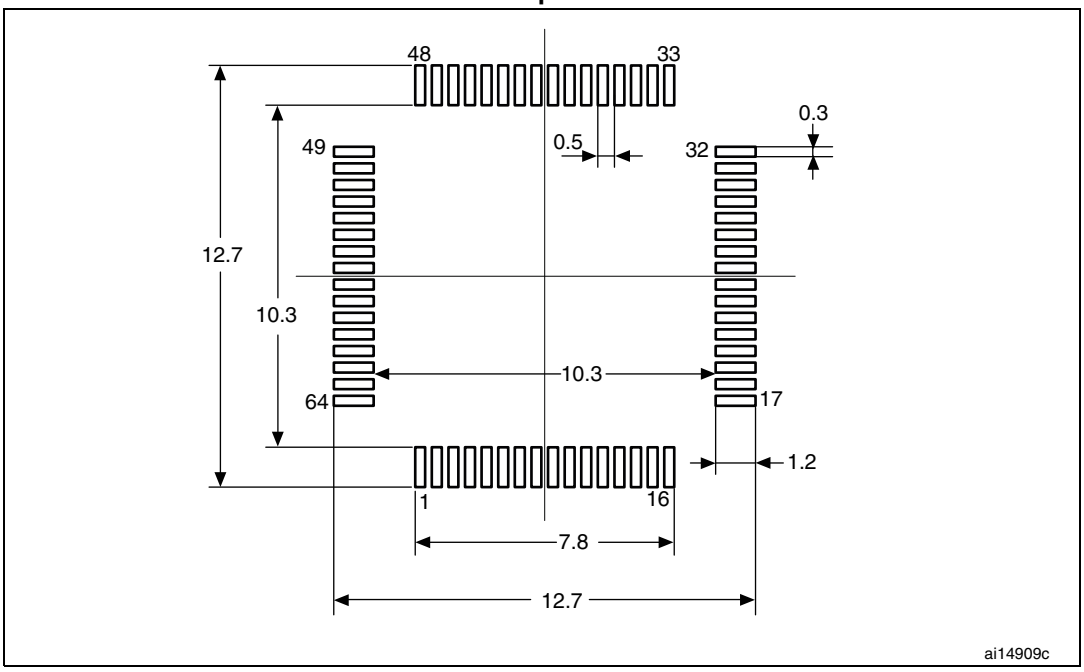
| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.60 | - | - | 0.063 |
| A1 | 0.05 | - | 0.15 | 0.002 | - | 0.0059 |

**Table 82. LQFP64 – 10 x 10 mm, low-profile quad flat package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| E1 | - | 10.00 | - | - | 0.3937 | - |
| E3 | - | 7.50 | - | - | 0.2953 | - |
| e | - | 0.50 | - | - | 0.0197 | - |
| K | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.45 | 0.60 | 0.75 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.00 | - | - | 0.0394 | - |
| ccc | - | - | 0.08 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 43. LQFP64 – 10 x 10 mm, low-profile quad flat package recommended footprint**

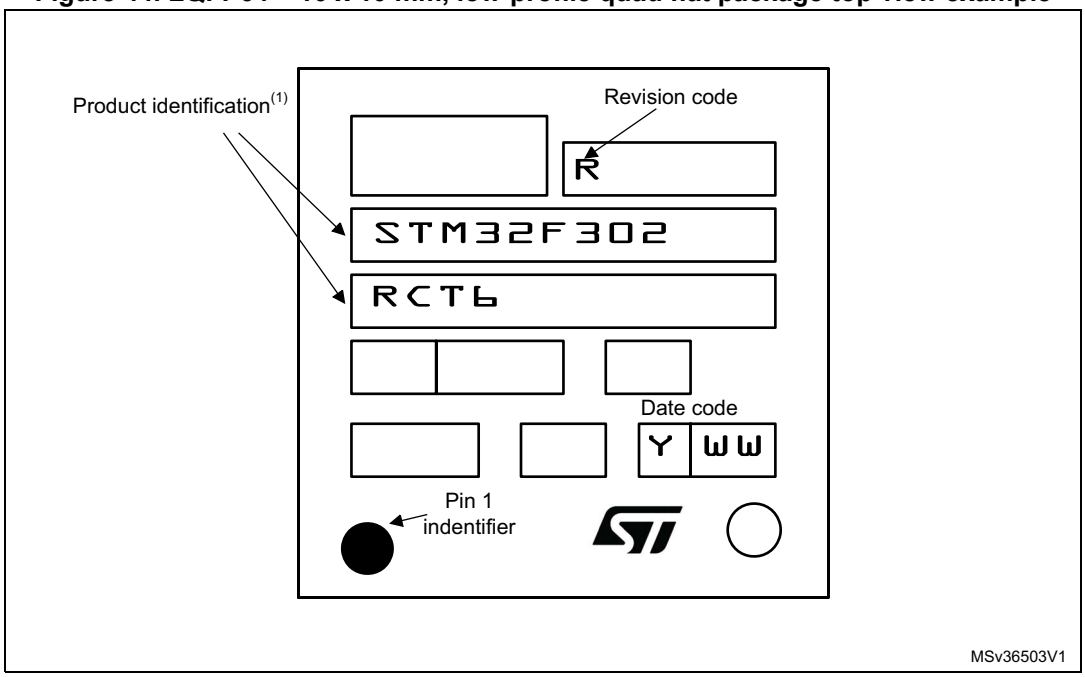



1. Dimensions are in millimeters.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

**Figure 44. LQFP64 – 10 x 10 mm, low-profile quad flat package top view example**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

**Table 88. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 06-May-2016 | 7 | Updated *Figure 5: STM32F302xB/STM32F302xC LQFP64 pinout* replacing VSS by PF4.<br>Updated *Table 13: STM32F302xB/STM32F302xC pin definitions*:<br>– Adding 'digital power supply' in the Pin function column at the line corresponding to K8/28/19 pins.<br>– Adding VSS digital ground line with WLCSP100 K9 and K10 pins connected.<br>– Replacing in VDD line for WLCSP100: 'A10, B10' by 'A9, A10, B10, B8'.<br>Updated *Figure 21: Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port*.<br>Updated *Table 77: Operational amplifier characteristics* high saturation and low saturation voltages.<br>Updated *Table 13: STM32F302xB/STM32F302xC pin definitions* adding note 'Fast ADC channel' for ADCx_IN1..5.<br>Updated *Table 75: DAC characteristics* resistive load.<br>Updated *Table 68: ADC characteristics* adding CMIR parameter and modifying tSTAB parameter characteristics. |