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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 9x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f302cbt7

3.13.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC1_IN17. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

3.13.4 OPAMP reference voltage (VREFOPAMP)

Every OPAMP reference voltage can be measured using a corresponding ADC internal channel: VREFOPAMP1 connected to ADC1 channel 15, VREFOPAMP2 connected to ADC2 channel 17.

3.14 Digital-to-analog converter (DAC)

A single 12-bit buffered DAC channel can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- One DAC output channel
- 8-bit or 10-bit monotonic output
- Left or right data alignment in 12-bit mode
- Noise-wave generation
- Triangular-wave generation
- DMA capability
- External triggers for conversion

3.15 Operational amplifier (OPAMP)

The STM32F302xB/STM32F302xC embeds two operational amplifiers with external or internal follower routing and PGA capability (or even amplifier and filter capability with external components). When an operational amplifier is selected, an external ADC channel is used to enable output measurement.

The operational amplifier features:

- 8.2 MHz bandwidth
- 0.5 mA output capability
- Rail-to-rail input/output
- In PGA mode, the gain can be programmed to be 2, 4, 8 or 16.

3.16 Fast comparators (COMP)

The STM32F302xB/STM32F302xC devices embed four fast rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) and with selectable output polarity.

Table 13. STM32F302xB/STM32F302xC pin definitions (continued)

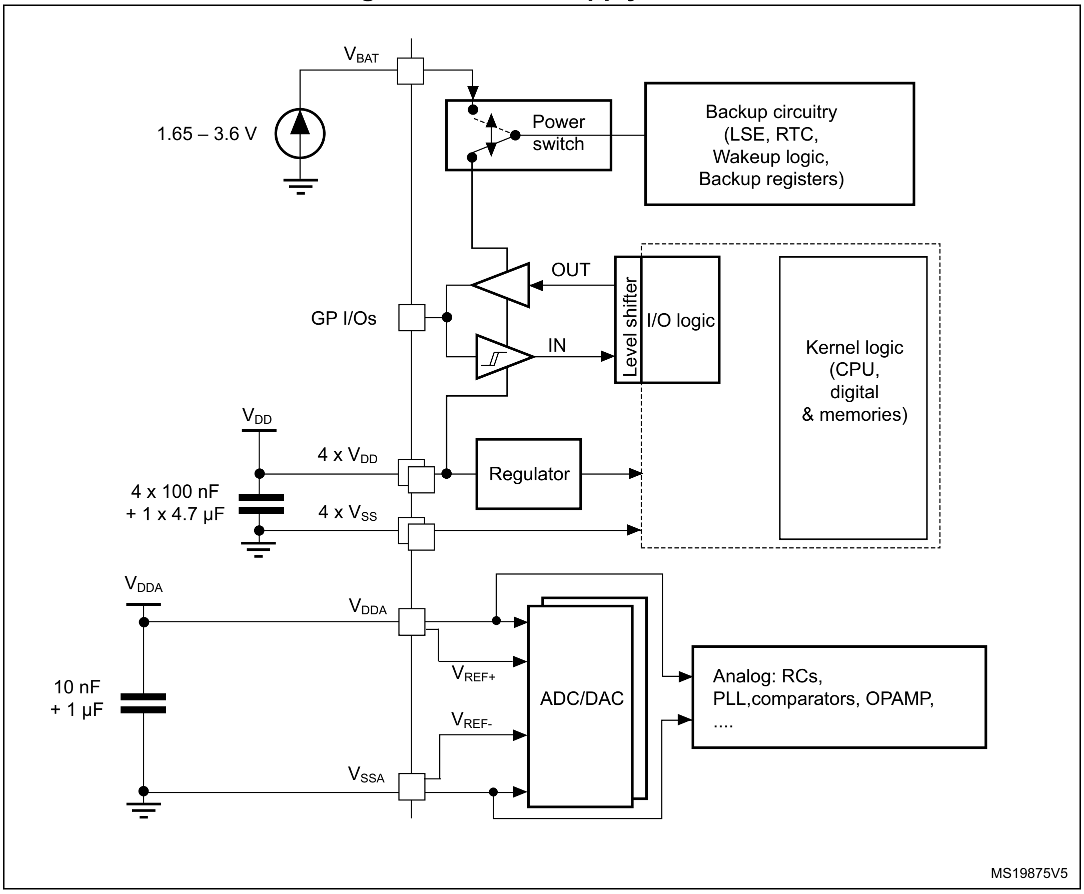
Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
WLCSP100	LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
E2	70	44	32	PA11	I/O	FT	-	USART1_CTS, USB_DM, CAN_RX, TIM1_CH1N, TIM1_CH4, TIM1_BKIN2, TIM4_CH1, COMP1_OUT, EVENTOUT	-
D1	71	45	33	PA12	I/O	FT	-	USART1_RTS_DE, USB_DP, CAN_TX, TIM1_CH2N, TIM1_ETR, TIM4_CH2, TIM16_CH1, COMP2_OUT, EVENTOUT	-
E3	72	46	34	PA13	I/O	FT	-	USART3_CTS, TIM4_CH3, TIM16_CH1N, TSC_G4_IO3, IR_OUT, SWDIO-JTMS, EVENTOUT	-
C1	73	-	-	PF6	I/O	FTf	(1)	I2C2_SCL, USART3_RTS_DE, TIM4_CH4, EVENTOUT	-
A1, A2, B1	74	47	35	VSS	S	-	-	Ground	
D2	75	48	36	VDD	S	-	-	Digital power supply	
C2	76	49	37	PA14	I/O	FTf	-	I2C1_SDA, USART2_TXTIM1_BKIN, TSC_G4_IO4, SWCLK-JTCK, EVENTOUT	-
B2	77	50	38	PA15	I/O	FTf	-	I2C1_SCL, SPI1_NSS, SPI3_NSS, I2S3_WS, JTDI, USART2_RX, TIM1_BKIN, TIM2_CH1_ETR, EVENTOUT	-
E4	78	51	-	PC10	I/O	FT	(1)	SPI3_SCK, I2S3_CK, USART3_TX, UART4_TX, EVENTOUT	-
D3	79	52	-	PC11	I/O	FT	(1)	SPI3_MISO, I2S3ext_SD, USART3_RX, UART4_RX, EVENTOUT	-
A3	80	53	-	PC12	I/O	FT	(1)	SPI3_MOSI, I2S3_SD, USART3_CK, UART5_TX, EVENTOUT	-
B3	81	-	-	PD0	I/O	FT	(1)	CAN_RX, EVENTOUT	-

Table 14. Alternate functions for port A

Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF14	AF15
PA0	-	TIM2_CH1_ETR	-	TSC_G1_IO1	-	-	-	USART2_CTS	COMP1_OUT			-	-	-	EVENT OUT
PA1	RTC_REFIN	TIM2_CH2	-	TSC_G1_IO2	-	-	-	USART2_RTS_DE		TIM15_CH1N	-	-	-	-	EVENT OUT
PA2	-	TIM2_CH3	-	TSC_G1_IO3	-	-	-	USART2_TX	COMP2_OUT	TIM15_CH1	-	-	-	-	EVENT OUT
PA3	-	TIM2_CH4	-	TSC_G1_IO4	-	-	-	USART2_RX	-	TIM15_CH2	-	-	-	-	EVENT OUT
PA4	-	-	TIM3_CH2	TSC_G2_IO1	-	SPI1_NSS	SPI3_NSS, I2S3_WS	USART2_CK	-	-	-	-	-	-	EVENT OUT
PA5	-	TIM2_CH1_ETR	-	TSC_G2_IO2	-	SPI1_SCK	-	-	-	-	-	-	-	-	EVENT OUT
PA6	-	TIM16_CH1	TIM3_CH1	TSC_G2_IO3		SPI1_MISO	TIM1_BKIN	-	COMP1_OUT	-	-	-	-	-	EVENT OUT
PA7	-	TIM17_CH1	TIM3_CH2	TSC_G2_IO4		SPI1_MOSI	TIM1_CH1N	-	COMP2_OUT	-	-	-	-	-	EVENT OUT
PA8	MCO	-	-	-	I2C2_SMBA	I2S2_MCK	TIM1_CH1	USART1_CK		-	TIM4_ETR	-	-	-	EVENT OUT
PA9	-	-	-	TSC_G4_IO1	I2C2_SCL	I2S3_MCK	TIM1_CH2	USART1_TX		TIM15_BKIN	TIM2_CH3	-	-	-	EVENT OUT
PA10	-	TIM17_BKIN	-	TSC_G4_IO2	I2C2_SDA	-	TIM1_CH3	USART1_RX	COMP6_OUT	-	TIM2_CH4		-	-	EVENT OUT
PA11	-	-	-	-	-	-	TIM1_CH1N	USART1_CTS	COMP1_OUT	CAN_RX	TIM4_CH1	TIM1_CH4	TIM1_BKIN2	USB_DM	EVENT OUT

6.1.6 Power supply scheme

Figure 11. Power supply scheme



1. Dotted lines represent the internal connections on low pin count packages, joining the dedicated supply pins.

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc..) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

Table 30. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6V (continued)

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(1)			Typ	Max @ T_A(1)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Sleep mode, executing from Flash or RAM	External clock (HSE bypass)	72 MHz	44.0	48.4	49.4	50.5	6.6	7.5	7.9	8.7	mA
			64 MHz	39.2	43.3	44.0	45.2	6.0	6.8	7.2	7.9	
			48 MHz	29.6	32.7	33.3	34.3	4.5	5.2	5.6	6.3	
			32 MHz	19.7	23.3	23.3	23.5	3.1	3.5	4.0	4.8	
			24 MHz	14.9	17.6	17.8	18.3	2.4	2.8	3.3	3.9	
			8 MHz	4.9	5.7	6.1	6.9	0.8	1.0	1.4	2.2	
			1 MHz	0.6	0.9	1.2	2.1	0.1	0.3	0.6	1.5	
		Internal clock (HSI)	64 MHz	34.2	38.1	39.2	40.3	5.7	6.3	6.8	7.5	
			48 MHz	25.8	28.7	29.6	30.3	4.3	4.8	5.2	5.9	
			32 MHz	17.4	19.4	19.9	20.7	2.9	3.2	3.7	4.5	
			24 MHz	13.2	15.1	15.6	15.9	1.5	1.8	2.2	2.9	
			8 MHz	4.5	5.0	5.6	6.2	0.7	0.9	1.2	2.1	

1. Guaranteed by characterization results unless otherwise specified.
2. Data based on characterization results and tested in production with code executing from RAM.

Table 31. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Parameter	Conditions (1)	f_{HCLK}	V_{DDA} = 2.4 V				V_{DDA} = 3.6 V				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run/Sleep mode, code executing from Flash or RAM	HSE bypass	72 MHz	225	276	289	297	245	302	319	329	µA
			64 MHz	198	249	261	268	216	270	284	293	
			48 MHz	149	195	204	211	159	209	222	230	
			32 MHz	102	145	152	157	110	154	162	169	
			24 MHz	80	119	124	128	86	126	131	135	
			8 MHz	2	3	4	6	3	4	5	9	
			1 MHz	2	3	5	7	3	4	6	9	
		HSI clock	64 MHz	270	323	337	344	299	354	371	381	
			48 MHz	220	269	280	286	244	293	309	318	
			32 MHz	173	218	228	233	193	239	251	257	
			24 MHz	151	194	200	204	169	211	219	225	
			8 MHz	73	97	99	103	88	105	110	116	

1. Current consumption from the V_{DDA} supply is independent of whether the peripherals are on or off. Furthermore when the PLL is off, I_{DDA} is independent from the frequency.
2. Guaranteed by characterization results.

Table 32. Typical and maximum V_{DD} consumption in Stop and Standby modes

Symbol	Parameter	Conditions	Typ @V_{DD} (V_{DD}=V_{DDA})						Max(1)			Unit
			2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, all oscillators OFF	20.05	20.33	20.42	20.50	20.67	20.80	44.2(2)	350	735(2)	µA
		Regulator in low-power mode, all oscillators OFF	7.63	7.77	7.90	8.07	8.17	8.33	30.6(2)	335	720(2)	
	Supply current in Standby mode	LSI ON and IWDG ON	0.80	0.96	1.09	1.23	1.37	1.51	-	-	-	
		LSI OFF and IWDG OFF	0.60	0.74	0.83	0.93	1.02	1.11	5.0(2)	7.8	13.3(2)	

1. Guaranteed by characterization results unless otherwise specified.
2. Data based on characterization results and tested in production.

Table 33. Typical and maximum V_{DDA} consumption in Stop and Standby modes

Symbol	Parameter	Conditions		Typ @V_{DD} (V_{DD} = V_{DDA})						Max(1)			Unit
				2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DDA}	Supply current in Stop mode	V_{DDA} monitoring ON	Regulator in run mode, all oscillators OFF	1.81	1.95	2.07	2.20	2.35	2.52	3.7	5.5	8.8	µA
			Regulator in low-power mode, all oscillators OFF	1.81	1.95	2.07	2.20	2.35	2.52	3.7	5.5	8.8	
	Supply current in Standby mode		LSI ON and IWDG ON	2.22	2.42	2.59	2.78	3.0	3.24	-	-	-	
			LSI OFF and IWDG OFF	1.69	1.82	1.94	2.08	2.23	2.40	3.5	5.4	9.2	
	Supply current in Stop mode	V_{DDA} monitoring OFF	Regulator in run mode, all oscillators OFF	1.05	1.08	1.10	1.15	1.22	1.29	-	-	-	
			Regulator in low-power mode, all oscillators OFF	1.05	1.08	1.10	1.15	1.22	1.29	-	-	-	
	Supply current in Standby mode		LSI ON and IWDG ON	1.44	1.52	1.60	1.71	1.84	1.98	-	-	-	
			LSI OFF and IWDG OFF	0.93	0.95	0.98	1.02	1.08	1.15	-	-	-	

1. Guaranteed by characterization results.

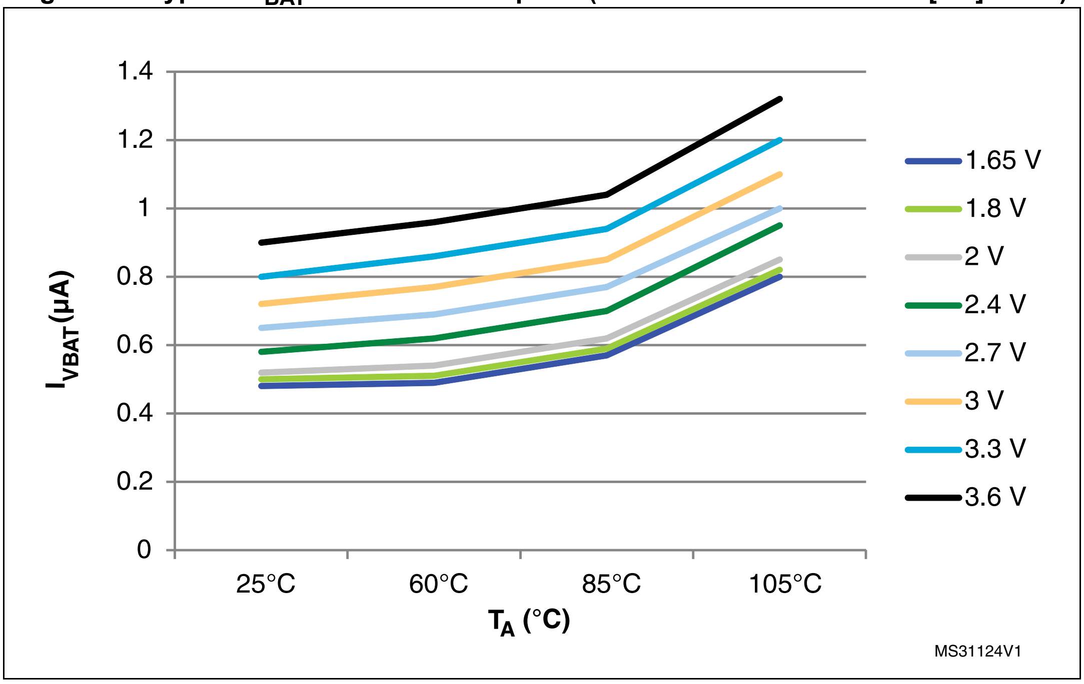
The total consumption is the sum of IDD and IDDA.

Table 34. Typical and maximum current consumption from V_{BAT} supply

Symbol	Para meter	Conditions (1)	Typ @V_{BAT}								Max @V_{BAT} = 3.6 V(2)			Unit
			1.65V	1.8V	2V	2.4V	2.7V	3V	3.3V	3.6V	T_A = 25°C	T_A = 85°C	T_A = 105°C	
I_{DD_VBAT}	Backup domain supply current	LSE & RTC ON; "Xtal mode" lower driving capability; LSEDRV[1:0] = '00'	0.48	0.50	0.52	0.58	0.65	0.72	0.80	0.90	1.1	1.5	2.0	µA
		LSE & RTC ON; "Xtal mode" higher driving capability; LSEDRV[1:0] = '11'	0.83	0.86	0.90	0.98	1.03	1.10	1.20	1.30	1.5	2.2	2.9	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a CL of 6 pF for typical values.
2. Guaranteed by characterization results.

Figure 13. Typical V_{BAT} current consumption (LSE and RTC ON/LSEDRV[1:0] = ’00’)



I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 54: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 38: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Low-speed external user clock generated from an external source

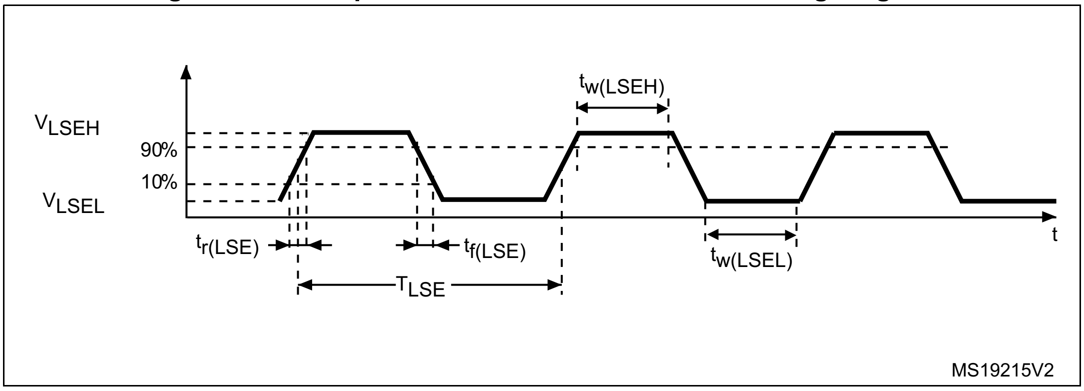
In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 15*

Table 41. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	

1. Guaranteed by design.

Figure 15. Low-speed external clock source AC timing diagram



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 22*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 22*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 55* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 24*. All I/Os (FT, TTa and TC unless otherwise specified) are CMOS and TTL compliant.

Table 55. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL} (1)	Output low level voltage for an I/O pin	CMOS port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin	TTL port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	
V_{OH} (3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL} (1)(4)	Output low level voltage for an I/O pin	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	
V_{OH} (3)(4)	Output high level voltage for an I/O pin		V_{DD}–1.3	-	
V_{OL} (1)(4)	Output low level voltage for an I/O pin	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	
V_{OH} (3)(4)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OLFM+} (1)(4)	Output low level voltage for an FTf I/O pin in FM+ mode	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 22* and the sum of I_{IO} (I/O ports and control pins) must not exceed $\Sigma I_{IO(PIN)}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 22* and the sum of I_{IO} (I/O ports and control pins) must not exceed $\Sigma I_{IO(PIN)}$.
4. Data based on design simulation.

SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 63* for SPI or in *Table 64* for I²S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 24*.

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 63. SPI characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode, SPI1 $2.7<V_{DD}<3.6$	-	-	24	MHz
		Slave mode, SPI1 $2.7<V_{DD}<3.6$			24	
		Master mode, SPI1/2/3 $2<V_{DD}<3.6$			18	
		Slave mode, SPI1/2/3 $2<V_{DD}<3.6$			18	
DuCy(SCK)	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	5.5	-	-	
$t_{su(SI)}$		Slave mode	6.5	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	5	-	-	
$t_{h(SI)}$		Slave mode	5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	0	-	4*Tpclk	
$t_{dis(SO)}$	Data output disable time	Slave mode	0	-	24	
$t_{v(SO)}$	Data output valid time	Slave mode	-	12	27	
		Slave mode, SPI1 $2.7<V_{DD}<3.6V$	-	12	18	
$t_{v(MO)}$		Master mode	-	1.5	3	
$t_{h(SO)}$	Data output hold time	Slave mode	11	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. Guaranteed by characterization results.

Table 71. ADC accuracy, 100-pin packages[(1)(2)(3)] (continued)

Symbol	Parameter	Conditions			Min [(4)]	Max[(4)]	Unit
SINAD [(5)]	Signal-to-noise and distortion ratio	ADC clock freq. ≤ 72 MHz, Sampling freq. ≤ 5 Msps, 2 V ≤ V_{DDA}, V_{REF+} ≤ 3.6 V 100-pin package	Single Ended	Fast channel 5.1 Ms	64	-	dB
				Slow channel 4.8 Ms	63	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
SNR[(5)]	Signal-to-noise ratio		Single Ended	Fast channel 5.1 Ms	64	-	
				Slow channel 4.8 Ms	64	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
THD[(5)]	Total harmonic distortion		Single Ended	Fast channel 5.1 Ms	-	-74	
				Slow channel 4.8 Ms	-	-74	
			Differential	Fast channel 5.1 Ms	-	-78	
				Slow channel 4.8 Ms	-	-76	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.14* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Guaranteed by characterization results.
5. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

6.3.23 V_{BAT} monitoring characteristics

Table 80. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	2	-	
Er[(1)]	Error on Q	-1	-	+1	%
T_{S_vbat}[(1)(2)]	ADC sampling time when reading the V_{BAT} 1mV accuracy	2.2	-	-	µs

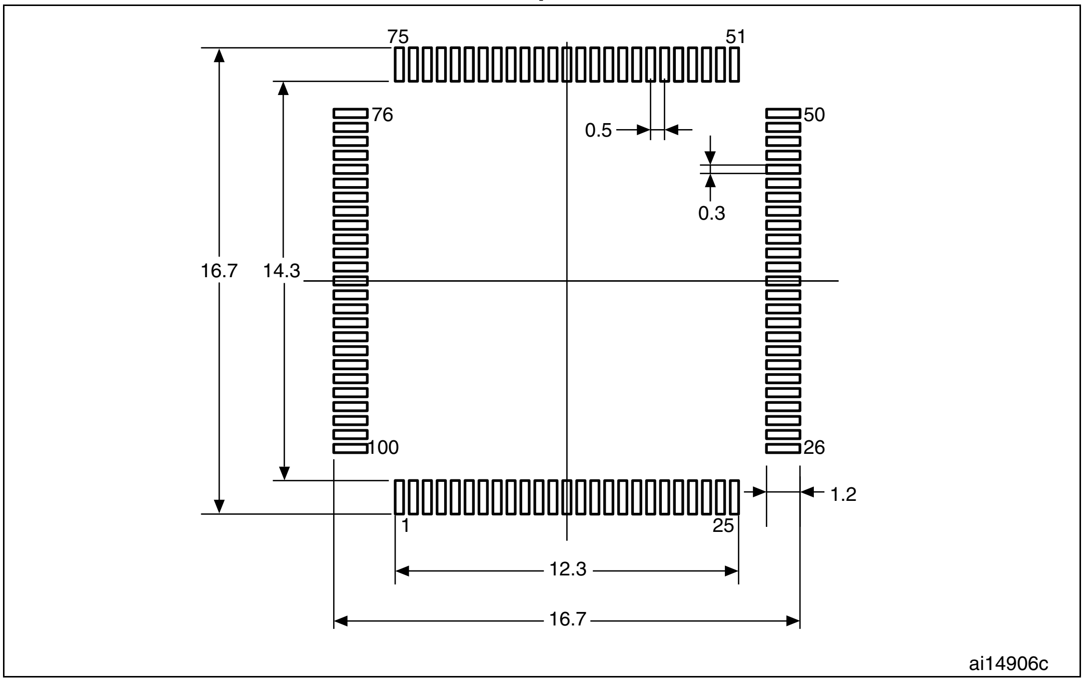
1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

Table 81. LQPF100 – 14 x 14 mm, low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09	-	0.2	0.0035	-	0.0079
D	15.80	16.00	16.2	0.622	0.6299	0.6378
D1	13.80	14.00	14.2	0.5433	0.5512	0.5591
D3	-	12.00	-	-	0.4724	-
E	15.80	16.00	16.2	0.622	0.6299	0.6378
E1	13.80	14.00	14.2	0.5433	0.5512	0.5591
E3	-	12.00	-	-	0.4724	-
e	-	0.50	-	-	0.0197	-
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	-	1.00	-	-	0.0394	-
K	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 40. LQFP100 – 14 x 14 mm, low-profile quad flat package recommended footprint

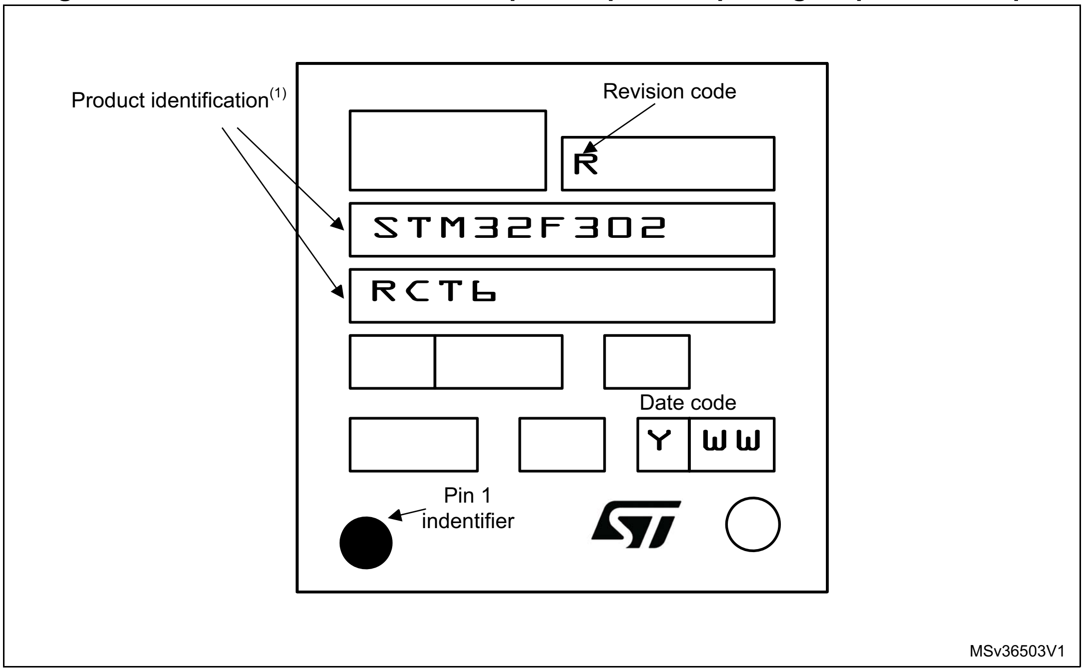


1. Dimensions are in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 44. LQFP64 – 10 x 10 mm, low-profile quad flat package top view example

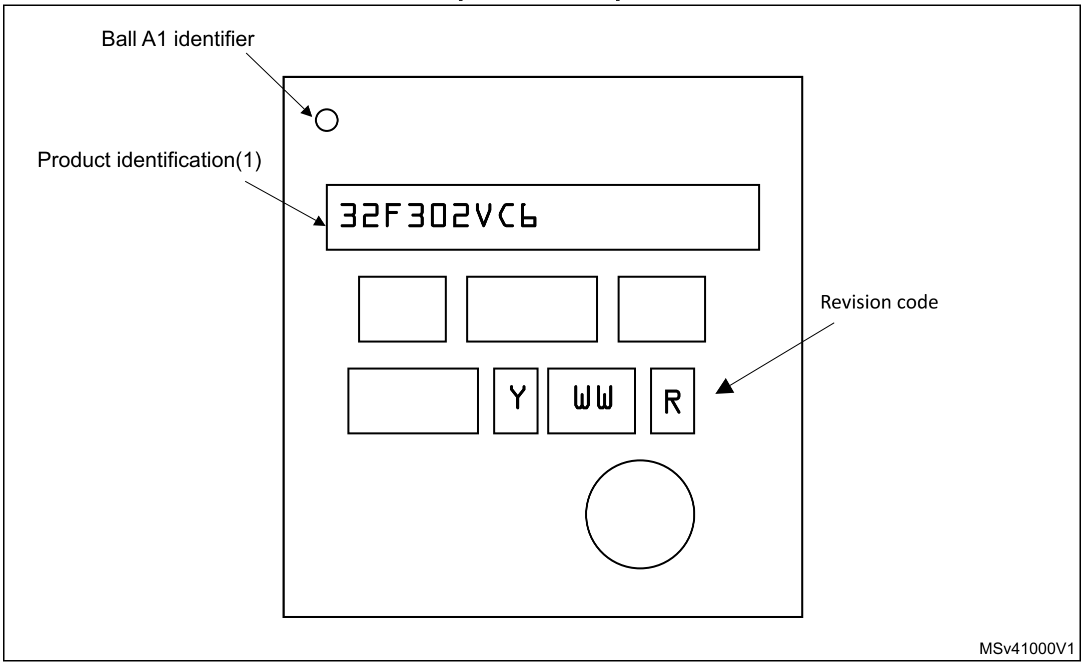


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Marking of engineering samples

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Figure 50. WLCSP100, 0.4 mm pitch wafer level chip scale package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 88. Document revision history (continued)

Date	Revision	Changes
29-Jan-2015	4	Updated cover page with ADC up to 17 channels. Updated *Section 6.3.20: Comparator characteristics* modifying ts_sc characteristics in *Table 76* and adding *Figure 37: Maximum VREFINT scaler startup time from power down*. Updated I_{DD} data in *Table 42: HSE oscillator characteristics*.
17-Apr-2015	5	Updated *Figure 1: STM32F302xB/STM32F302xC block diagram* changing 32 KB of SRAM by 40 KB of SRAM. Updated *Section 7: Package information*: with new package information structure adding 1 sub paragraph for each package. Updated *Figure 41: LQFP100 – 14 x 14 mm, low-profile quad flat package top view example* removing gate mark. Added note for all package device markings: "the following figure gives an example of topside marking orientation versus pin 1 identifier location". Updated *Table 82: LQFP64 – 10 x 10 mm, low-profile quad flat package mechanical data*. Updated *Table 7: STM32F302xB/STM32F302xC peripheral interconnect matrix* removing TIM8 reference and updating note below the table, replacing by a reference to RM0365.
22-Feb-2016	6	Added WLCSP100: – Updated cover page. – Updated *Table 2: STM32F302xx family device features and peripheral counts*. – Added *Figure 7: STM32F302xB/STM32F302xC WLCSP100 pinout*. – Updated *Table 13: STM32F302xB/STM32F302xC pin definitions*. – Updated *Table 24: General operating conditions*. – Added *Section 7.4: WLCSP100 - 0.4 mm pitch wafer level chip scale package information*. – Updated *Table 86: Package thermal characteristics*. – Updated *Table 87: Ordering information scheme*. Updated *Figure 4*, *Figure 5*, *Figure 6*, *Table 13* and *Table 22* removing all VDD and VSS indexes. Updated all the notes removing 'not tested in production'. Updated *Table 68: ADC characteristics* adding V_{REF-} negative voltage reference. Updated *Table 21: Voltage characteristics* adding table note 4. Updated *Table 43: LSE oscillator characteristics (fLSE = 32.768 kHz)* LSEDRV[1:0] bits. Updated *Table 28: Embedded internal reference voltage* V_{REFINT} internal reference voltage (min and typ values). Updated *Table 51: ESD absolute maximum ratings* ESD CDM at class 3 and 4 including WLCSP100 package information.