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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	37
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 9x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f302cct6tr

Contents

Figure 5. STM32F302xB/STM32F302xC LQFP64 pinout

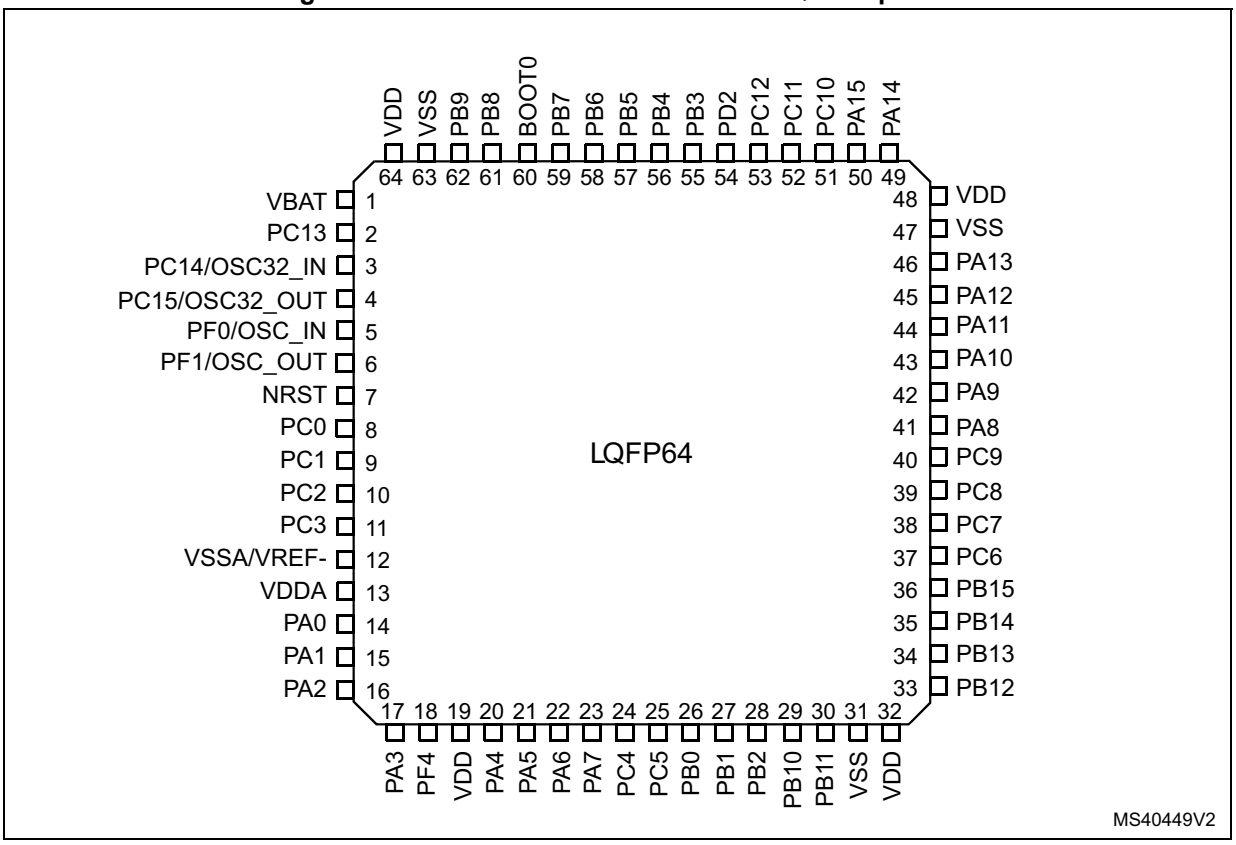


Figure 6. STM32F302xB/STM32F302xC LQFP100 pinout

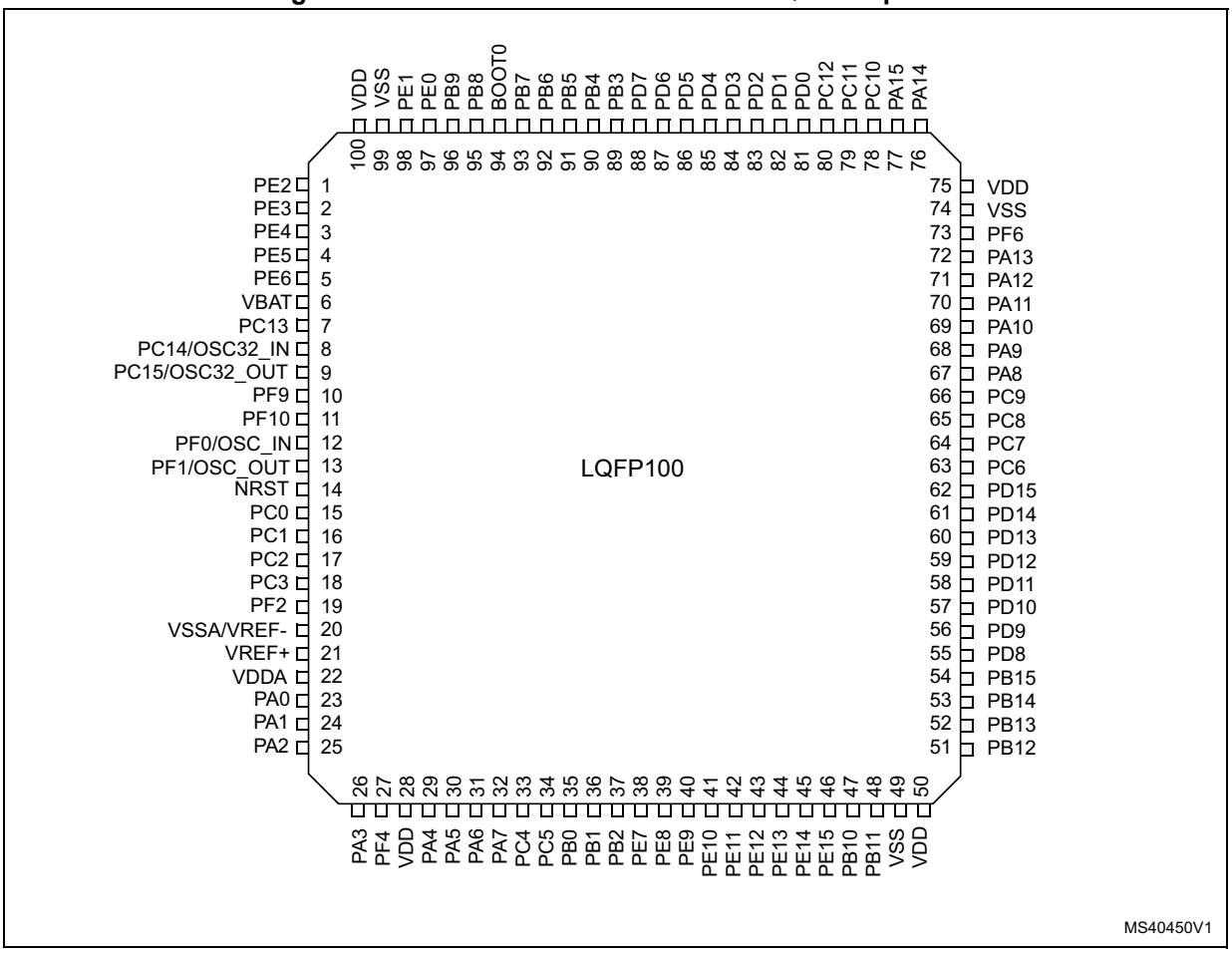


Table 13. STM32F302xB/STM32F302xC pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
WLCSP100	LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
J9	24	15	11	PA1	I/O	TTa	(4)	USART2_RTS_DE, TIM2_CH2, TSC_G1_IO2, TIM15_CH1N, RTC_REFIN, EVENTOUT	ADC1_IN2, COMP1_INP, OPAMP1_VINP
F7	25	16	12	PA2	I/O	TTa	(4) (5)	USART2_TX, TIM2_CH3, TIM15_CH1, TSC_G1_IO3, COMP2_OUT, EVENTOUT	ADC1_IN3, COMP2_INM, OPAMP1_VOUT
G7	26	17	13	PA3	I/O	TTa	(4)	USART2_RX, TIM2_CH4, TIM15_CH2, TSC_G1_IO4, EVENTOUT	ADC1_IN4, OPAMP1_VINP, COMP2_INP, OPAMP1_VINM
-	27	18	-	PF4	I/O	TTa	**(1)** (4)	COMP1_OUT, EVENTOUT	ADC1_IN5
K9, K10	-	-	-	VSS	S	-	-	Digital ground	
K8	28	19	-	VDD	S	**-**	**-**	Digital power supply	
J7	29	20	14	PA4	I/O	TTa	(4) (5)	SPI1_NSS, SPI3_NSS,I2S3_WS, USART2_CK, TSC_G2_IO1, TIM3_CH2, EVENTOUT	ADC2_IN1, DAC1_OUT1, COMP1_INM, COMP2_INM, COMP4_INM, COMP6_INM
H7	30	21	15	PA5	I/O	TTa	(4) (5)	SPI1_SCK, TIM2_CH1_ETR, TSC_G2_IO2, EVENTOUT	ADC2_IN2 OPAMP1_VINP, OPAMP2_VINM COMP1_INM, COMP2_INM, COMP4_INM, COMP6_INM
H6	31	22	16	PA6	I/O	TTa	(4) (5)	SPI1_MISO, TIM3_CH1, TIM1_BKIN, TIM16_CH1, COMP1_OUT, TSC_G2_IO3, EVENTOUT	ADC2_IN3, OPAMP2_VOUT
K7	32	23	17	PA7	I/O	TTa	(4)	SPI1_MOSI, TIM3_CH2, TIM17_CH1, TIM1_CH1N, , TSC_G2_IO4, COMP2_OUT, EVENTOUT	ADC2_IN4, COMP2_INP, OPAMP2_VINP, OPAMP1_VINP
G6	33	24	-	PC4	I/O	TTa	**(1)** (4)	USART1_TX, EVENTOUT	ADC2_IN5
F6	34	25	-	PC5	I/O	TTa	**(1)**	USART1_RX, TSC_G3_IO1, EVENTOUT	ADC2_IN11, OPAMP2_VINM, OPAMP1_VINM
J6	35	26	18	PB0	I/O	TTa	-	TIM3_CH3, TIM1_CH2N, TSC_G3_IO2, EVENTOUT	COMP4_INP, OPAMP2_VINP

Table 13. STM32F302xB/STM32F302xC pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
WLCSP100	LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
C3	82	-	-	PD1	I/O	FT	(1)	CAN_TX, EVENTOUT	-
A4	83	54	-	PD2	I/O	FT	(1)	UART5_RX, TIM3_ETR, EVENTOUT	-
B4	84	-	-	PD3	I/O	FT	(1)	USART2_CTS, TIM2_CH1_ETR, EVENTOUT	-
C4	85	-	-	PD4	I/O	FT	(1)	USART2_RTS_DE, TIM2_CH2, EVENTOUT	-
-	86	-	-	PD5	I/O	FT	(1)	USART2_TX, EVENTOUT	-
-	87	-	-	PD6	I/O	FT	(1)	USART2_RX, TIM2_CH4, EVENTOUT	-
D4	88	-	-	PD7	I/O	FT	(1)	USART2_CK, TIM2_CH3, EVENTOUT	-
A5	89	55	39	PB3	I/O	FT	-	SPI3_SCK, I2S3_CK, SPI1_SCK, USART2_TX, TIM2_CH2, TIM3_ETR, TIM4_ETR, TSC_G5_IO1, JTDO-TRACESWO, EVENTOUT	-
B5	90	56	40	PB4	I/O	FT	-	SPI3_MISO, I2S3ext_SD, SPI1_MISO, USART2_RX, TIM3_CH1, TIM16_CH1, TIM17_BKIN, TSC_G5_IO2, NJTRST, EVENTOUT	-
A6	91	57	41	PB5	I/O	FT	-	SPI3_MOSI, SPI1_MOSI, I2S3_SD, I2C1_SMBA, USART2_CK, TIM16_BKIN, TIM3_CH2, TIM17_CH1, EVENTOUT	-
B6	92	58	42	PB6	I/O	FTf	-	I2C1_SCL, USART1_TX, TIM16_CH1N, TIM4_CH1, TSC_G5_IO3EVENTOUT	-
C5	93	59	43	PB7	I/O	FTf	-	I2C1_SDA, USART1_RX, TIM3_CH4, TIM4_CH2, TIM17_CH1N, TSC_G5_IO4, EVENTOUT	-
A7	94	60	44	BOOT0	I	B	-	Boot memory selection	

Table 14. Alternate functions for port A

Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF14	AF15
PA0	-	TIM2_ CH1_ ETR	-	TSC_ G1_IO1	-	-	-	USART2_ CTS	COMP1 _OUT			-	-	-	EVENT OUT
PA1	RTC_ REFIN	TIM2_ CH2	-	TSC_ G1_IO2	-	-	-	USART2_ RTS_DE		TIM15_ CH1N	-	-	-	-	EVENT OUT
PA2	-	TIM2_ CH3	-	TSC_ G1_IO3	-	-	-	USART2_ TX	COMP2 _OUT	TIM15_ CH1	-	-	-	-	EVENT OUT
PA3	-	TIM2_ CH4	-	TSC_ G1_IO4	-	-	-	USART2_ RX	-	TIM15_ CH2	-	-	-	-	EVENT OUT
PA4	-	-	TIM3_ CH2	TSC_ G2_IO1	-	SPI1_ NSS	SPI3_NSS, I2S3_WS	USART2_ CK	-	-	-	-	-	-	EVENT OUT
PA5	-	TIM2_ CH1_ ETR	-	TSC_ G2_IO2	-	SPI1_ SCK	-	-	-	-	-	-	-	-	EVENT OUT
PA6	-	TIM16_ CH1	TIM3_ CH1	TSC_ G2_IO3		SPI1_ MISO	TIM1_BKIN	-	COMP1 _OUT	-	-	-	-	-	EVENT OUT
PA7	-	TIM17_ CH1	TIM3_ CH2	TSC_ G2_IO4		SPI1_ MOSI	TIM1_CH1N	-	COMP2 _OUT	-	-	-	-	-	EVENT OUT
PA8	MCO	-	-	-	I2C2_ SMBA	I2S2_ MCK	TIM1_CH1	USART1_ CK		-	TIM4_ ETR	-	-	-	EVENT OUT
PA9	-	-	-	TSC_ G4_IO1	I2C2_ SCL	I2S3_ MCK	TIM1_CH2	USART1_ TX		TIM15_ BKIN	TIM2_ CH3	-	-	-	EVENT OUT
PA10	-	TIM17_ BKIN	-	TSC_ G4_IO2	I2C2_ SDA	-	TIM1_CH3	USART1_ RX	COMP6 _OUT	-	TIM2_ CH4		-	-	EVENT OUT
PA11	-	-	-	-	-	-	TIM1_CH1N	USART1_ CTS	COMP1 _OUT	CAN_RX	TIM4_ CH1	TIM1_CH4	TIM1_ BKIN2	USB_ DM	EVENT OUT

Table 17. Alternate functions for port D

Port & Pin Name	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	EVENTOUT	-	-	-	-	-	CAN_RX
PD1	EVENTOUT	-	-		-		CAN_TX
PD2	EVENTOUT	TIM3_ETR	-		UART5_RX	-	-
PD3	EVENTOUT	TIM2_CH1_ETR	-	-	-	-	USART2_CTS
PD4	EVENTOUT	TIM2_CH2	-	-	-	-	USART2_RTS_DE
PD5	EVENTOUT	-	-	-	-	-	USART2_TX
PD6	EVENTOUT	TIM2_CH4	-	-	-	-	USART2_RX
PD7	EVENTOUT	TIM2_CH3	-	-	-	-	USART2_CK
PD8	EVENTOUT	-	-	-	-	-	USART3_TX
PD9	EVENTOUT	-	-	-	-	-	USART3_RX
PD10	EVENTOUT	-	-	-	-	-	USART3_CK
PD11	EVENTOUT	-	-	-	-	-	USART3_CTS
PD12	EVENTOUT	TIM4_CH1	TSC_G8_IO1	-	-	-	USART3_RTS_DE
PD13	EVENTOUT	TIM4_CH2	TSC_G8_IO2	-	-	-	-
PD14	EVENTOUT	TIM4_CH3	TSC_G8_IO3	-	-	-	-
PD15	EVENTOUT	TIM4_CH4	TSC_G8_IO4	-	-	SPI2_NSS	-

Table 20. STM32F302xB/STM32F302xC memory map, peripheral register boundary addresses

Bus	Boundary address	Size (bytes)	Peripheral
	0x5000 0400 - 0x5000 07FF	1 K	Reserved
AHB3	0x5000 0000 - 0x5000 03FF	1 K	ADC1 - ADC2
	0x4800 1800 - 0x4FFF FFFF	~132 M	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1 K	GPIOF
	0x4800 1000 - 0x4800 13FF	1 K	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1 K	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 K	GPIOC
	0x4800 0400 - 0x4800 07FF	1 K	GPIOB
	0x4800 0000 - 0x4800 03FF	1 K	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 M	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 K	TSC
	0x4002 3400 - 0x4002 3FFF	3 K	Reserved
	0x4002 3000 - 0x4002 33FF	1 K	CRC
	0x4002 2400 - 0x4002 2FFF	3 K	Reserved
	0x4002 2000 - 0x4002 23FF	1 K	Flash interface
	0x4002 1400 - 0x4002 1FFF	3 K	Reserved
	0x4002 1000 - 0x4002 13FF	1 K	RCC
	0x4002 0800 - 0x4002 0FFF	2 K	Reserved
	0x4002 0400 - 0x4002 07FF	1 K	DMA2
	0x4002 0000 - 0x4002 03FF	1 K	DMA1
	0x4001 8000 - 0x4001 FFFF	32 K	Reserved
APB2	0x4001 4C00 - 0x4001 7FFF	13 K	Reserved
	0x4001 4800 - 0x4001 4BFF	1 K	TIM17
	0x4001 4400 - 0x4001 47FF	1 K	TIM16
	0x4001 4000 - 0x4001 43FF	1 K	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 K	Reserved
	0x4001 3800 - 0x4001 3BFF	1 K	USART1
	0x4001 3400 - 0x4001 37FF	1 K	Reserved
	0x4001 3000 - 0x4001 33FF	1 K	SPI1
	0x4001 2C00 - 0x4001 2FFF	1 K	TIM1
	0x4001 0800 - 0x4001 2BFF	9 K	Reserved
	0x4001 0400 - 0x4001 07FF	1 K	EXTI
	0x4001 0000 - 0x4001 03FF	1 K	SYSCFG + COMP + OPAMP

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 9. Pin loading conditions

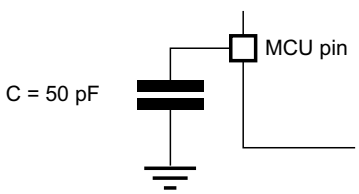
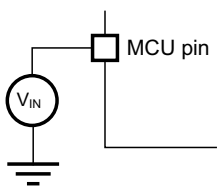


Figure 10. Pin input voltage



On-chip peripheral current consumption

The MCU is placed under the following conditions:

- all I/O pins are in analog input configuration
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature at 25°C and $V_{DD} = V_{DDA} = 3.3$ V.

Table 38. Peripheral current consumption

Peripheral	Typical consumption(1)	Unit
	I_{DD}	
BusMatrix (2)	12.6	µA/MHz
DMA1	7.6	
DMA2	6.1	
CRC	2.1	
GPIOA	10.0	
GPIOB	10.3	
GPIOC	2.2	
GPIOD	8.8	
GPIOE	3.3	
GPIOF	3.0	
TSC	5.5	
ADC1&2	17.3	
APB2-Bridge (3)	3.6	
SYSCFG	7.3	
TIM1	40.0	
SPI1	8.8	
USART1	23.3	
TIM15	17.1	
TIM16	10.1	
TIM17	11.0	
APB1-Bridge (3)	6.1	
TIM2	49.1	
TIM3	38.8	
TIM4	38.3	

6.3.6 Wakeup time from low-power mode

The wakeup times given in *Table 39* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep mode: the wakeup event is WFE.
- WKUP1 (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 24*.

Table 39. Low-power mode wakeup timings

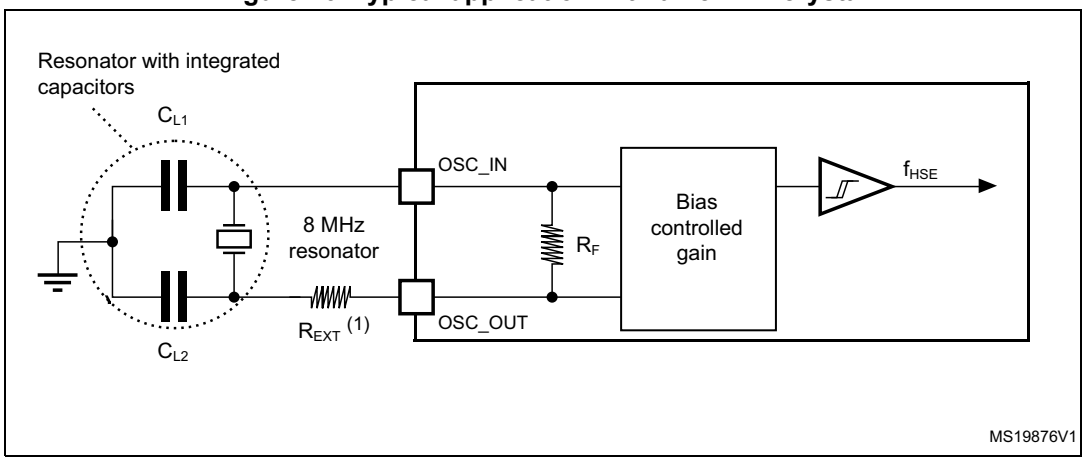
Symbol	Parameter	Conditions	Typ @V_{DD}, V_{DD} = V_{DDA}						Max	Unit
			2.0 V	2.4 V	2.7 V	3 V	3.3 V	3.6 V		
t_{WUSTOP}	Wakeup from Stop mode	Regulator in run mode	4.1	3.9	3.8	3.7	3.6	3.5	4.5	µs
		Regulator in low-power mode	7.9	6.7	6.1	5.7	5.4	5.2	9	
$t_{WUSTANDBY}$(1)	Wakeup from Standby mode	LSI and IWDG OFF	69.2	60.3	56.4	53.7	51.7	50	100	
$t_{WUSLEEP}$	Wakeup from Sleep mode	-	6						-	CPU clock cycles

1. Guaranteed by characterization results.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 16*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 16. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

6.3.9 PLL characteristics

The parameters given in *Table 46* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 24*.

Table 46. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock(1)	1(2)	-	24(2)	MHz
	PLL input clock duty cycle	40(2)	-	60(2)	%
f_{PLL_OUT}	PLL multiplier output clock	16(2)	-	72	MHz
t_{LOCK}	PLL lock time	-	-	200(2)	µs
Jitter	Cycle-to-cycle jitter	-	-	300(2)	ps

1. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.
2. Guaranteed by design.

6.3.10 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 47. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	53.5	60	µs
t_{ERASE}	Page (2 KB) erase time	T_A = –40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA

1. Guaranteed by design.

Table 48. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycles(2) at T_A = 55 °C	20	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 54* are derived from tests performed under the conditions summarized in *Table 24*. All I/Os are CMOS and TTL compliant.

Table 54. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	$0.3\ V_{DD}+0.07$ (1)	V
		FT and FTf I/O	-	-	$0.475\ V_{DD}-0.2$ (1)	
		BOOT0	-	-	$0.3\ V_{DD}–0.3$ (1)	
		All I/Os except BOOT0	-	-	$0.3\ V_{DD}$ (2)	
V_{IH}	High level input voltage	TC and TTa I/O	$0.445\ V_{DD}+0.398$ (1)	-	-	
		FT and FTf I/O	$0.5\ V_{DD}+0.2$ (1)	-	-	
		BOOT0	$0.2\ V_{DD}+0.95$ (1)	-	-	
		All I/Os except BOOT0	$0.7\ V_{DD}$ (2)	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	200 (1)	-	mV
		FT and FTf I/O	-	100 (1)	-	
		BOOT0	-	300 (1)	-	
I_{lkg}	Input leakage current (3)	TC, FT and FTf I/O TTa I/O in digital mode $V_{SS} \le V_{IN} \le V_{DD}$	-	-	±0.1	µA
		TTa I/O in digital mode $V_{DD} \le V_{IN} \le V_{DDA}$	-	-	1	
		TTa I/O in analog mode $V_{SS} \le V_{IN} \le V_{DDA}$	-	-	±0.2	
		FT and FTf I/O(4) $V_{DD} \le V_{IN} \le 5$ V	-	-	10	
R_{PU}	Weak pull-up equivalent resistor(5)	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN} = V_{DD}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation.
2. Tested in production.
3. Leakage could be higher than the maximum value. if negative current is injected on adjacent pins. Refer to *Table 53: I/O current injection susceptibility*.
4. To sustain a voltage higher than V_{DD} +0.3 V, the internal pull-up/pull-down resistors must be disabled.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 22*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 22*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 55* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 24*. All I/Os (FT, TTa and TC unless otherwise specified) are CMOS and TTL compliant.

Table 55. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin	CMOS port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin	TTL port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	
V_{OH} (3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(1)(4)	Output low level voltage for an I/O pin	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	
V_{OH}(3)(4)	Output high level voltage for an I/O pin		V_{DD}–1.3	-	
V_{OL}(1)(4)	Output low level voltage for an I/O pin	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	
V_{OH}(3)(4)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OLFM+}(1)(4)	Output low level voltage for an FTf I/O pin in FM+ mode	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 22* and the sum of I_{IO} (I/O ports and control pins) must not exceed $\Sigma I_{IO(PIN)}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 22* and the sum of I_{IO} (I/O ports and control pins) must not exceed $\Sigma I_{IO(PIN)}$.
4. Data based on design simulation.

Table 71. ADC accuracy, 100-pin packages(1)(2)(3)

Symbol	Parameter	Conditions			Min (4)	Max(4)	Unit
ET	Total unadjusted error	ADC clock freq. ≤ 72 MHz, Sampling freq. ≤ 5 Msps 2 V ≤ V_{DDA} , V_{REF+} ≤ 3.6 V 100-pin package	Single Ended	Fast channel 5.1 Ms	-	±6.5	LSB
				Slow channel 4.8 Ms	-	±6.5	
			Differential	Fast channel 5.1 Ms	-	±4	
				Slow channel 4.8 Ms	-	±4	
EO	Offset error		Single Ended	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3	
			Differential	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±2	
EG	Gain error		Single Ended	Fast channel 5.1 Ms	-	±6	
				Slow channel 4.8 Ms	-	±6	
			Differential	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3	
ED	Differential linearity error		Single Ended	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	
			Differential	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	
EL	Integral linearity error		Single Ended	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±3	
			Differential	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±2	
ENOB (5)	Effective number of bits		Single Ended	Fast channel 5.1 Ms	10.4	-	bits
				Slow channel 4.8 Ms	10.2	-	
			Differential	Fast channel 5.1 Ms	10.8	-	
				Slow channel 4.8 Ms	10.8	-	

Figure 34. ADC accuracy characteristics

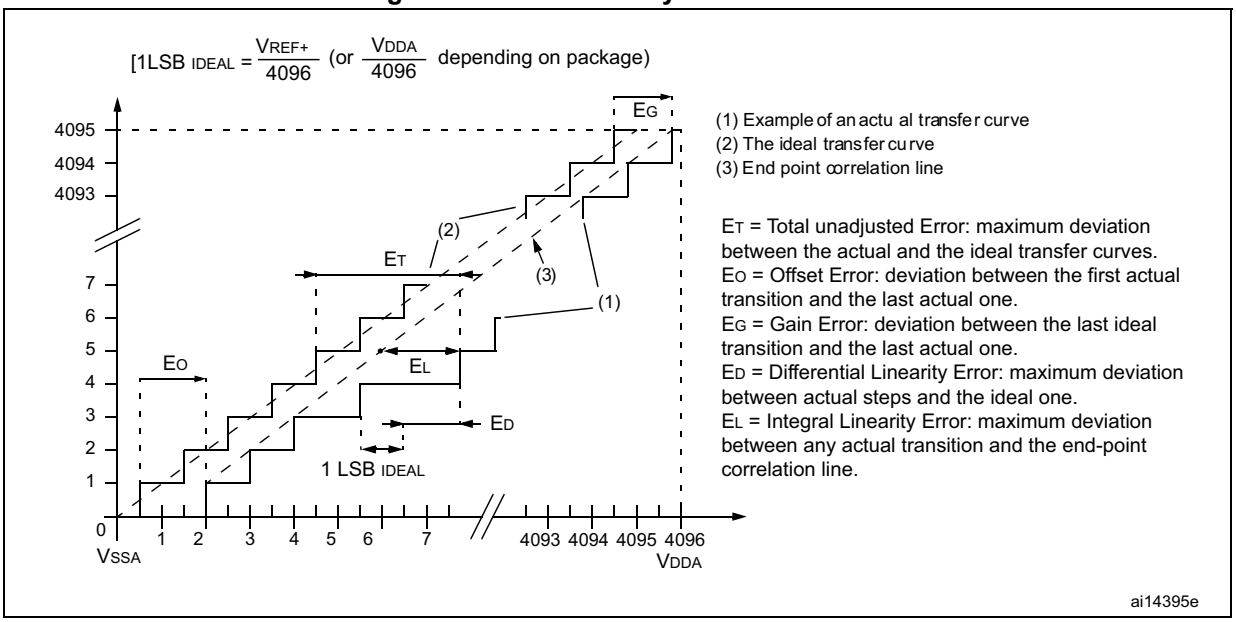
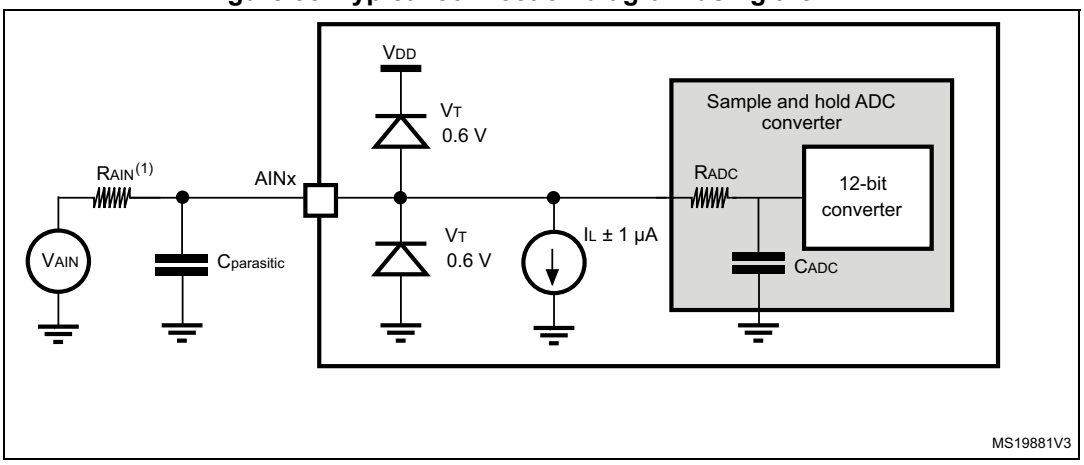


Figure 35. Typical connection diagram using the ADC



1. Refer to *Table 68* for the values of R_{AIN}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 11*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

6.3.20 Comparator characteristics

Table 76. Comparator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		2	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	
V_{BG}	Scaler input voltage	-		-	1.2	-	
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
t_{S_SC}	V_{REFINT} scaler startup time from power down	First V_{REFINT} scaler activation after device power on		-	-	1(2)	s
		Next activations		-	-	0.2	ms
t_{START}	Comparator startup time	Startup time to reach propagation delay specification		-	-	60	µs
t_D	Propagation delay for 200 mV step with 100 mV overdrive	Ultra-low-power mode		-	2	4.5	µs
		Low-power mode		-	0.7	1.5	
		Medium power mode		-	0.3	0.6	
		High speed mode	$V_{DDA} \geq 2.7$ V	-	50	100	ns
			$V_{DDA} < 2.7$ V	-	100	240	
	Propagation delay for full range step with 100 mV overdrive	Ultra-low-power mode		-	2	7	µs
		Low-power mode		-	0.7	2.1	
		Medium power mode		-	0.3	1.2	
		High speed mode	$V_{DDA} \geq 2.7$ V	-	90	180	ns
			$V_{DDA} < 2.7$ V	-	110	300	
V_{offset}	Comparator offset error	-		-	±4	±10	mV
dV_{offset}/dT	Offset error temperature coefficient	-		-	18	-	µV/°C
$I_{DD(COMP)}$	COMP current consumption	Ultra-low-power mode		-	1.2	1.5	µA
		Low-power mode		-	3	5	
		Medium power mode		-	10	15	
		High speed mode		-	75	100	

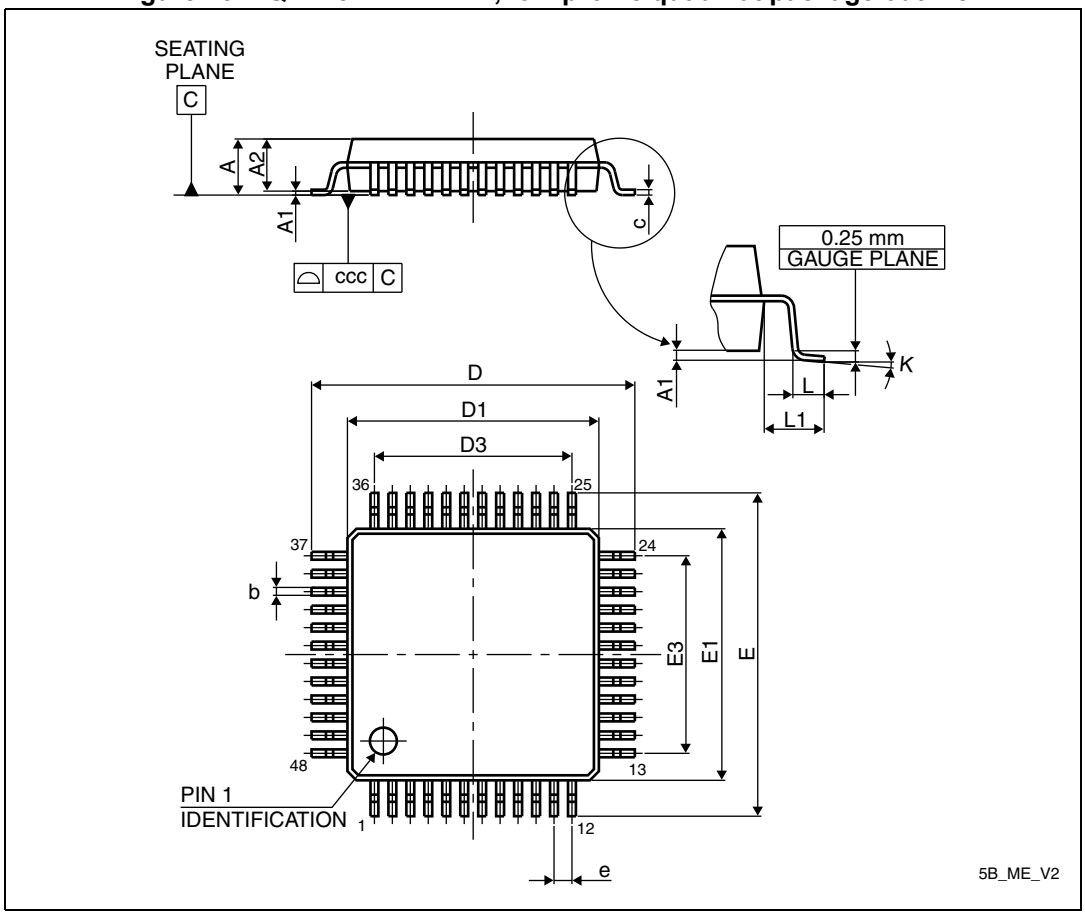
Table 77. Operational amplifier characteristics(1) (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
PGA gain	Non inverting gain value	-	-	2	-	-
			-	4	-	-
			-	8	-	-
			-	16	-	-
$R_{network}$	R2/R1 internal resistance values in PGA mode (3)	Gain=2	-	5.4/5.4	-	kΩ
		Gain=4	-	16.2/5.4	-	
		Gain=8	-	37.8/5.4	-	
		Gain=16	-	40.5/2.7	-	
PGA gain error	PGA gain error	-	-1%	-	1%	
I_{bias}	OPAMP input bias current	-	-	-	±0.2(4)	µA
PGA BW	PGA bandwidth for different non inverting gain	PGA Gain = 2, Cload = 50pF, Rload = 4 KΩ	-	4	-	MHz
		PGA Gain = 4, Cload = 50pF, Rload = 4 KΩ	-	2	-	
		PGA Gain = 8, Cload = 50pF, Rload = 4 KΩ	-	1	-	
		PGA Gain = 16, Cload = 50pF, Rload = 4 KΩ	-	0.5	-	
en	Voltage noise density	@ 1KHz, Output loaded with 4 KΩ	-	109	-	$\frac{nV}{\sqrt{Hz}}$
		@ 10KHz, Output loaded with 4 KΩ	-	43	-	

1. Guaranteed by design.
2. The saturation voltage can be also limited by the Iload (drive current).
3. R2 is the internal resistance between OPAMP output and OPAMP inverting input.
   R1 is the internal resistance between OPAMP inverting input and ground.
   The PGA gain =1+R2/R1
4. Mostly TTa I/O leakage, when used in analog mode.

7.3 LQFP48 – 7 x 7 mm, low-profile quad flat package information

Figure 45. LQFP48 – 7 x 7 mm, low-profile quad flat package outline



1. Drawing is not to scale.

Table 83. LQFP48 – 7 x 7 mm, low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09	-	0.20	0.0035	-	0.0079
D	8.80	9.00	9.20	0.3465	0.3543	0.3622
D1	6.80	7.00	7.20	0.2677	0.2756	0.2835
D3	-	5.50	-	-	0.2165	-
E	8.80	9.00	9.20	0.3465	0.3543	0.3622