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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	52
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f302rbt6

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F302xB/STM32F302xC microcontrollers.

This STM32F302xB/STM32F302xC datasheet should be read in conjunction with the STM32F302xx reference manual (RM0365). The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M4 core with FPU, please refer to:

- **Cortex®-M4 with FPU Technical Reference Manual**, available from ARM website www.arm.com.
- **STM32F3xxx and STM32F4xxx Cortex®-M4 programming manual (PM0214)** available from our website *www.st.com*.

Table 2. STM32F302xx family device features and peripheral counts

Peripheral		STM32F302Cx		STM32F302Rx		STM32F302Vx	
Flash (Kbytes)		128	256	128	256	128	256
SRAM (Kbytes) on data bus		32	40	32	40	32	40
Timers	Advanced control	1 (16-bit)					
	General purpose	5 (16-bit) 1 (32-bit)					
	Basic	1 (16-bit)					
PWM channels (all) (1)		26					
PWM channels (except complementary)		20					
Communication interfaces	SPI (I2S)(2)	3 (2)					
	I^2C	2					
	USART	3					
	UART	0		2			
	CAN	1					
	USB	1					
GPIOs	Normal I/Os (TC, TTa)	20		27		45 in LQFP100 37 in WLCSP100	
	5-volt tolerant I/Os (FT, FTf)	17		25		42 in LQFP100 40 in WLCSP100	
DMA channels		12					
Capacitive sensing channels		17		18		24	
12-bit ADCs		2					
Number of channels		9		16		17	
12-bit DAC channels		1					
Analog comparator		4					
Operational amplifiers		2					
CPU frequency		72 MHz					
Operating voltage		2.0 to 3.6 V					
Operating temperature		Ambient operating temperature: - 40 to 85 °C / - 40 to 105 °C Junction temperature: - 40 to 125 °C					
Packages		LQFP48		LQFP64		LQFP100 WLCSP100	

1. This total number considers also the PWMs generated on the complementary output channels
2. The SPI interfaces can work in an exclusive way in either the SPI mode or the I^2S audio mode.

3.17.1 Advanced timer (TIM1)

The advanced-control timer, TIM1, can be seen as a three-phase PWM multiplexed on six channels. It has a complementary PWM output with programmable inserted dead-times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIM timers (described in *Section 3.17.2* using the same architecture, so the advanced-control timers can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

3.17.2 General-purpose timers (TIM2, TIM3, TIM4, TIM15, TIM16, TIM17)

There are up to six synchronizable general-purpose timers embedded in the STM32F302xB/STM32F302xC (see *Table 5* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, 3, and TIM4

  These are full-featured general-purpose timers:

  – TIM2 has a 32-bit auto-reload up/downcounter and 32-bit prescaler

  – TIM3 and 4 have 16-bit auto-reload up/downcounters and 16-bit prescalers.

  These timers all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

  The counters can be frozen in debug mode.

  All have independent DMA request generation and support quadrature encoders.

- TIM15, 16 and 17

  These three timers general-purpose timers with mid-range features:

  They have 16-bit auto-reload upcounters and 16-bit prescalers.

  – TIM15 has 2 channels and 1 complementary channel

  – TIM16 and TIM17 have 1 channel and 1 complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output.

  The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

  The counters can be frozen in debug mode.

3.17.3 Basic timer (TIM6)

This timer is mainly used for DAC trigger generation. It can also be used as a generic 16-bit time base.

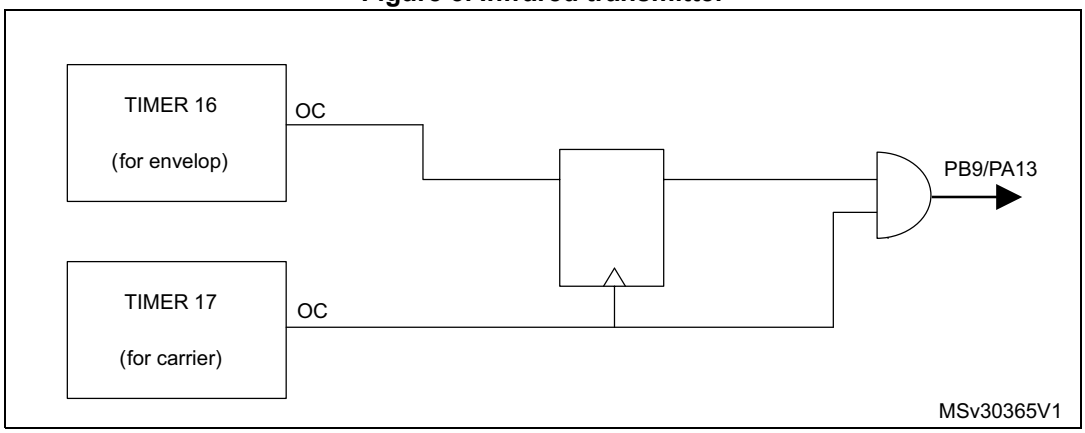
3.25 Infrared Transmitter

The STM32F302xB/STM32F302xC devices provide an infrared transmitter solution. The solution is based on internal connections between TIM16 and TIM17 as shown in the figure below.

TIM17 is used to provide the carrier frequency and TIM16 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate the infrared remote control signals, TIM16 channel 1 and TIM17 channel 1 must be properly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming the two timers output compare channels.

Figure 3. Infrared transmitter



3.26 Touch sensing controller (TSC)

The STM32F302xB/STM32F302xC devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 24 capacitive sensing channels distributed over 8 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

3.27 Development support

3.27.1 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.27.2 Embedded trace macrocell™

The ARM embedded trace macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F302xB/STM32F302xC through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using a high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

Figure 5. STM32F302xB/STM32F302xC LQFP64 pinout

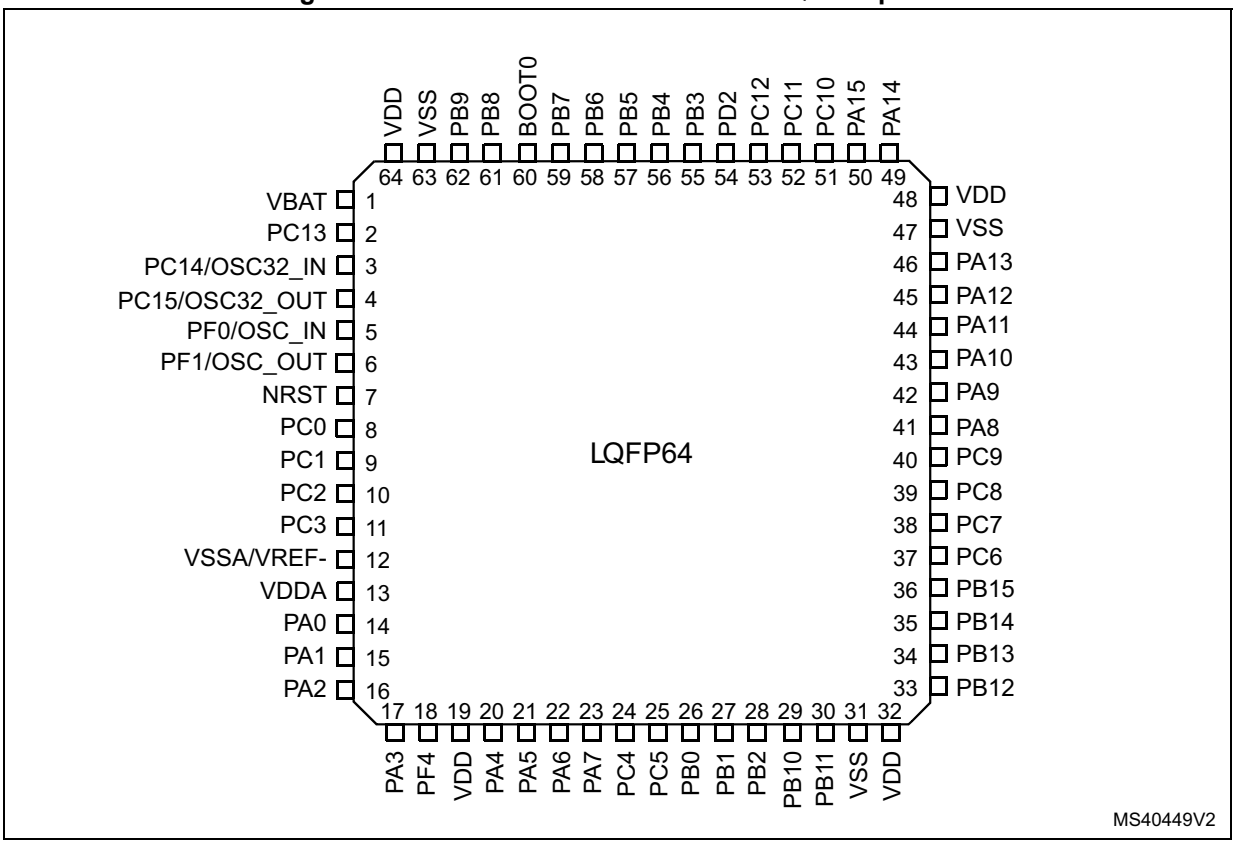


Table 13. STM32F302xB/STM32F302xC pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
WLCSP100	LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
C9	7	2	2	PC13(2)	I/O	TC	-	TIM1_CH1N	WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT
C10	8	3	3	PC14(2) OSC32_IN (PC14)	I/O	TC	-	-	OSC32_IN
D9	9	4	4	PC15(2) OSC32_ OUT (PC15)	I/O	TC	-	-	OSC32_OUT
D10	10	-	-	PF9	I/O	FT	(1)	TIM15_CH1, SPI2_SCK, EVENTOUT	-
E10	11	-	-	PF10	I/O	FT	(1)	TIM15_CH2, SPI2_SCK, EVENTOUT	-
F10	12	5	5	PF0- OSC_IN (PF0)	I/O	FTf	-	TIM1_CH3N, I2C2_SDA,	OSC_IN
F9	13	6	6	PF1- OSC_OUT (PF1)	I/O	FTf	-	I2C2_SCL	OSC_OUT
E9	14	7	7	NRST	I/O	RST		Device reset input / internal reset output (active low)	
G10	15	8	-	PC0	I/O	TTa	(1)	EVENTOUT	ADC12_IN6
G9	16	9	-	PC1	I/O	TTa	(1)	EVENTOUT	ADC12_IN7
G8	17	10	-	PC2	I/O	TTa	(1)	EVENTOUT	ADC12_IN8
H10	18	11	-	PC3	I/O	TTa	(1)	TIM1_BKIN2, EVENTOUT	ADC12_IN9
E8	19	-	-	PF2	I/O	TTa	(1)	EVENTOUT	ADC12_IN10
H8	20	12	8	VSSA/ VREF-	S	-	-	Analog ground/Negative reference voltage	
J8	21	-	-	VREF+(3)	S	-	-	Positive reference voltage	
J10	22	-	-	VDDA	S	-	-	Analog power supply	
-	-	13	9	VDDA/ VREF+	S	-	-	Analog power supply/Positive reference voltage	
H9	23	14	10	PA0	I/O	TTa	(4)	USART2_CTS, TIM2_CH1_ETR, TSC_G1_IO1, COMP1_OUT, EVENTOUT	ADC1_IN1, COMP1_INM, RTC_ TAMP2, WKUP1

Table 27. Programmable voltage detector characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{PVD0}	PVD threshold 0	Rising edge	2.1	2.18	2.26	V
		Falling edge	2	2.08	2.16	
V_{PVD1}	PVD threshold 1	Rising edge	2.19	2.28	2.37	
		Falling edge	2.09	2.18	2.27	
V_{PVD2}	PVD threshold 2	Rising edge	2.28	2.38	2.48	
		Falling edge	2.18	2.28	2.38	
V_{PVD3}	PVD threshold 3	Rising edge	2.38	2.48	2.58	
		Falling edge	2.28	2.38	2.48	
V_{PVD4}	PVD threshold 4	Rising edge	2.47	2.58	2.69	
		Falling edge	2.37	2.48	2.59	
V_{PVD5}	PVD threshold 5	Rising edge	2.57	2.68	2.79	
		Falling edge	2.47	2.58	2.69	
V_{PVD6}	PVD threshold 6	Rising edge	2.66	2.78	2.9	
		Falling edge	2.56	2.68	2.8	
V_{PVD7}	PVD threshold 7	Rising edge	2.76	2.88	3	
		Falling edge	2.66	2.78	2.9	
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
IDD(PVD)	PVD current consumption	-	-	0.15	0.26	µA

1. Guaranteed by characterization results.
2. Guaranteed by design.

Table 37. Switching output I/O current consumption

Symbol	Parameter	Conditions[1]	I/O toggling frequency (f_{SW})	Typ	Unit
I_{SW}	I/O current consumption	V_{DD} = 3.3 V C_{ext} = 0 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.90	mA
			4 MHz	0.93	
			8 MHz	1.16	
			18 MHz	1.60	
			36 MHz	2.51	
			48 MHz	2.97	
		V_{DD} = 3.3 V C_{ext} = 10 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.93	
			4 MHz	1.06	
			8 MHz	1.47	
			18 MHz	2.26	
			36 MHz	3.39	
			48 MHz	5.99	
		V_{DD} = 3.3 V C_{ext} = 22 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.03	
			4 MHz	1.30	
			8 MHz	1.79	
			18 MHz	3.01	
			36 MHz	5.99	
		V_{DD} = 3.3 V C_{ext} = 33 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.10	
			4 MHz	1.31	
			8 MHz	2.06	
			18 MHz	3.47	
			36 MHz	8.35	
		V_{DD} = 3.3 V C_{ext} = 47 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.20	
			4 MHz	1.54	
			8 MHz	2.46	
			18 MHz	4.51	
			36 MHz	9.98	

1. CS = 5 pF (estimated value).

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- all I/O pins are in analog input configuration
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature at 25°C and $V_{DD} = V_{DDA} = 3.3$ V.

Table 38. Peripheral current consumption

Peripheral	Typical consumption(1)	Unit
	I_{DD}	
BusMatrix (2)	12.6	µA/MHz
DMA1	7.6	
DMA2	6.1	
CRC	2.1	
GPIOA	10.0	
GPIOB	10.3	
GPIOC	2.2	
GPIOD	8.8	
GPIOE	3.3	
GPIOF	3.0	
TSC	5.5	
ADC1&2	17.3	
APB2-Bridge (3)	3.6	
SYSCFG	7.3	
TIM1	40.0	
SPI1	8.8	
USART1	23.3	
TIM15	17.1	
TIM16	10.1	
TIM17	11.0	
APB1-Bridge (3)	6.1	
TIM2	49.1	
TIM3	38.8	
TIM4	38.3	

6.3.6 Wakeup time from low-power mode

The wakeup times given in *Table 39* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep mode: the wakeup event is WFE.
- WKUP1 (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 24*.

Table 39. Low-power mode wakeup timings

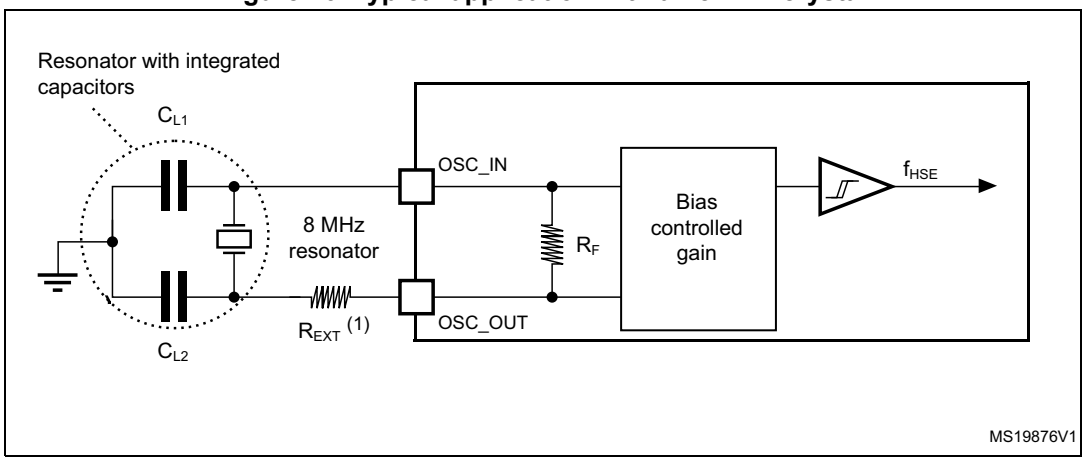
Symbol	Parameter	Conditions	Typ @V_{DD}, V_{DD} = V_{DDA}						Max	Unit
			2.0 V	2.4 V	2.7 V	3 V	3.3 V	3.6 V		
t_{WUSTOP}	Wakeup from Stop mode	Regulator in run mode	4.1	3.9	3.8	3.7	3.6	3.5	4.5	µs
		Regulator in low-power mode	7.9	6.7	6.1	5.7	5.4	5.2	9	
$t_{WUSTANDBY}$(1)	Wakeup from Standby mode	LSI and IWDG OFF	69.2	60.3	56.4	53.7	51.7	50	100	
$t_{WUSLEEP}$	Wakeup from Sleep mode	-	6						-	CPU clock cycles

1. Guaranteed by characterization results.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 16*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

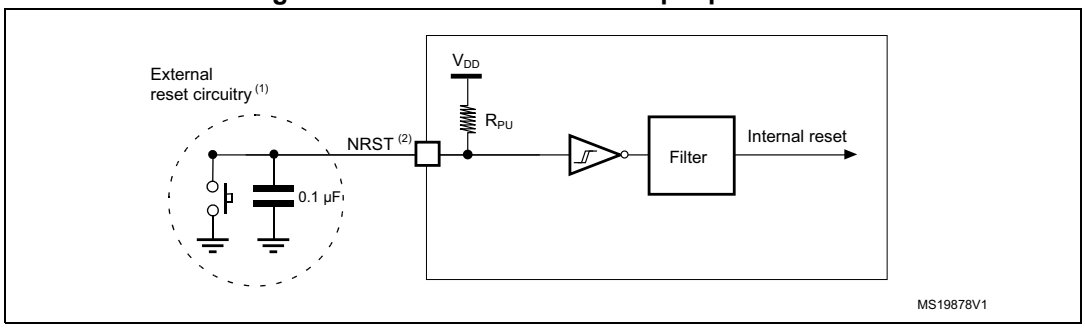
Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 16. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Figure 24. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 57*. Otherwise the reset will not be taken into account by the device.

6.3.16 Timer characteristics

The parameters given in *Table 58* are guaranteed by design.

Refer to *Section 6.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 58. TIMx(1)(2) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	13.9	-	ns
		$f_{TIM1CLK}$ = 144 MHz	6.95	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 72 MHz	0	36	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2)	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	0.0139	910	µs
		$f_{TIM1CLK}$ = 144 MHz	0.0069	455	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	-	59.65	s
		$f_{TIM1CLK}$ = 144 MHz	-	29.825	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3, TIM4, TIM15, TIM16 and TIM17 timers.
2. Guaranteed by design.

SPI/I^2S characteristics

Unless otherwise specified, the parameters given in *Table 63* for SPI or in *Table 64* for I^2S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 24*.

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I^2S).

Table 63. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode, SPI1 $2.7<V_{DD}<3.6$	-	-	24	MHz
		Slave mode, SPI1 $2.7<V_{DD}<3.6$			24	
		Master mode, SPI1/2/3 $2<V_{DD}<3.6$			18	
		Slave mode, SPI1/2/3 $2<V_{DD}<3.6$			18	
DuCy(SCK)	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	5.5	-	-	
$t_{su(SI)}$		Slave mode	6.5	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	5	-	-	
$t_{h(SI)}$		Slave mode	5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	0	-	4*Tpclk	
$t_{dis(SO)}$	Data output disable time	Slave mode	0	-	24	
$t_{v(SO)}$	Data output valid time	Slave mode	-	12	27	
		Slave mode, SPI1 $2.7<V_{DD}<3.6V$	-	12	18	
$t_{v(MO)}$		Master mode	-	1.5	3	
$t_{h(SO)}$	Data output hold time	Slave mode	11	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. Guaranteed by characterization results.

Table 72. ADC accuracy - limited test conditions, 64-pin packages(1)(2) (continued)

Symbol	Parameter	Conditions			Min (3)	Typ	Max (3)	Unit
SNR(4)	Signal-to-noise ratio	ADC clock freq. ≤ 72 MHz Sampling freq ≤ 5 Msps V_{DDA} = 3.3 V 25°C 64-pin package	Single ended	Fast channel 5.1 Ms	66	67	-	dB
				Slow channel 4.8 Ms	66	67	-	
			Differential	Fast channel 5.1 Ms	69	70	-	
				Slow channel 4.8 Ms	69	70	-	
THD(4)	Total harmonic distortion		Single ended	Fast channel 5.1 Ms	-	-80	-80	
				Slow channel 4.8 Ms	-	-78	-77	
			Differential	Fast channel 5.1 Ms	-	-83	-82	
				Slow channel 4.8 Ms	-	-81	-80	

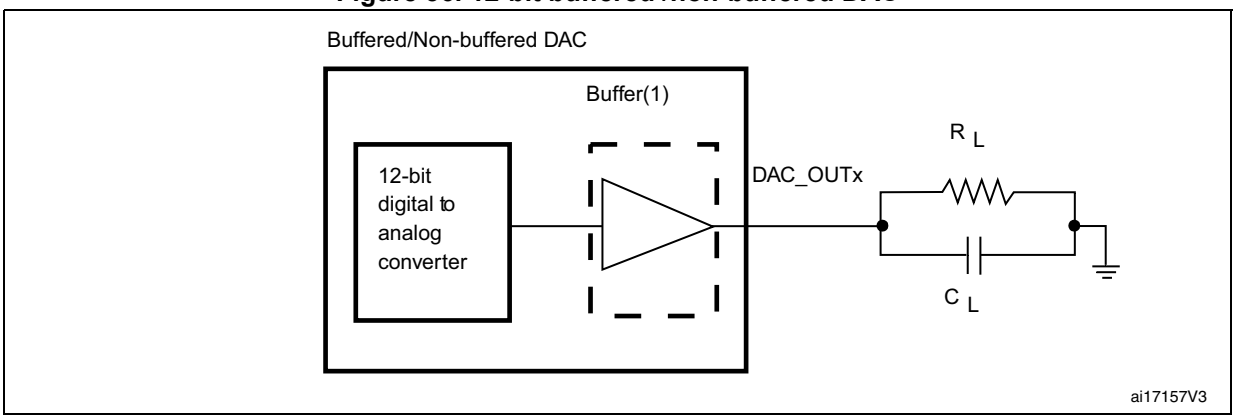
1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.14* does not affect the ADC accuracy.
3. Guaranteed by characterization results.
4. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

Table 75. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{WAKEUP}(3)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ	-	6.5	10	µs
PSRR+ (1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement	$C_{LOAD} = 50$ pF, No $R_{LOAD} \geq 5$ kΩ,	-	–67	–40	dB

1. Guaranteed by design.
2. Quiescent mode refers to the state of the DAC a keeping steady value on the output, so no dynamic consumption is involved.
3. Guaranteed by characterization results.

Figure 36. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Table 77. Operational amplifier characteristics(1) (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
PGA gain	Non inverting gain value	-	-	2	-	-
			-	4	-	-
			-	8	-	-
			-	16	-	-
$R_{network}$	R2/R1 internal resistance values in PGA mode (3)	Gain=2	-	5.4/5.4	-	kΩ
		Gain=4	-	16.2/5.4	-	
		Gain=8	-	37.8/5.4	-	
		Gain=16	-	40.5/2.7	-	
PGA gain error	PGA gain error	-	-1%	-	1%	
I_{bias}	OPAMP input bias current	-	-	-	±0.2(4)	µA
PGA BW	PGA bandwidth for different non inverting gain	PGA Gain = 2, Cload = 50pF, Rload = 4 KΩ	-	4	-	MHz
		PGA Gain = 4, Cload = 50pF, Rload = 4 KΩ	-	2	-	
		PGA Gain = 8, Cload = 50pF, Rload = 4 KΩ	-	1	-	
		PGA Gain = 16, Cload = 50pF, Rload = 4 KΩ	-	0.5	-	
en	Voltage noise density	@ 1KHz, Output loaded with 4 KΩ	-	109	-	$\frac{nV}{\sqrt{Hz}}$
		@ 10KHz, Output loaded with 4 KΩ	-	43	-	

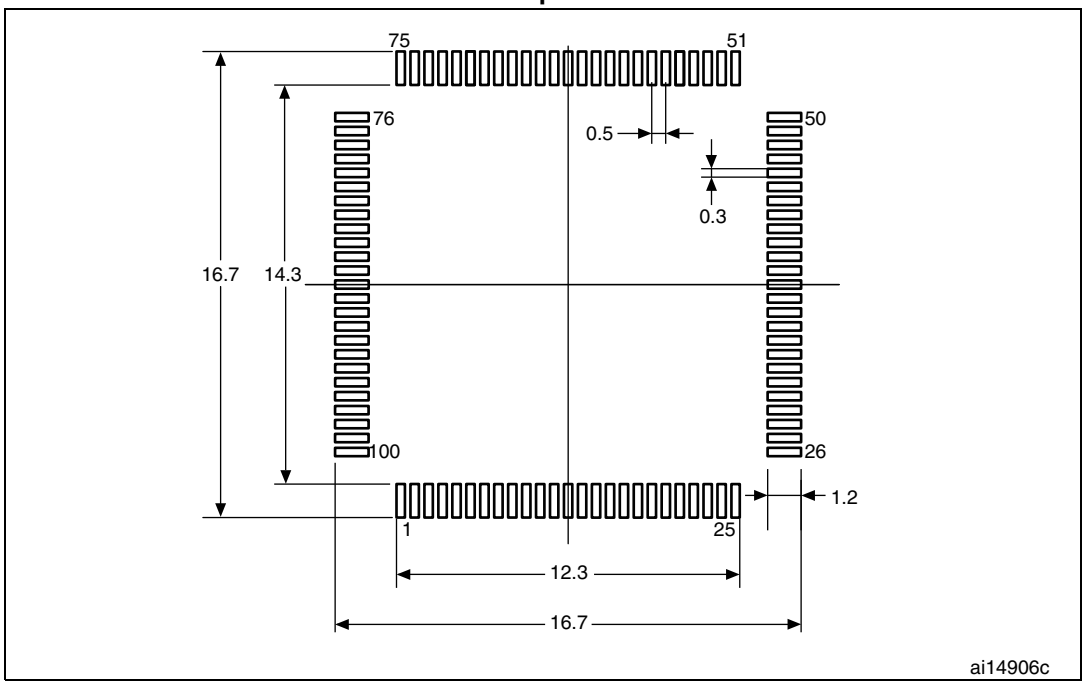
1. Guaranteed by design.
2. The saturation voltage can be also limited by the Iload (drive current).
3. R2 is the internal resistance between OPAMP output and OPAMP inverting input.
   R1 is the internal resistance between OPAMP inverting input and ground.
   The PGA gain =1+R2/R1
4. Mostly TTa I/O leakage, when used in analog mode.

Table 81. LQPF100 – 14 x 14 mm, low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09	-	0.2	0.0035	-	0.0079
D	15.80	16.00	16.2	0.622	0.6299	0.6378
D1	13.80	14.00	14.2	0.5433	0.5512	0.5591
D3	-	12.00	-	-	0.4724	-
E	15.80	16.00	16.2	0.622	0.6299	0.6378
E1	13.80	14.00	14.2	0.5433	0.5512	0.5591
E3	-	12.00	-	-	0.4724	-
e	-	0.50	-	-	0.0197	-
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	-	1.00	-	-	0.0394	-
K	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 40. LQFP100 – 14 x 14 mm, low-profile quad flat package recommended footprint



1. Dimensions are in millimeters.