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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	52
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f302rbt6tr

Table 4. STM32F302xB/STM32F302xC peripheral interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action
GPIO RTCCLK HSE/32 MC0	TIM16	Clock source used as input channel for HSI and LSI calibration
CSS CPU (hard fault) COMPx PVD GPIO	TIM1, TIM15, 16, 17	Timer break
GPIO	TIMx	External trigger, timer break
	ADCx DAC1	Conversion external trigger
DAC1	COMPx	Comparator inverting input

Note: For more details about the interconnect actions, please refer to the corresponding sections in the reference manual (RM0365.

3.9 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

3.10 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allows I/O toggling up to 36 MHz.

3.11 Direct memory access (DMA)

The flexible general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each of the 12 DMA channels is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose timers, DAC and ADC.

3.12 Interrupts and events

3.12.1 Nested vectored interrupt controller (NVIC)

The STM32F302xB/STM32F302xC devices embed a nested vectored interrupt controller (NVIC) able to handle up to 66 maskable interrupt channels and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.22 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I2S)

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Two standard I2S interfaces (multiplexed with SPI2 and SPI3) supporting four different audio standards can operate as master or slave at half-duplex and full duplex communication modes. They can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by 8-bit programmable linear prescaler. When operating in master mode it can output a clock for an external audio component at 256 times the sampling frequency.

Refer to *Table 9* for the features available in SPI1, SPI2 and SPI3.

Table 9. STM32F302xB/STM32F302xC SPI/I2S implementation

SPI features(1)	SPI1	SPI2	SPI3
Hardware CRC calculation	X	X	X
Rx/Tx FIFO	X	X	X
NSS pulse mode	X	X	X
I2S mode	-	X	X
TI mode	X	X	X

1. X = supported.

3.23 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

3.24 Universal serial bus (USB)

The STM32F302xB/STM32F302xC devices embed an USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator). The USB has a dedicated 512-bytes SRAM memory for data transmission and reception.

The parameters given in Table 30 to Table 34 are derived from tests performed under ambient temperature and supply voltage conditions summarized in Table 24.

Table 30. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6V

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A (1)			Typ	Max @ T_A (1)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, executing from Flash	External clock (HSE bypass)	72 MHz	61.2	65.8	67.6	68.5	27.8	30.3	30.7	31.5	mA
			64 MHz	54.7	59.1	60.2	61.1	24.6	27.2	27.6	28.3	
			48 MHz	41.7	45.1	46.2	47.2	19.2	21.1	21.4	21.8	
			32 MHz	28.1	31.5	32.5	32.7	12.9	14.6	14.8	15.3	
			24 MHz	21.4	23.7	24.4	25.2	10.0	11.4	11.4	12.1	
			8 MHz	7.4	8.4	8.6	9.4	3.6	4.1	4.4	5.0	
			1 MHz	1.3	1.6	1.8	2.6	0.8	1.0	1.2	2.1	
		Internal clock (HSI)	64 MHz	49.7	54.4	55.4	56.3	24.5	27.2	27.4	28.1	
			48 MHz	37.9	42.2	43.0	43.5	18.9	21.4	21.5	21.6	
			32 MHz	25.8	29.2	29.2	30.0	12.7	14.2	14.6	15.2	
			24 MHz	19.7	22.3	22.6	23.2	6.7	7.7	7.9	8.5	
			8 MHz	6.9	7.8	8.3	8.8	3.5	4.0	4.4	5.0	
	Supply current in Run mode, executing from RAM	External clock (HSE bypass)	72 MHz	60.8	66.2(2)	69.7	70.4(2)	27.4	31.7(2)	32.2	32.5(2)	
			64 MHz	54.3	59.1	62.2	63.3	24.3	28.3	28.7	28.8	
			48 MHz	41.0	45.6	47.3	47.9	18.3	21.6	21.9	22.1	
			32 MHz	27.6	32.4	32.4	32.9	12.3	15.0	15.2	15.4	
			24 MHz	20.8	23.9	24.3	25.0	9.3	11.3	11.4	12.0	
			8 MHz	6.9	7.8	8.7	9.0	3.1	3.7	4.2	4.9	
			1 MHz	0.9	1.2	1.5	2.3	0.4	0.6	1.0	1.8	
		Internal clock (HSI)	64 MHz	49.2	53.9	55.2	57.4	23.9	27.8	28.2	28.4	
			48 MHz	37.3	40.8	41.4	44.1	18.2	21.0	21.6	21.9	
			32 MHz	25.1	27.6	29.1	30.1	12.0	14.0	14.5	15.1	
			24 MHz	19.0	21.6	22.1	22.9	6.3	7.2	7.7	8.1	
			8 MHz	6.4	7.3	7.9	8.4	3.0	3.5	4.0	4.7	

Table 30. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6V (continued)

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(1)			Typ	Max @ T_A(1)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Sleep mode, executing from Flash or RAM	External clock (HSE bypass)	72 MHz	44.0	48.4	49.4	50.5	6.6	7.5	7.9	8.7	mA
			64 MHz	39.2	43.3	44.0	45.2	6.0	6.8	7.2	7.9	
			48 MHz	29.6	32.7	33.3	34.3	4.5	5.2	5.6	6.3	
			32 MHz	19.7	23.3	23.3	23.5	3.1	3.5	4.0	4.8	
			24 MHz	14.9	17.6	17.8	18.3	2.4	2.8	3.3	3.9	
			8 MHz	4.9	5.7	6.1	6.9	0.8	1.0	1.4	2.2	
			1 MHz	0.6	0.9	1.2	2.1	0.1	0.3	0.6	1.5	
		Internal clock (HSI)	64 MHz	34.2	38.1	39.2	40.3	5.7	6.3	6.8	7.5	
			48 MHz	25.8	28.7	29.6	30.3	4.3	4.8	5.2	5.9	
			32 MHz	17.4	19.4	19.9	20.7	2.9	3.2	3.7	4.5	
			24 MHz	13.2	15.1	15.6	15.9	1.5	1.8	2.2	2.9	
			8 MHz	4.5	5.0	5.6	6.2	0.7	0.9	1.2	2.1	

1. Guaranteed by characterization results unless otherwise specified.
2. Data based on characterization results and tested in production with code executing from RAM.

Table 31. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Parameter	Conditions (1)	f_{HCLK}	V_{DDA} = 2.4 V				V_{DDA} = 3.6 V				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run/Sleep mode, code executing from Flash or RAM	HSE bypass	72 MHz	225	276	289	297	245	302	319	329	µA
			64 MHz	198	249	261	268	216	270	284	293	
			48 MHz	149	195	204	211	159	209	222	230	
			32 MHz	102	145	152	157	110	154	162	169	
			24 MHz	80	119	124	128	86	126	131	135	
			8 MHz	2	3	4	6	3	4	5	9	
			1 MHz	2	3	5	7	3	4	6	9	
		HSI clock	64 MHz	270	323	337	344	299	354	371	381	
			48 MHz	220	269	280	286	244	293	309	318	
			32 MHz	173	218	228	233	193	239	251	257	
			24 MHz	151	194	200	204	169	211	219	225	
			8 MHz	73	97	99	103	88	105	110	116	

1. Current consumption from the V_{DDA} supply is independent of whether the peripherals are on or off. Furthermore when the PLL is off, I_{DDA} is independent from the frequency.
2. Guaranteed by characterization results.

Table 32. Typical and maximum V_{DD} consumption in Stop and Standby modes

Symbol	Parameter	Conditions	Typ @V_{DD} (V_{DD}=V_{DDA})						Max(1)			Unit
			2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, all oscillators OFF	20.05	20.33	20.42	20.50	20.67	20.80	44.2(2)	350	735(2)	µA
		Regulator in low-power mode, all oscillators OFF	7.63	7.77	7.90	8.07	8.17	8.33	30.6(2)	335	720(2)	
	Supply current in Standby mode	LSI ON and IWDG ON	0.80	0.96	1.09	1.23	1.37	1.51	-	-	-	
		LSI OFF and IWDG OFF	0.60	0.74	0.83	0.93	1.02	1.11	5.0(2)	7.8	13.3(2)	

1. Guaranteed by characterization results unless otherwise specified.
2. Data based on characterization results and tested in production.

Table 33. Typical and maximum V_{DDA} consumption in Stop and Standby modes

Symbol	Parameter	Conditions		Typ @V_{DD} (V_{DD} = V_{DDA})						Max(1)			Unit
				2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DDA}	Supply current in Stop mode	V_{DDA} monitoring ON	Regulator in run mode, all oscillators OFF	1.81	1.95	2.07	2.20	2.35	2.52	3.7	5.5	8.8	µA
			Regulator in low-power mode, all oscillators OFF	1.81	1.95	2.07	2.20	2.35	2.52	3.7	5.5	8.8	
	Supply current in Standby mode		LSI ON and IWDG ON	2.22	2.42	2.59	2.78	3.0	3.24	-	-	-	
			LSI OFF and IWDG OFF	1.69	1.82	1.94	2.08	2.23	2.40	3.5	5.4	9.2	
	Supply current in Stop mode	V_{DDA} monitoring OFF	Regulator in run mode, all oscillators OFF	1.05	1.08	1.10	1.15	1.22	1.29	-	-	-	
			Regulator in low-power mode, all oscillators OFF	1.05	1.08	1.10	1.15	1.22	1.29	-	-	-	
	Supply current in Standby mode		LSI ON and IWDG ON	1.44	1.52	1.60	1.71	1.84	1.98	-	-	-	
			LSI OFF and IWDG OFF	0.93	0.95	0.98	1.02	1.08	1.15	-	-	-	

1. Guaranteed by characterization results.

The total consumption is the sum of IDD and IDDA.

Table 36. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Sleep mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash or RAM	72 MHz	44.1	7.0	mA
			64 MHz	39.7	6.3	
			48 MHz	30.3	4.9	
			32 MHz	20.5	3.5	
			24 MHz	15.4	2.8	
			16 MHz	10.6	2.0	
			8 MHz	5.4	1.1	
			4 MHz	3.2	1.0	
			2 MHz	2.1	0.9	
			1 MHz	1.5	0.8	
			500 kHz	1.2	0.8	
			125 kHz	1.0	0.8	
I_{DDA} (1) (2)	Supply current in Sleep mode from V_{DDA} supply		72 MHz	239.7	238.5	µA
			64 MHz	210.5	209.6	
			48 MHz	155.0	155.6	
			32 MHz	105.3	105.2	
			24 MHz	81.9	81.8	
			16 MHz	58.7	58.6	
			8 MHz	2.4	2.4	
			4 MHz	2.4	2.4	
			2 MHz	2.4	2.4	
			1 MHz	2.4	2.4	
			500 kHz	2.4	2.4	
			125 kHz	2.4	2.4	

1. V_{DDA} monitoring is ON.
2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.

Table 37. Switching output I/O current consumption

Symbol	Parameter	Conditions(1)	I/O toggling frequency (f_{SW})	Typ	Unit
I_{SW}	I/O current consumption	V_{DD} = 3.3 V C_{ext} = 0 pF C = C_{INT} + C_{EXT}+ C_S	2 MHz	0.90	mA
			4 MHz	0.93	
			8 MHz	1.16	
			18 MHz	1.60	
			36 MHz	2.51	
			48 MHz	2.97	
		V_{DD} = 3.3 V C_{ext} = 10 pF C = C_{INT} + C_{EXT} +C_S	2 MHz	0.93	
			4 MHz	1.06	
			8 MHz	1.47	
			18 MHz	2.26	
			36 MHz	3.39	
			48 MHz	5.99	
		V_{DD} = 3.3 V C_{ext} = 22 pF C = C_{INT} + C_{EXT} +C_S	2 MHz	1.03	
			4 MHz	1.30	
			8 MHz	1.79	
			18 MHz	3.01	
			36 MHz	5.99	
		V_{DD} = 3.3 V C_{ext} = 33 pF C = C_{INT} + C_{EXT}+ C_S	2 MHz	1.10	
			4 MHz	1.31	
			8 MHz	2.06	
			18 MHz	3.47	
			36 MHz	8.35	
		V_{DD} = 3.3 V C_{ext} = 47 pF C = C_{INT} + C_{EXT}+ C_S	2 MHz	1.20	
			4 MHz	1.54	
			8 MHz	2.46	
			18 MHz	4.51	
			36 MHz	9.98	

1. CS = 5 pF (estimated value).

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- all I/O pins are in analog input configuration
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature at 25°C and $V_{DD} = V_{DDA} = 3.3$ V.

Table 38. Peripheral current consumption

Peripheral	Typical consumption(1) I_{DD}	Unit
BusMatrix (2)	12.6	µA/MHz
DMA1	7.6	
DMA2	6.1	
CRC	2.1	
GPIOA	10.0	
GPIOB	10.3	
GPIOC	2.2	
GPIOD	8.8	
GPIOE	3.3	
GPIOF	3.0	
TSC	5.5	
ADC1&2	17.3	
APB2-Bridge (3)	3.6	
SYSCFG	7.3	
TIM1	40.0	
SPI1	8.8	
USART1	23.3	
TIM15	17.1	
TIM16	10.1	
TIM17	11.0	
APB1-Bridge (3)	6.1	
TIM2	49.1	
TIM3	38.8	
TIM4	38.3	

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 23* and *Table 56*, respectively.

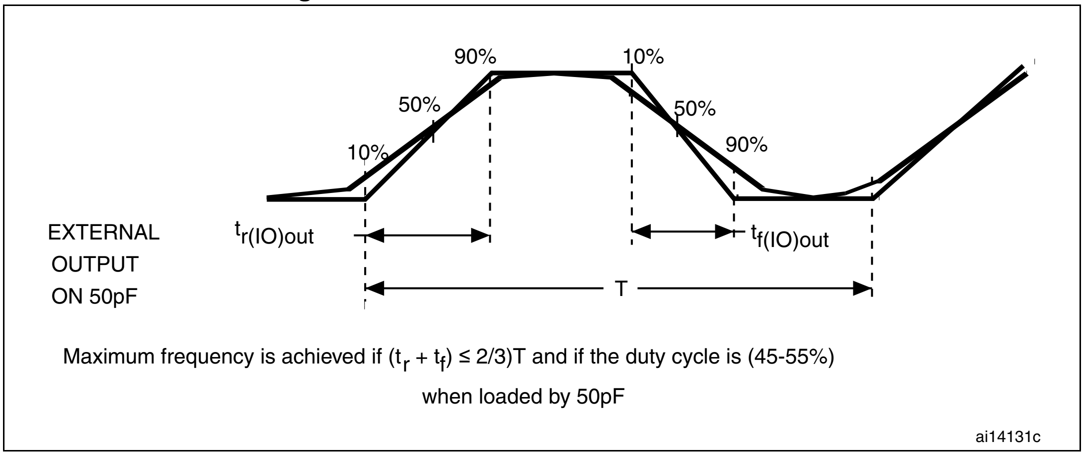
Unless otherwise specified, the parameters given are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 24*.

Table 56. I/O AC characteristics[1]

OSPEEDRy [1:0] value[1]	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency[2]	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	2[3]	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	125[3]	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125[3]	
01	$f_{max(IO)out}$	Maximum frequency[2]	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	10[3]	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	25[3]	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25[3]	
11	$f_{max(IO)out}$	Maximum frequency[2]	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	50[3]	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	30[3]	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	20[3]	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5[3]	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8[3]	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12[3]	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5[3]	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8[3]	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12[3]	
FM+ configuration[4]	$f_{max(IO)out}$	Maximum frequency[2]	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	2[4]	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	12[4]	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	34[4]	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10[3]	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the RM0365 reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 23*.
3. Guaranteed by design.
4. The I/O speed configuration is bypassed in FM+ I/O mode. Refer to the STM32F302xx STM32F312xx reference manual RM0365 for a description of FM+ I/O mode configuration.

Figure 23. I/O AC characteristics definition



6.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 54*).

Unless otherwise specified, the parameters given in *Table 57* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 24*.

Table 57. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	-	-	-	$0.3V_{DD}$+ 0.07(1)	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage	-	$0.445V_{DD}$+ 0.398(1)	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse	-	-	-	100(1)	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	-	500(1)	-	-	ns

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

USB characteristics

Table 65. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

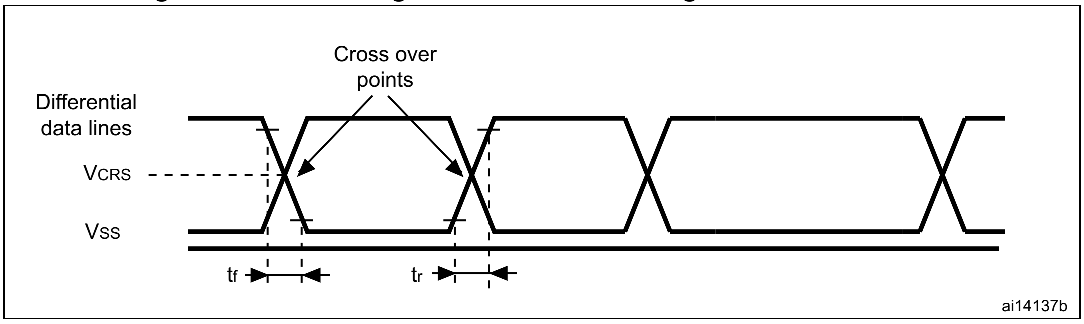
1. Guaranteed by design.

Table 66. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage(2)	-	3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
V_{CM}(4)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(4)	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(5)	-	0.3	V
V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(5)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. The STM32F302xB/STM32F302xC USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
4. Guaranteed by design.
5. R_L is the load connected on the USB drivers.

Figure 31. USB timings: definition of data signal rise and fall time



6.3.19 DAC electrical specifications

Table 75. DAC characteristics

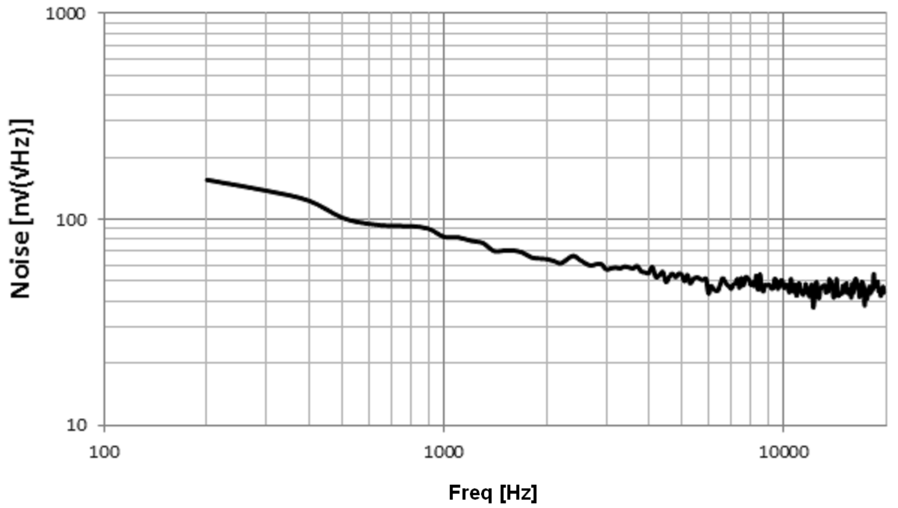
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	2.4	-	3.6	V
R_{LOAD} (1)	Resistive load	DAC output buffer ON: Connected to V_{SSA}	5	-	-	kΩ
		DAC output buffer ON: Connected to V_{DDA}	25	-	-	kΩ
R_O (1)	Output impedance	DAC output buffer OFF	-	-	15	kΩ
C_{LOAD} (1)	Capacitive load	DAC output buffer ON	-	-	50	pF
V_{DAC_OUT} (1)	Voltage on DAC_OUT output	Corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{DDA} = 3.6 V and (0x155) and (0xEAB) at V_{DDA} = 2.4 V DAC output buffer ON.	0.2	-	$V_{DDA} - 0.2$	V
		DAC output buffer OFF	-	0.5	V_{DDA} - 1LSB	mV
I_{DDA} (3)	DAC DC current consumption in quiescent mode (Standby mode)(2)	With no load, middle code (0x800) on the input.	-	-	380	µA
		With no load, worst code (0xF1C) on the input.	-	-	480	µA
DNL(3)	Differential non linearity Difference between two consecutive code-1LSB)	Given for a 10-bit input code	-	-	±0.5	LSB
		Given for a 12-bit input code	-	-	±2	LSB
INL(3)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095)	Given for a 10-bit input code	-	-	±1	LSB
		Given for a 12-bit input code	-	-	±4	LSB
Offset(3)	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{DDA}/2$)	-	-	-	±10	mV
		Given for a 10-bit input code at V_{DDA} = 3.6 V	-	-	±3	LSB
		Given for a 12-bit input code at V_{DDA} = 3.6 V	-	-	±12	LSB
Gain error(3)	Gain error	Given for a 12-bit input code	-	-	±0.5	%
$t_{SETTLING}$ (3)	Settling time (full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ	-	3	4	µs
Update rate(3)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ	-	-	1	MS/s

6.3.20 Comparator characteristics

Table 76. Comparator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	2	-	3.6	V
V_{IN}	Comparator input voltage range	-	0	-	V_{DDA}	V
V_{BG}	Scaler input voltage	-	-	1.2	-	V
V_{SC}	Scaler offset voltage	-	-	±5	±10	mV
t_{S_SC}	V_{REFINT} scaler startup time from power down	First V_{REFINT} scaler activation after device power on	-	-	1(2)	s
		Next activations	-	-	0.2	ms
t_{START}	Comparator startup time	Startup time to reach propagation delay specification	-	-	60	µs
t_D	Propagation delay for 200 mV step with 100 mV overdrive	Ultra-low-power mode	-	2	4.5	µs
		Low-power mode	-	0.7	1.5	µs
		Medium power mode	-	0.3	0.6	µs
		High speed mode, $V_{DDA} \geq 2.7$ V	-	50	100	ns
		High speed mode, $V_{DDA} < 2.7$ V	-	100	240	ns
	Propagation delay for full range step with 100 mV overdrive	Ultra-low-power mode	-	2	7	µs
		Low-power mode	-	0.7	2.1	µs
		Medium power mode	-	0.3	1.2	µs
		High speed mode, $V_{DDA} \geq 2.7$ V	-	90	180	ns
		High speed mode, $V_{DDA} < 2.7$ V	-	110	300	ns
V_{offset}	Comparator offset error	-	-	±4	±10	mV
dV_{offset}/dT	Offset error temperature coefficient	-	-	18	-	µV/°C
$I_{DD(COMP)}$	COMP current consumption	Ultra-low-power mode	-	1.2	1.5	µA
		Low-power mode	-	3	5	µA
		Medium power mode	-	10	15	µA
		High speed mode	-	75	100	µA

Figure 38. OPAMP voltage noise versus frequency



6.3.22 Temperature sensor characteristics

Table 78. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}(1)	Startup time	4	-	10	µs
T_{S_temp}(1)(2)	ADC sampling time when reading the temperature	2.2	-	-	µs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

Table 79. Temperature sensor calibration values

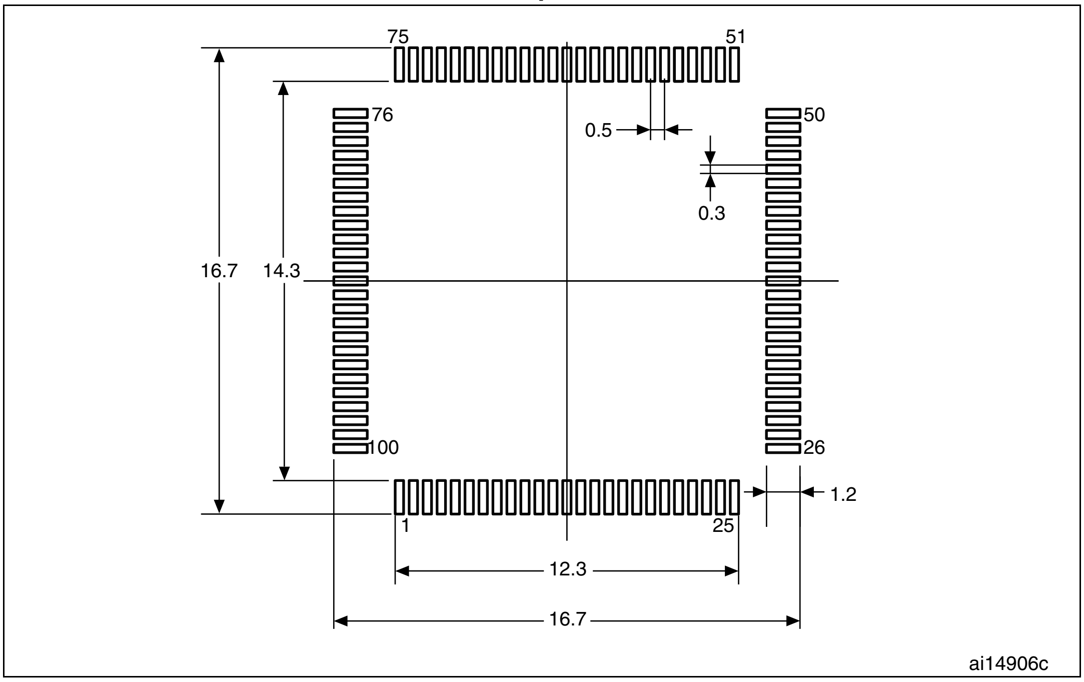
Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C V_{DDA}= 3.3 V	0x1FFF F7C2 - 0x1FFF F7C3

Table 81. LQPF100 – 14 x 14 mm, low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09	-	0.2	0.0035	-	0.0079
D	15.80	16.00	16.2	0.622	0.6299	0.6378
D1	13.80	14.00	14.2	0.5433	0.5512	0.5591
D3	-	12.00	-	-	0.4724	-
E	15.80	16.00	16.2	0.622	0.6299	0.6378
E1	13.80	14.00	14.2	0.5433	0.5512	0.5591
E3	-	12.00	-	-	0.4724	-
e	-	0.50	-	-	0.0197	-
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	-	1.00	-	-	0.0394	-
K	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 40. LQFP100 – 14 x 14 mm, low-profile quad flat package recommended footprint



1. Dimensions are in millimeters.

Table 84. WLCSP100 – 100L, 4.166 x 4.628 mm 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Typ	Min	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.17	-	-	0.0067	-
A2	-	0.38	-	-	0.0150	-
A3(2)	-	0.025	-	-	0.0010	-
Ø b(3)	0.22	0.25	0.28	-	0.0098	0.0110
D	4.166	4.201	4.236	-	0.1654	0.1668
E	4.628	4.663	4.698	-	0.1836	0.1850
e	-	0.4	-	-	0.0157	-
e1	-	3.6	-	-	0.1417	-
e2	-	3.6	-	-	0.1417	-
F	-	0.3005	-	-	0.0118	-
G	-	0.5315	-	-	0.0209	-
N	-	100	-	-	3.9370	-
aaa	-	0.1	-	-	0.0039	-
bbb	-	0.1	-	-	0.0039	-
ccc	-	0.1	-	-	0.0039	-
ddd	-	0.05	-	-	0.0020	-
eee	-	0.05	-	-	0.0020	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Table 88. Document revision history (continued)

Date	Revision	Changes
06-May-2016	7	Updated *Figure 5: STM32F302xB/STM32F302xC LQFP64 pinout* replacing VSS by PF4. Updated *Table 13: STM32F302xB/STM32F302xC pin definitions*: – Adding ‘digital power supply’ in the Pin function column at the line corresponding to K8/28/19 pins. – Adding VSS digital ground line with WLCSP100 K9 and K10 pins connected. – Replacing in VDD line for WLCSP100: ‘A10, B10’ by ‘A9, A10, B10, B8’. Updated *Figure 21: Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port*. Updated *Table 77: Operational amplifier characteristics* high saturation and low saturation voltages. Updated *Table 13: STM32F302xB/STM32F302xC pin definitions* adding note ‘Fast ADC channel’ for ADCx_IN1..5. Updated *Table 75: DAC characteristics* resistive load. Updated *Table 68: ADC characteristics* adding CMIR parameter and modifying tSTAB parameter characteristics.