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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	52
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f302rct6

2 Description

The STM32F302xB/STM32F302xC family is based on the high-performance ARM® Cortex®-M4 32-bit RISC core with FPU operating at a frequency of up to 72 MHz, and embedding a floating point unit (FPU), a memory protection unit (MPU) and an embedded trace macrocell (ETM). The family incorporates high-speed embedded memories (up to 256 Kbytes of Flash memory, up to 40 Kbytes of SRAM) and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The devices offer up to two fast 12-bit ADCs (5 Msps), four comparators, two operational amplifiers, up to one DAC channel, a low-power RTC, up to five general-purpose 16-bit timers, one general-purpose 32-bit timer, and one timer dedicated to motor control. They also feature standard and advanced communication interfaces: up to two I^2Cs, up to three SPIs (two SPIs are with multiplexed full-duplex I2Ss), three USARTs, up to two UARTs, CAN and USB. To achieve audio class accuracy, the I2S peripherals can be clocked via an external PLL.

The STM32F302xB/STM32F302xC family operates in the -40 to +85 °C and -40 to +105 °C temperature ranges from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F302xB/STM32F302xC family offers devices in four packages ranging from 48 pins to 100 pins.

The set of included peripherals changes with the device chosen.

3.4 Embedded SRAM

STM32F302xB/STM32F302xC devices feature up to 40 Kbytes of embedded SRAM with hardware parity check on first 16 Kbytes of SRAM. The memory can be accessed in read/write at CPU clock speed with 0 wait states.

3.5 Boot modes

At startup, Boot0 pin and Boot1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in the system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART2 (PD5/PD6) or USB (PA11/PA12) through DFU (device firmware upgrade).

3.6 Cyclic redundancy check (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

Table 4. STM32F302xB/STM32F302xC peripheral interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action
GPIO RTCCLK HSE/32 MC0	TIM16	Clock source used as input channel for HSI and LSI calibration
CSS CPU (hard fault) COMPx PVD GPIO	TIM1, TIM15, 16, 17	Timer break
GPIO	TIMx	External trigger, timer break
	ADCx DAC1	Conversion external trigger
DAC1	COMPx	Comparator inverting input

Note: For more details about the interconnect actions, please refer to the corresponding sections in the reference manual (RM0365.

3.9 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

Table 14. Alternate functions for port A (continued)

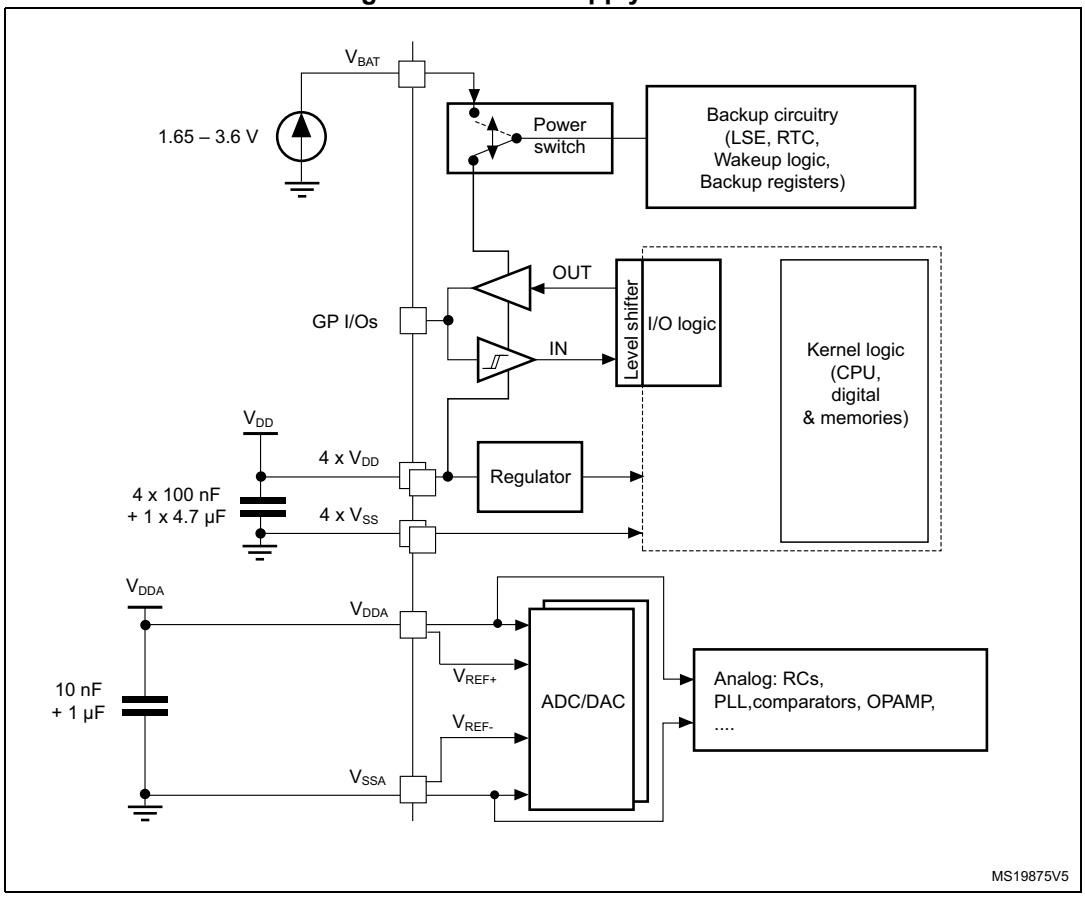
Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF14	AF15
PA12	-	TIM16_CH1	-	-	-	-	TIM1_CH2N	USART1_RTS_DE	COMP2_OUT	CAN_TX	TIM4_CH2	TIM1_ETR	-	USB_DP	EVENTOUT
PA13	SWDIO-JTMS	TIM16_CH1N	-	TSC_G4_IO3	-	IR_OUT	-	USART3_CTS	-	-	TIM4_CH3	-	-	-	EVENTOUT
PA14	SWCLK-JTCK	-	-	TSC_G4_IO4	I2C1_SDA		TIM1_BKIN	USART2_TX	-	-	-	-	-	-	EVENTOUT
PA15	JTDI	TIM2_CH1_ETR		-	I2C1_SCL	SPI1_NSS	SPI3_NSS, I2S3_WS	USART2_RX	-	TIM1_BKIN	-	-	-	-	EVENTOUT

Table 15. Alternate functions for port B

Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF15
PB0	-	-	TIM3_ CH3	TSC_ G3_IO2		-	TIM1_CH2N	-	-	-	-	-	EVENT OUT
PB1	-	-	TIM3_ CH4	TSC_ G3_IO3		-	TIM1_CH3N	-	COMP4_ OUT	-	-	-	EVENT OUT
PB2	-	-	-	TSC_ G3_IO4	-	-	-	-	-	-	-	-	EVENT OUT
PB3	JTDO-TRACESWO	TIM2_ CH2	TIM4_ ETR	TSC_ G5_IO1		SPI1_ SCK	SPI3_SCK, I2S3_CK	USART2_ TX	-	-	TIM3_ ETR	-	EVENT OUT
PB4	NJTRST	TIM16_ CH1	TIM3_ CH1	TSC_ G5_IO2		SPI1_ MISO	SPI3_MISO, I2S3ext_SD	USART2_ RX	-	-	TIM17_ BKIN	-	EVENT OUT
PB5	-	TIM16_ BKIN	TIM3_ CH2		I2C1_ SMBA	SPI1_ MOSI	SPI3_MOSI, I2S3_SD	USART2_ CK	-	-	TIM17_ CH1	-	EVENT OUT
PB6	-	TIM16_ CH1N	TIM4_ CH1	TSC_ G5_IO3	I2C1_SCL			USART1_ TX	-	-		-	EVENT OUT
PB7	-	TIM17_ CH1N	TIM4_ CH2	TSC_ G5_IO4	I2C1_ SDA		-	USART1_ RX	-	-	TIM3_ CH4	-	EVENT OUT
PB8	-	TIM16_ CH1	TIM4_ CH3	TSC_ SYNC	I2C1_SCL	-	-	-	COMP1_ OUT	CAN_RX		TIM1_ BKIN	EVENT OUT
PB9	-	TIM17_ CH1	TIM4_ CH4		I2C1_ SDA	-	IR_OUT	-	COMP2_ OUT	CAN_TX		-	EVENT OUT
PB10	-	TIM2_ CH3	-	TSC_ SYNC	-	-	-	USART3_ TX	-	-	-	-	EVENT OUT
PB11	-	TIM2_ CH4	-	TSC_ G6_IO1	-	-	-	USART3_ RX	-	-	-	-	EVENT OUT
PB12	-	-	-	TSC_ G6_IO2	I2C2_ SMBA	SPI2_NSS, I2S2_WS	TIM1_ BKIN	USART3_ CK	-	-	-	-	EVENT OUT

6.1.6 Power supply scheme

Figure 11. Power supply scheme



1. Dotted lines represent the internal connections on low pin count packages, joining the dedicated supply pins.

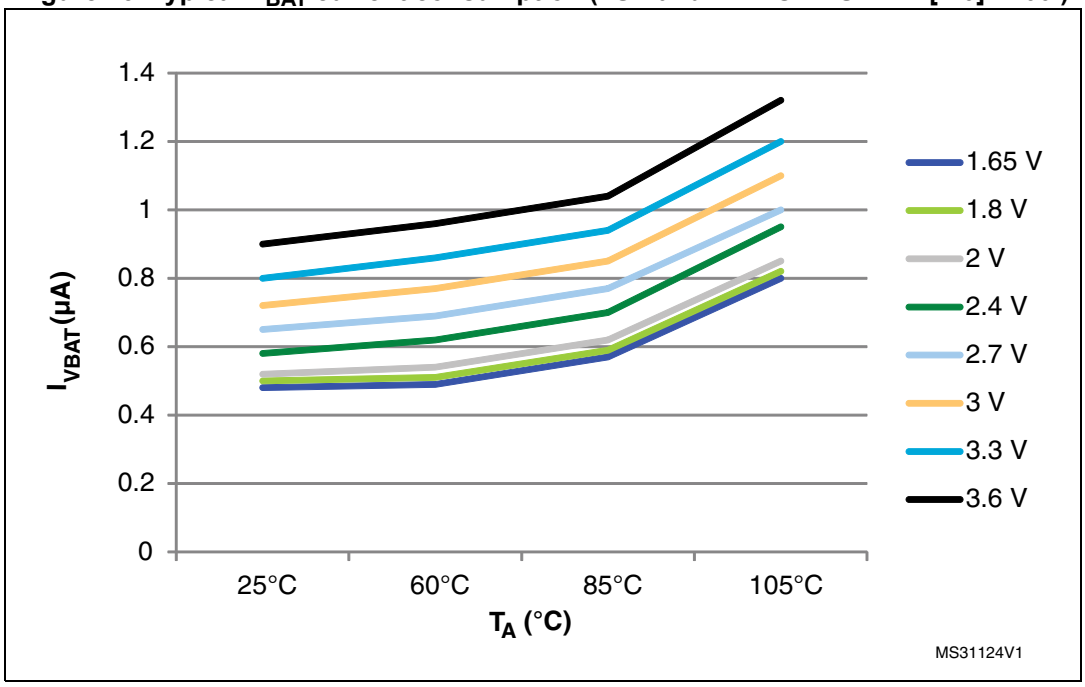
Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc..) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

Table 34. Typical and maximum current consumption from V_{BAT} supply

Symbol	Para meter	Conditions (1)	Typ @V_{BAT}								Max @V_{BAT} = 3.6 V(2)			Unit
			1.65V	1.8V	2V	2.4V	2.7V	3V	3.3V	3.6V	T_A = 25°C	T_A = 85°C	T_A = 105°C	
I_{DD_VBAT}	Backup domain supply current	LSE & RTC ON; "Xtal mode" lower driving capability; LSEDRV[1:0] = '00'	0.48	0.50	0.52	0.58	0.65	0.72	0.80	0.90	1.1	1.5	2.0	µA
		LSE & RTC ON; "Xtal mode" higher driving capability; LSEDRV[1:0] = '11'	0.83	0.86	0.90	0.98	1.03	1.10	1.20	1.30	1.5	2.2	2.9	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a CL of 6 pF for typical values.
2. Guaranteed by characterization results.

Figure 13. Typical V_{BAT} current consumption (LSE and RTC ON/LSEDRV[1:0] = '00')



Typical current consumption

The MCU is placed under the following conditions:

- $V_{DD} = V_{DDA} = 3.3$ V
- All I/O pins available on each package are in analog input configuration
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait states from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz), and Flash prefetch is ON
- When the peripherals are enabled, $f_{APB1} = f_{AHB/2}$, $f_{APB2} = f_{AHB}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8,16 and 64 is used for the frequencies 4 MHz, 2 MHz, 1 MHz, 500 kHz and 125 kHz respectively.

Table 35. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Run mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash	72 MHz	61.3	28.0	mA
			64 MHz	54.8	25.4	
			48 MHz	41.9	19.3	
			32 MHz	28.5	13.3	
			24 MHz	21.8	10.4	
			16 MHz	14.9	7.2	
			8 MHz	7.7	3.9	
			4 MHz	4.5	2.5	
			2 MHz	2.8	1.7	
			1 MHz	1.9	1.3	
			500 kHz	1.4	1.1	
			125 kHz	1.1	0.9	
I_{DDA} (1) (2)	Supply current in Run mode from V_{DDA} supply		72 MHz	240.3	239.5	µA
			64 MHz	210.9	210.3	
			48 MHz	155.8	155.6	
			32 MHz	105.7	105.6	
			24 MHz	82.1	82.0	
			16 MHz	58.8	58.8	
			8 MHz	2.4	2.4	
			4 MHz	2.4	2.4	
			2 MHz	2.4	2.4	
			1 MHz	2.4	2.4	
			500 kHz	2.4	2.4	
			125 kHz	2.4	2.4	

1. V_{DDA} monitoring is ON.
2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- all I/O pins are in analog input configuration
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature at 25°C and $V_{DD} = V_{DDA} = 3.3$ V.

Table 38. Peripheral current consumption

Peripheral	Typical consumption(1)	Unit
	I_{DD}	
BusMatrix (2)	12.6	µA/MHz
DMA1	7.6	
DMA2	6.1	
CRC	2.1	
GPIOA	10.0	
GPIOB	10.3	
GPIOC	2.2	
GPIOD	8.8	
GPIOE	3.3	
GPIOF	3.0	
TSC	5.5	
ADC1&2	17.3	
APB2-Bridge (3)	3.6	
SYSCFG	7.3	
TIM1	40.0	
SPI1	8.8	
USART1	23.3	
TIM15	17.1	
TIM16	10.1	
TIM17	11.0	
APB1-Bridge (3)	6.1	
TIM2	49.1	
TIM3	38.8	
TIM4	38.3	

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 49*. They are based on the EMS levels and classes defined in the application note AN1709.

Table 49. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25°C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25°C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 50. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/72 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 to 30 MHz	**7**	dBµV
			30 to 130 MHz	**20**	
			130 MHz to 1GHz	**27**	
			SAE EMI Level	**4**	-

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114, ANSI/ESD STM5.3.1 standard.

Table 51. ESD absolute maximum ratings

Symbol	Ratings	Conditions		Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114		2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	WLCSP100 package	3	250	
			Packages except WLCSP100	4	500	

1. Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 52. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence or oscillator frequency deviation).

The test results are given in *Table 53*.

Table 53. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	– 0	NA	mA
	Injected current on PC0, PC1, PC2, PC3, PF2, PA0, PA1, PA2, PA3, PF4, PA4, PA5, PA6, PA7, PC4, PC5, PB2 with induced leakage current on other pins from this group less than -50 µA	– 5	-	
	Injected current on PB0, PB1, PE7, PE8, PE9, PE10, PE11, PE12, PE13, PE14, PE15, PB12, PB13, PB14, PB15, PD8, PD9, PD10, PD11, PD12, PD13, PD14 with induced leakage current on other pins from this group less than -50 µA	– 5	-	
	Injected current on PC0, PC1, PC2, PC3, PF2, PA0, PA1, PA2, PA3, PF4, PA4, PA5, PA6, PA7, PC4, PC5, PB2, PB0, PB1, PE7, PE8, PE9, PE10, PE11, PE12, PE13, PE14, PE15, PB12, PB13, PB14, PB15, PD8, PD9, PD10, PD11, PD12, PD13, PD14 with induced leakage current on other pins from this group less than 400 µA	-	+5	
	Injected current on any other FT and FTf pins	– 5	NA	
	Injected current on any other pins	– 5	+5	

Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 22*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 22*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 55* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 24*. All I/Os (FT, TTa and TC unless otherwise specified) are CMOS and TTL compliant.

Table 55. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin	CMOS port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin	TTL port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	
V_{OH} (3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(1)(4)	Output low level voltage for an I/O pin	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	
V_{OH}(3)(4)	Output high level voltage for an I/O pin		V_{DD}–1.3	-	
V_{OL}(1)(4)	Output low level voltage for an I/O pin	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	
V_{OH}(3)(4)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OLFM+}(1)(4)	Output low level voltage for an FTf I/O pin in FM+ mode	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 22* and the sum of I_{IO} (I/O ports and control pins) must not exceed $\Sigma I_{IO(PIN)}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 22* and the sum of I_{IO} (I/O ports and control pins) must not exceed $\Sigma I_{IO(PIN)}$.
4. Data based on design simulation.

Table 59. IWDG min/max timeout period at 40 kHz (LSI) (1)

Prescaler divider	PR[2:0] bits	Min timeout (ms) RL[11:0]= 0x000	Max timeout (ms) RL[11:0]= 0xFFF
/4	0	0.1	409.6
/8	1	0.2	819.2
/16	2	0.4	1638.4
/32	3	0.8	3276.8
/64	4	1.6	6553.6
/128	5	3.2	13107.2
/256	7	6.4	26214.4

1. These timings are given for a 40 kHz clock but the microcontroller's internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 60. WWDG min-max timeout value @72 MHz (PCLK)(1)

Prescaler	WDGTB	Min timeout value	Max timeout value
1	0	0.05687	3.6409
2	1	0.1137	7.2817
4	2	0.2275	14.564
8	3	0.4551	29.127

1. Guaranteed by design.

Figure 26. SPI timing diagram - slave mode and CPHA = 0

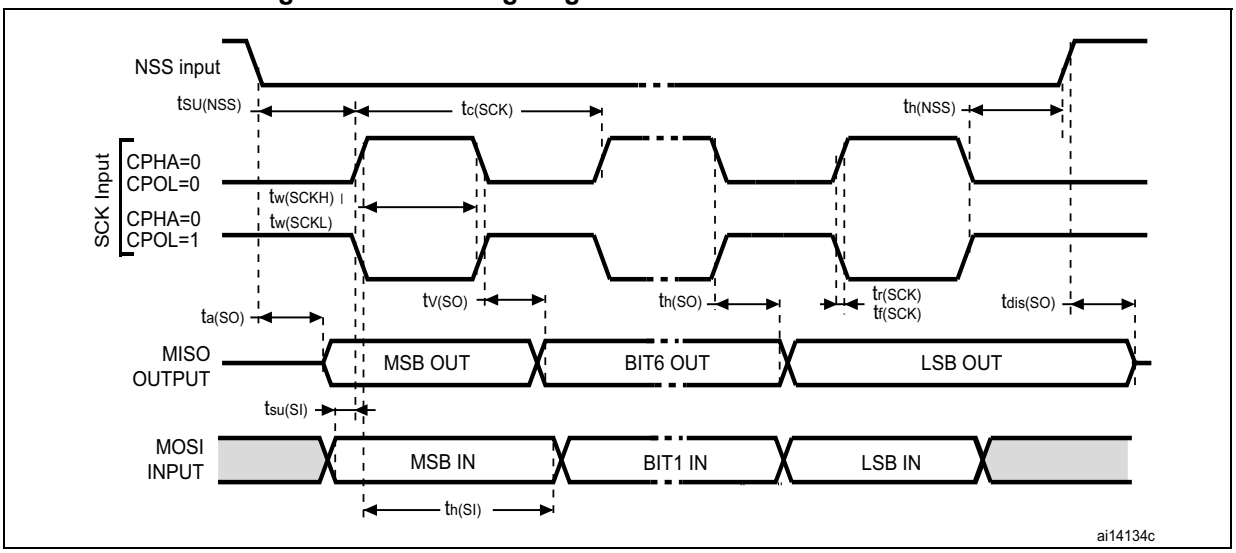
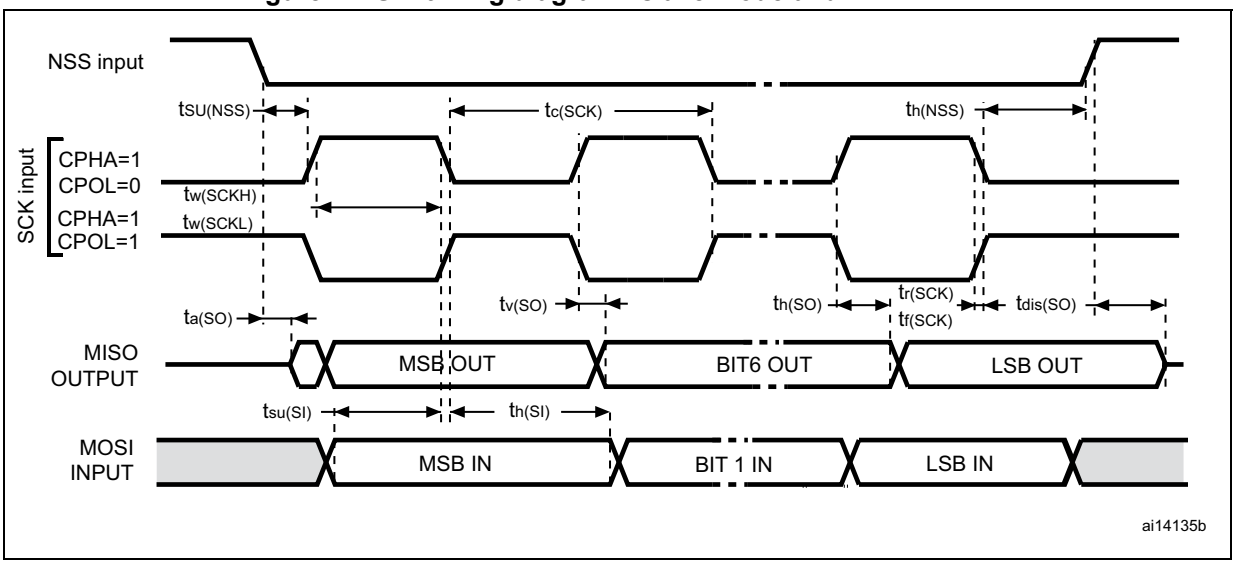


Figure 27. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Table 67. USB: Full-speed electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver characteristics						
t_r	Rise time(2)	C_L = 50 pF	4	-	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	-	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	-	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	-	2.0	V
Output driver Impedance(3)	Z_{DRV}	driving high and low	28	40	44	Ω

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).
3. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-), the matching impedance is already included in the embedded driver.

CAN (controller area network) interface

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

Table 71. ADC accuracy, 100-pin packages(1)(2)(3) (continued)

Symbol	Parameter	Conditions			Min (4)	Max(4)	Unit
SINAD (5)	Signal-to-noise and distortion ratio	ADC clock freq. ≤ 72 MHz, Sampling freq. ≤ 5 Msps, 2 V ≤ V_{DDA}, V_{REF+} ≤ 3.6 V 100-pin package	Single Ended	Fast channel 5.1 Ms	64	-	dB
				Slow channel 4.8 Ms	63	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
SNR(5)	Signal-to-noise ratio		Single Ended	Fast channel 5.1 Ms	64	-	
				Slow channel 4.8 Ms	64	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
THD(5)	Total harmonic distortion		Single Ended	Fast channel 5.1 Ms	-	-74	
				Slow channel 4.8 Ms	-	-74	
			Differential	Fast channel 5.1 Ms	-	-78	
				Slow channel 4.8 Ms	-	-76	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.14* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Guaranteed by characterization results.
5. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

7.5 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 24: General operating conditions on page 58*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 86. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	°C/W
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	55	
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	41	
	Thermal resistance junction-ambient WLCSP100 - 0.4 mm pitch	40	

7.5.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

8 Ordering information

Table 87. Ordering information scheme

Example: STM32 F 302 R B T 6 xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

302 = STM32F302xx

Pin count

C = 48 pins
R = 64 pins
V = 100 pins

Flash memory size

B = 128 Kbytes of Flash memory
C = 256 Kbytes of Flash memory

Package

T = LQFP
Y = WLCSP

Temperature range

6 = Industrial temperature range, –40 to 85 °C
7 = Industrial temperature range, –40 to 105 °C

Options

xxx = programmed parts
TR = tape and reel

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.