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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	52
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f302rct7

List of tables

Table 2. STM32F302xx family device features and peripheral counts

Peripheral		STM32F302Cx		STM32F302Rx		STM32F302Vx	
Flash (Kbytes)		128	256	128	256	128	256
SRAM (Kbytes) on data bus		32	40	32	40	32	40
Timers	Advanced control	1 (16-bit)					
	General purpose	5 (16-bit) 1 (32-bit)					
	Basic	1 (16-bit)					
PWM channels (all) (1)		26					
PWM channels (except complementary)		20					
Communication interfaces	SPI (I2S)(2)	3 (2)					
	I^2C	2					
	USART	3					
	UART	0		2			
	CAN	1					
	USB	1					
GPIOs	Normal I/Os (TC, TTa)	20		27		45 in LQFP100 37 in WLCSP100	
	5-volt tolerant I/Os (FT, FTf)	17		25		42 in LQFP100 40 in WLCSP100	
DMA channels		12					
Capacitive sensing channels		17		18		24	
12-bit ADCs		2					
Number of channels		9		16		17	
12-bit DAC channels		1					
Analog comparator		4					
Operational amplifiers		2					
CPU frequency		72 MHz					
Operating voltage		2.0 to 3.6 V					
Operating temperature		Ambient operating temperature: - 40 to 85 °C / - 40 to 105 °C Junction temperature: - 40 to 125 °C					
Packages		LQFP48		LQFP64		LQFP100 WLCSP100	

1. This total number considers also the PWMs generated on the complementary output channels
2. The SPI interfaces can work in an exclusive way in either the SPI mode or the I^2S audio mode.

Table 4. STM32F302xB/STM32F302xC peripheral interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action
GPIO RTCCLK HSE/32 MC0	TIM16	Clock source used as input channel for HSI and LSI calibration
CSS CPU (hard fault) COMPx PVD GPIO	TIM1, TIM15, 16, 17	Timer break
GPIO	TIMx	External trigger, timer break
	ADCx DAC1	Conversion external trigger
DAC1	COMPx	Comparator inverting input

Note: For more details about the interconnect actions, please refer to the corresponding sections in the reference manual (RM0365.

3.9 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

3.17.1 Advanced timer (TIM1)

The advanced-control timer, TIM1, can be seen as a three-phase PWM multiplexed on six channels. It has a complementary PWM output with programmable inserted dead-times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIM timers (described in *Section 3.17.2* using the same architecture, so the advanced-control timers can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

3.17.2 General-purpose timers (TIM2, TIM3, TIM4, TIM15, TIM16, TIM17)

There are up to six synchronizable general-purpose timers embedded in the STM32F302xB/STM32F302xC (see *Table 5* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, 3, and TIM4

  These are full-featured general-purpose timers:
  - TIM2 has a 32-bit auto-reload up/downcounter and 32-bit prescaler
  - TIM3 and 4 have 16-bit auto-reload up/downcounters and 16-bit prescalers.

  These timers all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

  The counters can be frozen in debug mode.

  All have independent DMA request generation and support quadrature encoders.
- TIM15, 16 and 17

  These three timers general-purpose timers with mid-range features:

  They have 16-bit auto-reload upcounters and 16-bit prescalers.
  - TIM15 has 2 channels and 1 complementary channel
  - TIM16 and TIM17 have 1 channel and 1 complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output.

  The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

  The counters can be frozen in debug mode.

3.17.3 Basic timer (TIM6)

This timer is mainly used for DAC trigger generation. It can also be used as a generic 16-bit time base.

- 17-bit Auto-reload counter for periodic interrupt with wakeup from STOP/STANDBY capability.

The RTC clock sources can be:
- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32.

3.19 Inter-integrated circuit interface (I^2C)

Up to two I^2C bus interfaces can operate in multimaster and slave modes. They can support standard (up to 100 KHz), fast (up to 400 KHz) and fast mode + (up to 1 MHz) modes.

Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

Table 6. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, they provide hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. They also have a clock domain independent from the CPU clock, allowing the I2Cx (x=1,2) to wake up the MCU from Stop mode on address match.

The I2C interfaces can be served by the DMA controller.

Refer to *Table 7* for the features available in I2C1 and I2C2.

Table 7. STM32F302xB/STM32F302xC I^2C implementation

I2C features[1]	I2C1	I2C2
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X
Independent clock	X	X

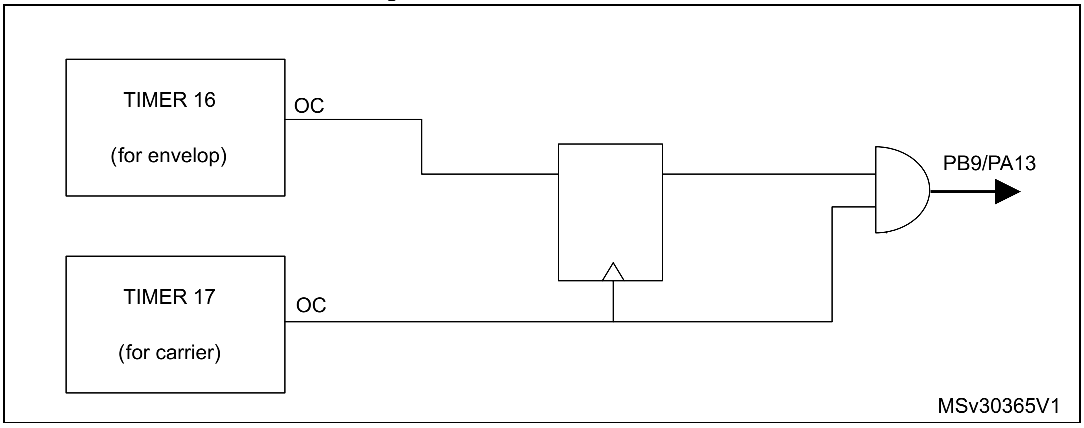
3.25 Infrared Transmitter

The STM32F302xB/STM32F302xC devices provide an infrared transmitter solution. The solution is based on internal connections between TIM16 and TIM17 as shown in the figure below.

TIM17 is used to provide the carrier frequency and TIM16 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate the infrared remote control signals, TIM16 channel 1 and TIM17 channel 1 must be properly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming the two timers output compare channels.

Figure 3. Infrared transmitter



3.26 Touch sensing controller (TSC)

The STM32F302xB/STM32F302xC devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 24 capacitive sensing channels distributed over 8 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

Table 13. STM32F302xB/STM32F302xC pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
WLCSP100	LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
C9	7	2	2	PC13(2)	I/O	TC	-	TIM1_CH1N	WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT
C10	8	3	3	PC14(2) OSC32_IN (PC14)	I/O	TC	-	-	OSC32_IN
D9	9	4	4	PC15(2) OSC32_OUT (PC15)	I/O	TC	-	-	OSC32_OUT
D10	10	-	-	PF9	I/O	FT	(1)	TIM15_CH1, SPI2_SCK, EVENTOUT	-
E10	11	-	-	PF10	I/O	FT	(1)	TIM15_CH2, SPI2_SCK, EVENTOUT	-
F10	12	5	5	PF0-OSC_IN (PF0)	I/O	FTf	-	TIM1_CH3N, I2C2_SDA,	OSC_IN
F9	13	6	6	PF1-OSC_OUT (PF1)	I/O	FTf	-	I2C2_SCL	OSC_OUT
E9	14	7	7	NRST	I/O	RST		Device reset input / internal reset output (active low)	
G10	15	8	-	PC0	I/O	TTa	(1)	EVENTOUT	ADC12_IN6
G9	16	9	-	PC1	I/O	TTa	(1)	EVENTOUT	ADC12_IN7
G8	17	10	-	PC2	I/O	TTa	(1)	EVENTOUT	ADC12_IN8
H10	18	11	-	PC3	I/O	TTa	(1)	TIM1_BKIN2, EVENTOUT	ADC12_IN9
E8	19	-	-	PF2	I/O	TTa	(1)	EVENTOUT	ADC12_IN10
H8	20	12	8	VSSA/ VREF-	S	-	-	Analog ground/Negative reference voltage	
J8	21	-	-	VREF+(3)	S	-	-	Positive reference voltage	
J10	22	-	-	VDDA	S	-	-	Analog power supply	
-	-	13	9	VDDA/ VREF+	S	-	-	Analog power supply/Positive reference voltage	
H9	23	14	10	PA0	I/O	TTa	(4)	USART2_CTS, TIM2_CH1_ETR, TSC_G1_IO1, COMP1_OUT, EVENTOUT	ADC1_IN1, COMP1_INM, RTC_ TAMP2, WKUP1

Table 13. STM32F302xB/STM32F302xC pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
WLCSP100	LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
J9	24	15	11	PA1	I/O	TTa	(4)	USART2_RTS_DE, TIM2_CH2, TSC_G1_IO2, TIM15_CH1N, RTC_REFIN, EVENTOUT	ADC1_IN2, COMP1_INP, OPAMP1_VINP
F7	25	16	12	PA2	I/O	TTa	(4) (5)	USART2_TX, TIM2_CH3, TIM15_CH1, TSC_G1_IO3, COMP2_OUT, EVENTOUT	ADC1_IN3, COMP2_INM, OPAMP1_VOUT
G7	26	17	13	PA3	I/O	TTa	(4)	USART2_RX, TIM2_CH4, TIM15_CH2, TSC_G1_IO4, EVENTOUT	ADC1_IN4, OPAMP1_VINP, COMP2_INP, OPAMP1_VINM
-	27	18	-	PF4	I/O	TTa	(1) (4)	COMP1_OUT, EVENTOUT	ADC1_IN5
K9, K10	-	-	-	VSS	S	-	-	Digital ground	
K8	28	19	-	VDD	S	-	-	Digital power supply	
J7	29	20	14	PA4	I/O	TTa	(4) (5)	SPI1_NSS, SPI3_NSS,I2S3_WS, USART2_CK, TSC_G2_IO1, TIM3_CH2, EVENTOUT	ADC2_IN1, DAC1_OUT1, COMP1_INM, COMP2_INM, COMP4_INM, COMP6_INM
H7	30	21	15	PA5	I/O	TTa	(4) (5)	SPI1_SCK, TIM2_CH1_ETR, TSC_G2_IO2, EVENTOUT	ADC2_IN2 OPAMP1_VINP, OPAMP2_VINM COMP1_INM, COMP2_INM, COMP4_INM, COMP6_INM
H6	31	22	16	PA6	I/O	TTa	(4) (5)	SPI1_MISO, TIM3_CH1, TIM1_BKIN, TIM16_CH1, COMP1_OUT, TSC_G2_IO3, EVENTOUT	ADC2_IN3, OPAMP2_VOUT
K7	32	23	17	PA7	I/O	TTa	(4)	SPI1_MOSI, TIM3_CH2, TIM17_CH1, TIM1_CH1N, , TSC_G2_IO4, COMP2_OUT, EVENTOUT	ADC2_IN4, COMP2_INP, OPAMP2_VINP, OPAMP1_VINP
G6	33	24	-	PC4	I/O	TTa	(1) (4)	USART1_TX, EVENTOUT	ADC2_IN5
F6	34	25	-	PC5	I/O	TTa	(1)	USART1_RX, TSC_G3_IO1, EVENTOUT	ADC2_IN11, OPAMP2_VINM, OPAMP1_VINM
J6	35	26	18	PB0	I/O	TTa	-	TIM3_CH3, TIM1_CH2N, TSC_G3_IO2, EVENTOUT	COMP4_INP, OPAMP2_VINP

5 Memory mapping

Figure 8. STM32F302xB/STM32F302xC memory map

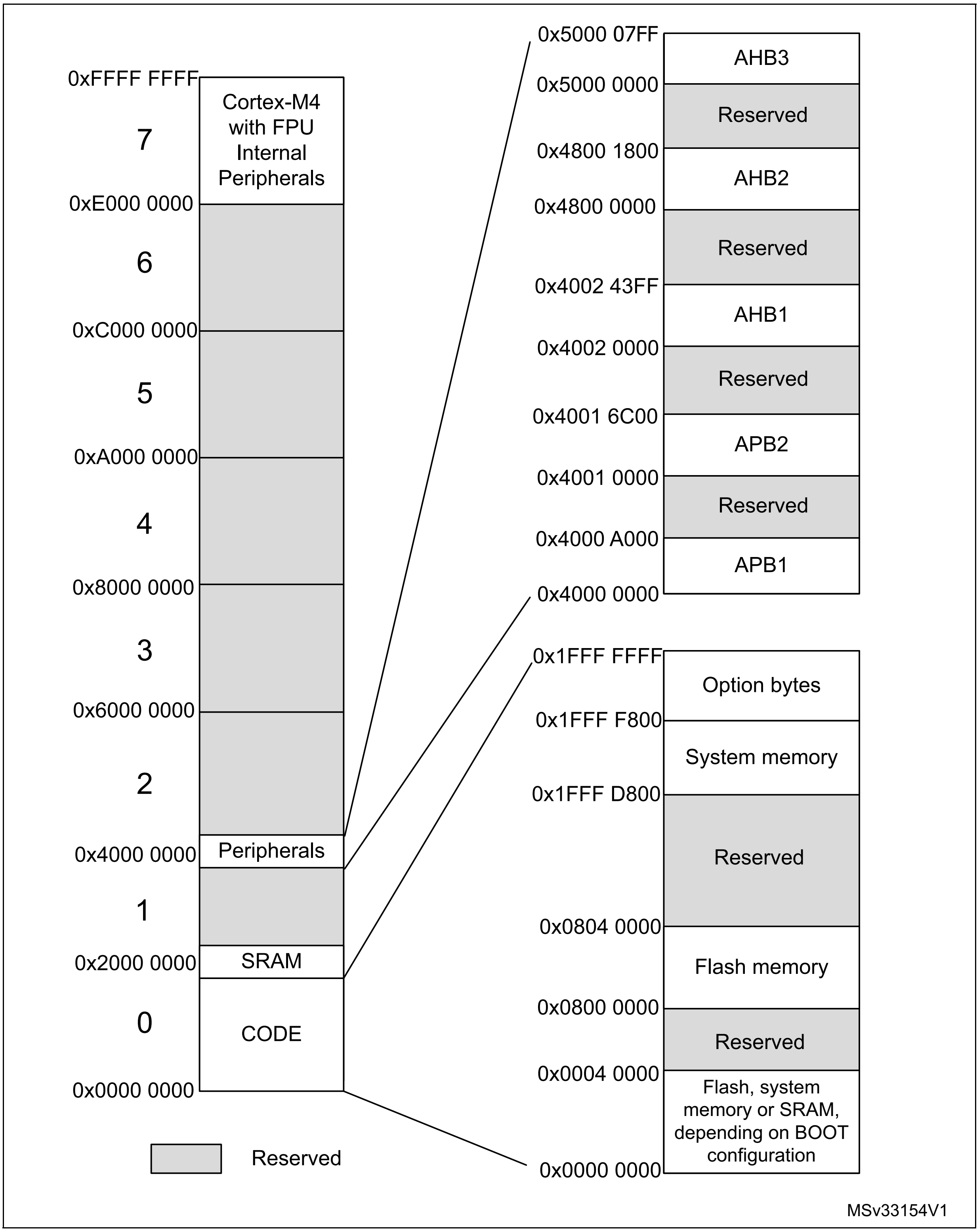


Table 20. STM32F302xB/STM32F302xC memory map, peripheral register boundary addresses

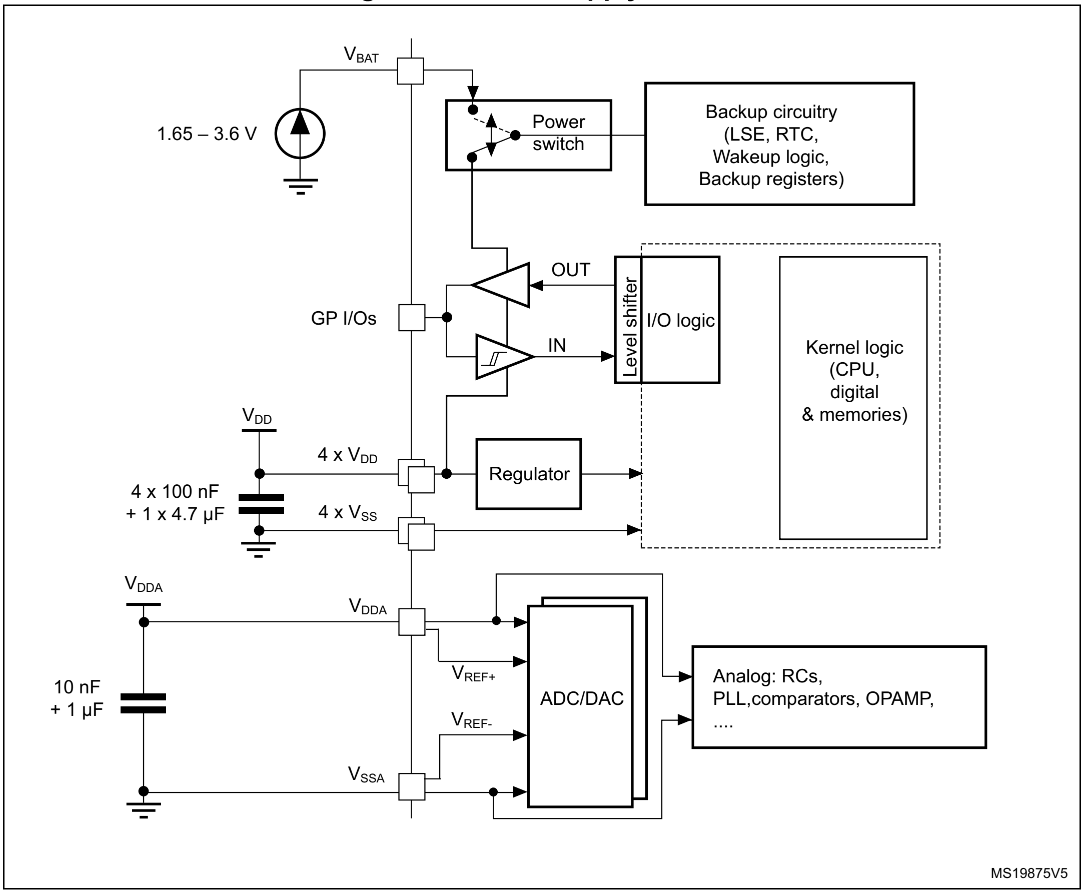
Bus	Boundary address	Size (bytes)	Peripheral
	0x5000 0400 - 0x5000 07FF	1 K	Reserved
AHB3	0x5000 0000 - 0x5000 03FF	1 K	ADC1 - ADC2
	0x4800 1800 - 0x4FFF FFFF	~132 M	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1 K	GPIOF
	0x4800 1000 - 0x4800 13FF	1 K	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1 K	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 K	GPIOC
	0x4800 0400 - 0x4800 07FF	1 K	GPIOB
	0x4800 0000 - 0x4800 03FF	1 K	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 M	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 K	TSC
	0x4002 3400 - 0x4002 3FFF	3 K	Reserved
	0x4002 3000 - 0x4002 33FF	1 K	CRC
	0x4002 2400 - 0x4002 2FFF	3 K	Reserved
	0x4002 2000 - 0x4002 23FF	1 K	Flash interface
	0x4002 1400 - 0x4002 1FFF	3 K	Reserved
	0x4002 1000 - 0x4002 13FF	1 K	RCC
	0x4002 0800 - 0x4002 0FFF	2 K	Reserved
	0x4002 0400 - 0x4002 07FF	1 K	DMA2
	0x4002 0000 - 0x4002 03FF	1 K	DMA1
	0x4001 8000 - 0x4001 FFFF	32 K	Reserved
APB2	0x4001 4C00 - 0x4001 7FFF	13 K	Reserved
	0x4001 4800 - 0x4001 4BFF	1 K	TIM17
	0x4001 4400 - 0x4001 47FF	1 K	TIM16
	0x4001 4000 - 0x4001 43FF	1 K	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 K	Reserved
	0x4001 3800 - 0x4001 3BFF	1 K	USART1
	0x4001 3400 - 0x4001 37FF	1 K	Reserved
	0x4001 3000 - 0x4001 33FF	1 K	SPI1
	0x4001 2C00 - 0x4001 2FFF	1 K	TIM1
	0x4001 0800 - 0x4001 2BFF	9 K	Reserved
	0x4001 0400 - 0x4001 07FF	1 K	EXTI
	0x4001 0000 - 0x4001 03FF	1 K	SYSCFG + COMP + OPAMP

Table 20. STM32F302xB/STM32F302xC memory map, peripheral register boundary addresses (continued)

Bus	Boundary address	Size (bytes)	Peripheral
	0x4000 8000 - 0x4000 FFFF	32 K	Reserved
APB1	0x4000 7800 - 0x4000 7FFF	2 K	Reserved
	0x4000 7400 - 0x4000 77FF	1 K	DAC
	0x4000 7000 - 0x4000 73FF	1 K	PWR
	0x4000 6800 - 0x4000 6FFF	2 K	Reserved
	0x4000 6400 - 0x4000 67FF	1 K	bxCAN
	0x4000 6000 - 0x4000 63FF	1 K	USB SRAM 512 bytes
	0x4000 5C00 - 0x4000 5FFF	1 K	USB device FS
	0x4000 5800 - 0x4000 5BFF	1 K	I2C2
	0x4000 5400 - 0x4000 57FF	1 K	I2C1
	0x4000 5000 - 0x4000 53FF	1 K	UART5
	0x4000 4C00 - 0x4000 4FFF	1 K	UART4
	0x4000 4800 - 0x4000 4BFF	1 K	USART3
	0x4000 4400 - 0x4000 47FF	1 K	USART2
	0x4000 4000 - 0x4000 43FF	1 K	I2S3ext
	0x4000 3C00 - 0x4000 3FFF	1 K	SPI3/I2S3
	0x4000 3800 - 0x4000 3BFF	1 K	SPI2/I2S2
	0x4000 3400 - 0x4000 37FF	1 K	I2S2ext
	0x4000 3000 - 0x4000 33FF	1 K	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 K	WWDG
	0x4000 2800 - 0x4000 2BFF	1 K	RTC
	0x4000 1800 - 0x4000 27FF	4 K	Reserved
	0x4000 1400 - 0x4000 17FF	1 K	Reserved
	0x4000 1000 - 0x4000 13FF	1 K	TIM6
	0x4000 0C00 - 0x4000 0FFF	1 K	Reserved
	0x4000 0800 - 0x4000 0BFF	1 K	TIM4
	0x4000 0400 - 0x4000 07FF	1 K	TIM3
	0x4000 0000 - 0x4000 03FF	1 K	TIM2

6.1.6 Power supply scheme

Figure 11. Power supply scheme



1. Dotted lines represent the internal connections on low pin count packages, joining the dedicated supply pins.

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc..) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

2. V_{REF+} must be always lower or equal than V_{DDA} ($V_{REF+} \leq V_{DDA}$). If unused then it must be connected to V_{DDA}.
3. V_{IN} maximum must always be respected. Refer to *Table 22: Current characteristics* for the maximum allowed injected current values.
4. Include VREF- pin.

Table 22. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all V_{DD} power lines (source)	160	mA
ΣI_{VSS}	Total current out of sum of all V_{SS} ground lines (sink)	–160	
I_{VDD}	Maximum current into each V_{DD} power line (source)(1)	100	
I_{VSS}	Maximum current out of each V_{SS} ground line (sink)(1)	–100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	–25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins(2)	80	
	Total output current sourced by sum of all IOs and control pins(2)	–80	
$I_{INJ(PIN)}$	Injected current on FT, FTf and B pins(3)	-5/+0	
	Injected current on TC and RST pin(4)	± 5	
	Injected current on TTa pins(5)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS} and V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins.The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 21: Voltage characteristics* for the maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN} > V_{DDA}$ while a negative injection is induced by $V_{IN} < V_{SS}$. I_{INJ}(PIN) must never be exceeded. Refer also to *Table 21: Voltage characteristics* for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note (2) below *Table 70*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 23. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

Table 38. Peripheral current consumption (continued)

Peripheral	Typical consumption[1]	Unit
	I_{DD}	
TIM6	9.7	µA/MHz
WWDG	6.4	
SPI2	40.4	
SPI3	40.0	
USART2	41.9	
USART3	40.2	
UART4	36.5	
UART5	30.8	
I2C1	10.5	
I2C2	10.4	
USB	26.2	
CAN	33.4	
PWR	5.7	
DAC	15.4	

1. The power consumption of the analog part (I_{DDA}) of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.
2. BusMatrix is automatically active when at least one master is ON (CPU, DMA1 or DMA2).
3. The APBx bridge is automatically active when at least one peripheral is ON on the same bus.

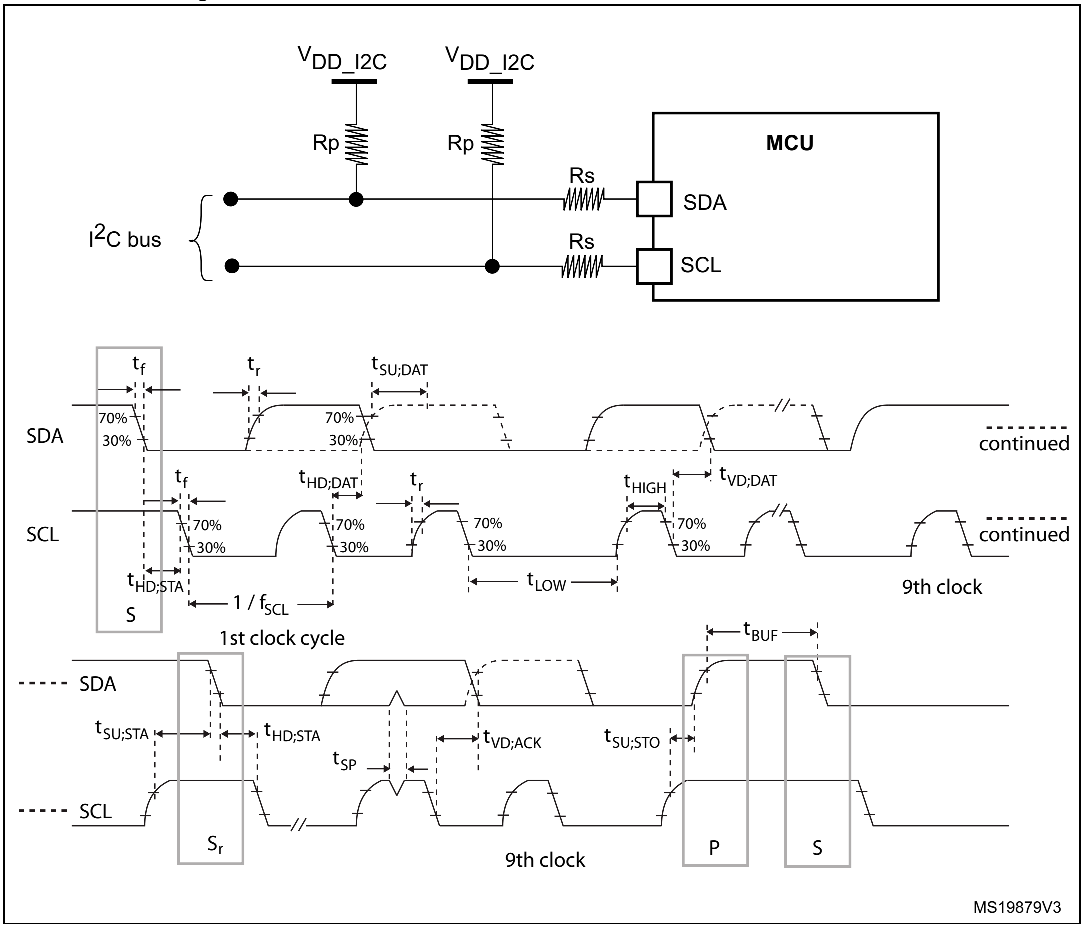
1. The I2C characteristics are the requirements from I2C bus specification rev03. They are guaranteed by design when I2Cx_TIMING register is correctly programmed (Refer to the RM0365 reference manual).
2. The maximum tHD;DAT could be 3.45 μs, 0.9 μs and 0.45 μs for standard mode, fast mode and fast mode plus, but must be less than the maximum of tVD;DAT or tVD;ACK by a transition time.
3. The minimum width of the spikes filtered by the analog filter is above t_{SP}(max).

Table 62. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Pulse width of spikes that are suppressed by the analog filter	50	260	ns

1. Guaranteed by design.

Figure 25. I²C bus AC waveforms and measurement circuit



1. Rs: Series protection resistors, Rp: Pull-up resistors, VDD_I2C: I2C bus supply.

Figure 26. SPI timing diagram - slave mode and CPHA = 0

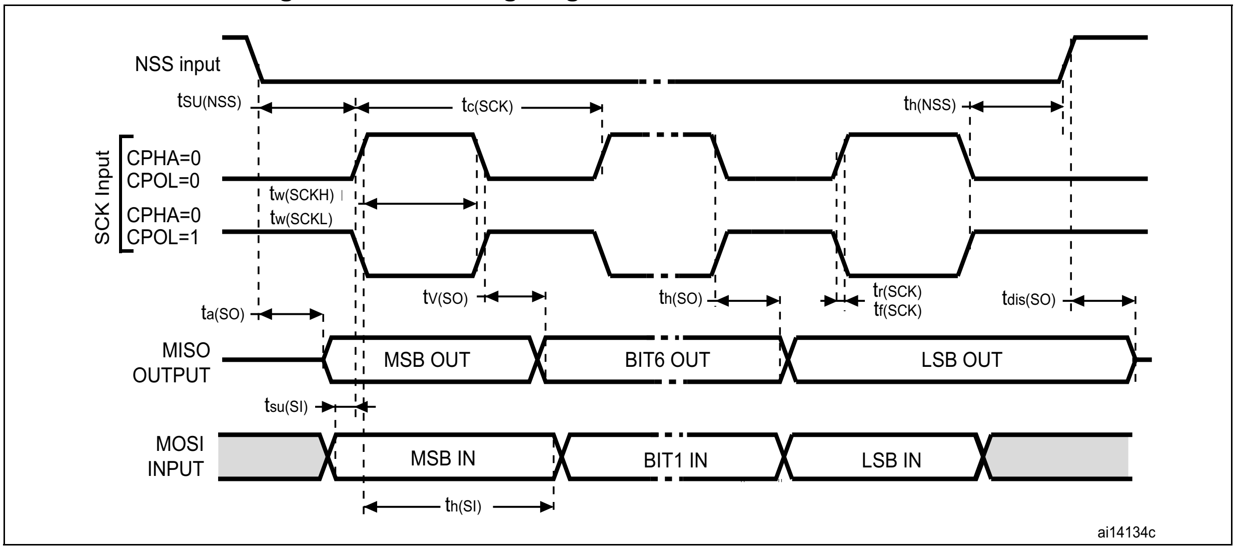
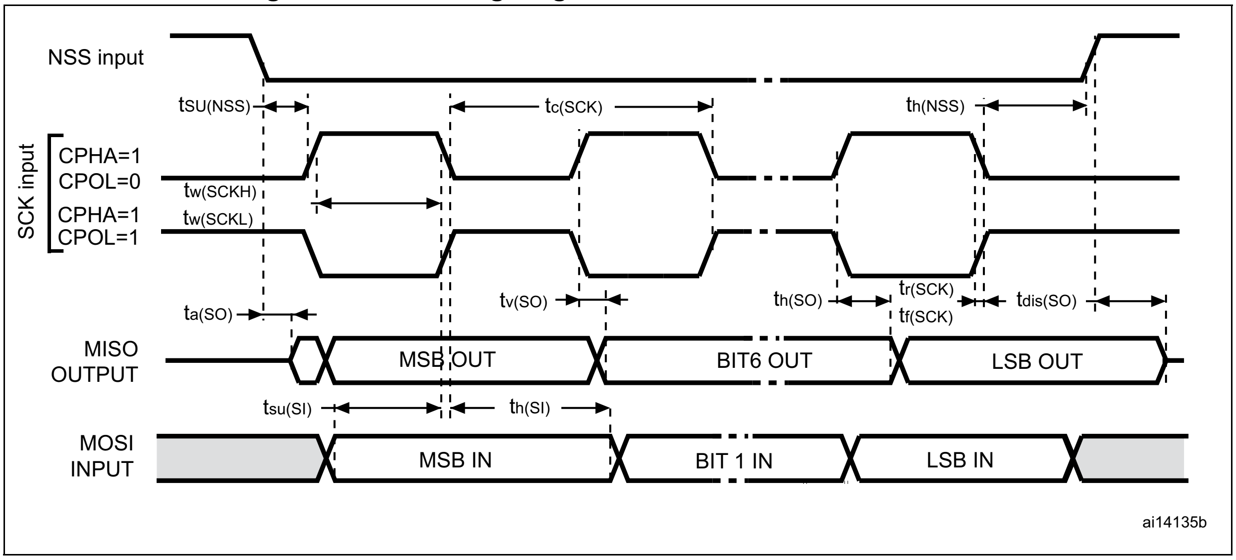
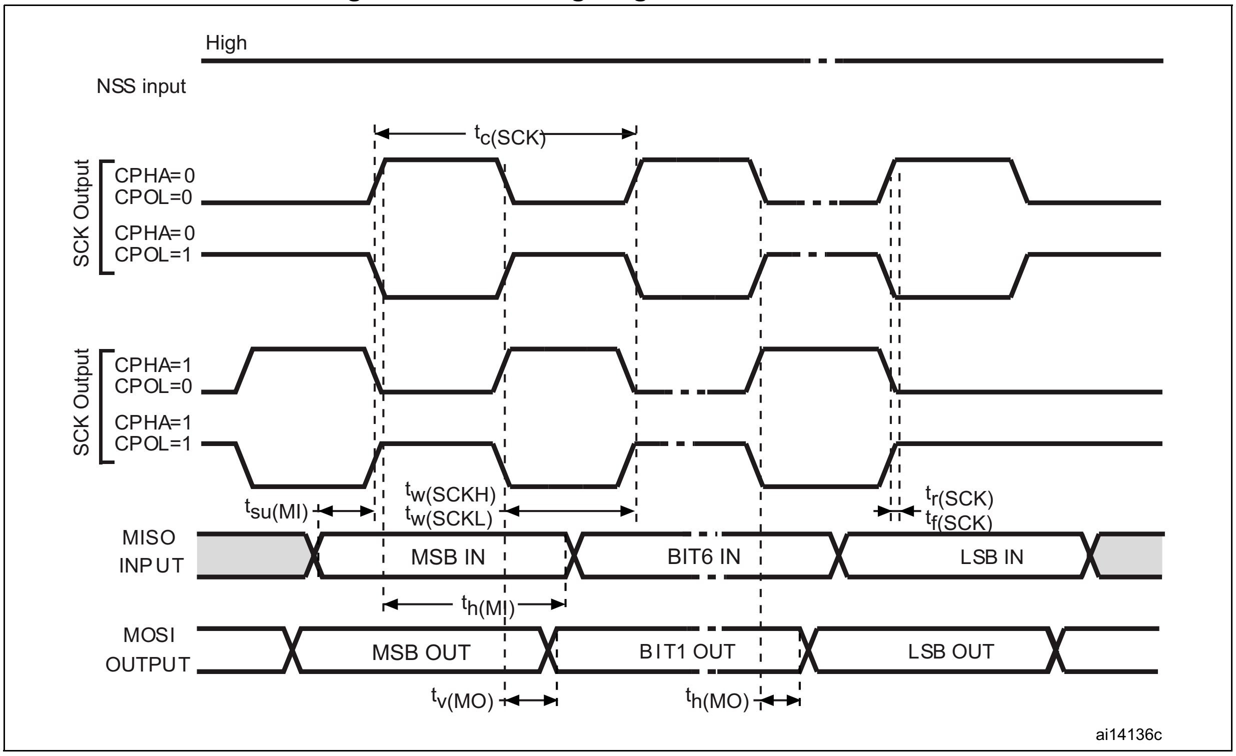


Figure 27. SPI timing diagram - slave mode and CPHA = 1[(1)]



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Figure 28. SPI timing diagram - master mode(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Table 72. ADC accuracy - limited test conditions, 64-pin packages(1)(2) (continued)

Symbol	Parameter	Conditions			Min (3)	Typ	Max (3)	Unit
SNR(4)	Signal-to-noise ratio	ADC clock freq. ≤ 72 MHz Sampling freq ≤ 5 Msps V_{DDA} = 3.3 V 25°C 64-pin package	Single ended	Fast channel 5.1 Ms	66	67	-	dB
				Slow channel 4.8 Ms	66	67	-	
			Differential	Fast channel 5.1 Ms	69	70	-	
				Slow channel 4.8 Ms	69	70	-	
THD(4)	Total harmonic distortion		Single ended	Fast channel 5.1 Ms	-	-80	-80	
				Slow channel 4.8 Ms	-	-78	-77	
			Differential	Fast channel 5.1 Ms	-	-83	-82	
				Slow channel 4.8 Ms	-	-81	-80	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.14* does not affect the ADC accuracy.
3. Guaranteed by characterization results.
4. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

8 Ordering information

Table 87. Ordering information scheme

Example: STM32 F 302 R B T 6 xxx

Device family
STM32 = ARM-based 32-bit microcontroller

Product type
F = general-purpose

Device subfamily
302 = STM32F302xx

Pin count
C = 48 pins
R = 64 pins
V = 100 pins

Flash memory size
B = 128 Kbytes of Flash memory
C = 256 Kbytes of Flash memory

Package
T = LQFP
Y = WLCSP

Temperature range
6 = Industrial temperature range, –40 to 85 °C
7 = Industrial temperature range, –40 to 105 °C

Options
xxx = programmed parts
TR = tape and reel

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

9 Revision history

Table 88. Document revision history

Date	Revision	Changes
21-Nov-2013	1	Initial release
16-Apr-2014	2	Updated *Table 38: Peripheral current consumption*. Updated SRAM size in *Table 2: STM32F302xx family device features and peripheral counts*, Cover page and description. Updated *Section 6.3.17: Communications interfaces* I^2C interface. Updated *Table 50: EMI characteristics* conditions :3.3v replaced by 3.6V. Updated *Table 77: Operational amplifier characteristics* adding TS_OPAMP_VOUT row. Updated *Section 3.13: Fast analog-to-digital converter (ADC)*. updated ARM and Cortex trademark. Updated *Table 32: Typical and maximum VDD consumption in Stop and Standby modes* with Max value at 85°C and 105°C. Updated *Table 70: ADC accuracy - limited test conditions, 100-pin packages* and *Table 71: ADC accuracy, 100-pin packages* for 100-pin package. Added *Table 72: ADC accuracy - limited test conditions, 64-pin packages* and *Table 73: ADC accuracy, 64-pin packages*for 64-pin package. Added *Table 74: ADC accuracy at 1MSPS* for 1MSPS sampling frequency. Updated *Table 63: SPI characteristics*. Updated *Table 75: DAC characteristics*. Updated note 2 and note 3 of *Table 69: Maximum ADC RAIN*.
09-Dec-2014	3	Updated core description in cover page. Updated HSI characteristics *Table 44: HSI oscillator characteristics* and *Figure 18: HSI oscillator accuracy characterization results for soldered parts*. Updated *Table 58: TIMx characteristics*. Updated *Table 16: STM32F302xB/STM32F302xC pin definitions* adding note for I/Os featuring an analog output function (DAC_OUT,OPAMP_OUT). Updated *Table 68: ADC characteristics* adding IDDA & IREF consumptions. Added *Figure 32: ADC typical current consumption on VDDA pin* and *Figure 33: ADC typical current consumption on VREF+ pin*. Added *Section 3.8: Interconnect matrix*. Added note after *Table 32: Typical and maximum VDD consumption in Stop and Standby modes*. Updated *Section 7: Package information* with new LQFP100, LQFP64, LQFP48 package marking. Updated *Table 16: STM32F302xB/STM32F302xC pin definitions* and alternate functions tables replacing usart_rts by usart_rts_de.