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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I ² S, POR, PWM, WDT
Number of I/O	52
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f302rct7tr

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3.7.4 Low-power modes

The STM32F302xB/STM32F302xC supports three low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep mode**
In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Stop mode**
Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.
The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the USB wakeup, the RTC alarm, COMPx, I2Cx or U(S)ARTx.
- **Standby mode**
The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.
The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin or an RTC alarm occurs.

Note: The RTC, the IWDG and the corresponding clock sources are not stopped by entering Stop or Standby mode.

3.8 Interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

Table 4. STM32F302xB/STM32F302xC peripheral interconnect matrix

Interconnect source	Interconnect destination	Interconnect action
TIMx	TIMx	Timers synchronization or chaining
	ADCx DAC1	Conversion triggers
	DMA	Memory to memory transfer trigger
	Comp _x	Comparator output blanking
COMPx	TIMx	Timer input: OCREF_CLR input, input capture
ADCx	TIMx	Timer triggered by analog watchdog

3.17.1 Advanced timer (TIM1)

The advanced-control timer, TIM1, can be seen as a three-phase PWM multiplexed on six channels. It has a complementary PWM output with programmable inserted dead-times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIM timers (described in [Section 3.17.2](#) using the same architecture, so the advanced-control timers can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

3.17.2 General-purpose timers (TIM2, TIM3, TIM4, TIM15, TIM16, TIM17)

There are up to six synchronizable general-purpose timers embedded in the STM32F302xB/STM32F302xC (see [Table 5](#) for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, 3, and TIM4

These are full-featured general-purpose timers:

- TIM2 has a 32-bit auto-reload up/downcounter and 32-bit prescaler
- TIM3 and 4 have 16-bit auto-reload up/downcounters and 16-bit prescalers.

These timers all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

The counters can be frozen in debug mode.

All have independent DMA request generation and support quadrature encoders.

- TIM15, 16 and 17

These three timers general-purpose timers with mid-range features:

They have 16-bit auto-reload upcounters and 16-bit prescalers.

- TIM15 has 2 channels and 1 complementary channel
- TIM16 and TIM17 have 1 channel and 1 complementary channel

All channels can be used for input capture/output compare, PWM or one-pulse mode output.

The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

The counters can be frozen in debug mode.

3.17.3 Basic timer (TIM6)

This timer is mainly used for DAC trigger generation. It can also be used as a generic 16-bit time base.

- 17-bit Auto-reload counter for periodic interrupt with wakeup from STOP/STANDBY capability.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32.

3.19 Inter-integrated circuit interface (I²C)

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard (up to 100 KHz), fast (up to 400 KHz) and fast mode + (up to 1 MHz) modes.

Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

Table 6. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, they provide hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. They also have a clock domain independent from the CPU clock, allowing the I2Cx (x=1,2) to wake up the MCU from Stop mode on address match.

The I2C interfaces can be served by the DMA controller.

Refer to [Table 7](#) for the features available in I2C1 and I2C2.

Table 7. STM32F302xB/STM32F302xC I²C implementation

I2C features ⁽¹⁾	I2C1	I2C2
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X
Independent clock	X	X

3.22 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I2S)

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Two standard I2S interfaces (multiplexed with SPI2 and SPI3) supporting four different audio standards can operate as master or slave at half-duplex and full duplex communication modes. They can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by 8-bit programmable linear prescaler. When operating in master mode it can output a clock for an external audio component at 256 times the sampling frequency.

Refer to [Table 9](#) for the features available in SPI1, SPI2 and SPI3.

Table 9. STM32F302xB/STM32F302xC SPI/I2S implementation

SPI features ⁽¹⁾	SPI1	SPI2	SPI3
Hardware CRC calculation	X	X	X
Rx/Tx FIFO	X	X	X
NSS pulse mode	X	X	X
I2S mode	-	X	X
TI mode	X	X	X

1. X = supported.

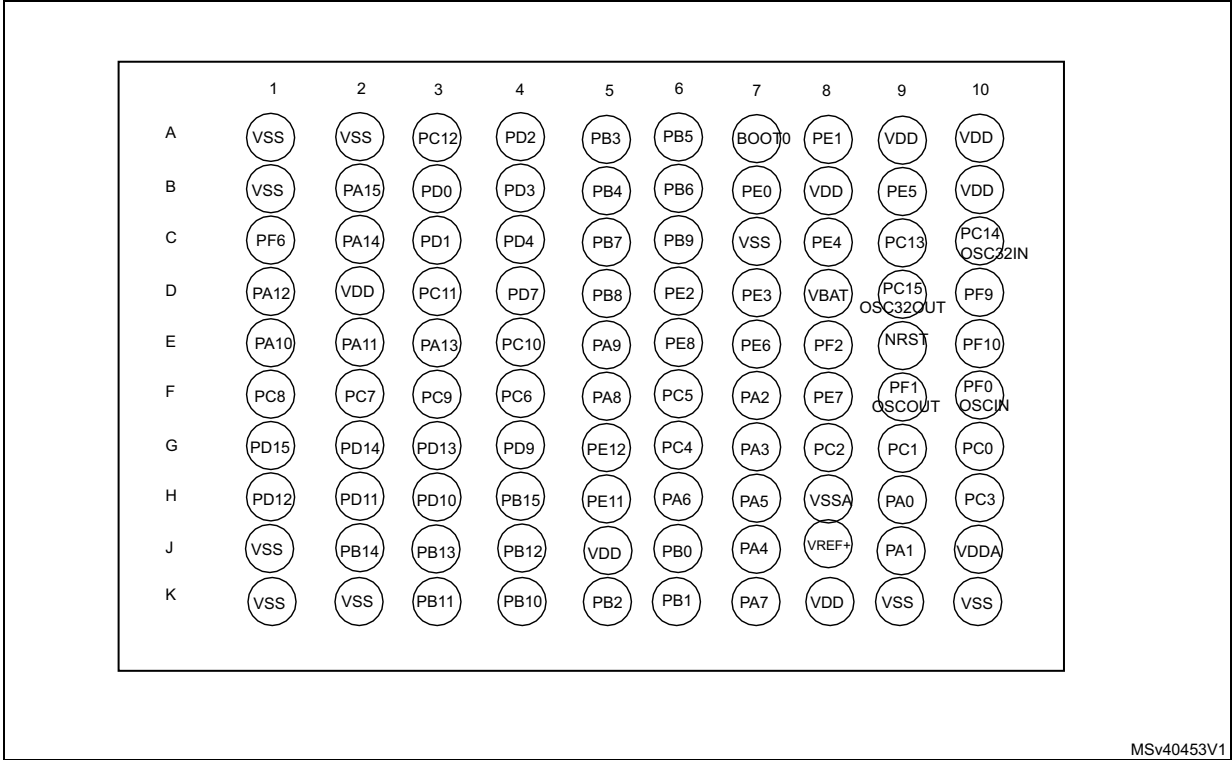
3.23 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

3.24 Universal serial bus (USB)

The STM32F302xB/STM32F302xC devices embed an USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator). The USB has a dedicated 512-bytes SRAM memory for data transmission and reception.

Figure 7. STM32F302xB/STM32F302xC WLCSP100 pinout



MSv40453V1

Table 12. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	3.3 V tolerant I/O directly connected to ADC
		TC	Standard 3.3V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 13. STM32F302xB/STM32F302xC pin definitions

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
WLCSP100	LQFP100	LQFP64	LQFP48					Alternate functions	Additional functions
D6	1	-	-	PE2	I/O	FT	(1)	TRACECK, TIM3_CH1, TSC_G7_IO1, EVENTOUT	-
D7	2	-	-	PE3	I/O	FT	(1)	TRACED0, TIM3_CH2, TSC_G7_IO2, EVENTOUT	-
C8	3	-	-	PE4	I/O	FT	(1)	TRACED1, TIM3_CH3, TSC_G7_IO3, EVENTOUT	-
B9	4	-	-	PE5	I/O	FT	(1)	TRACED2, TIM3_CH4, TSC_G7_IO4, EVENTOUT	-
E7	5	-	-	PE6	I/O	FT	(1)	TRACED3, EVENTOUT	WKUP3, RTC_TAMP3
D8	6	1	1	V _{BAT}	S	-	-	Backup power supply	

Table 14. Alternate functions for port A

Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF14	AF15
PA0	-	TIM2_CH1_ETR	-	TSC_G1_IO1	-	-	-	USART2_CTS	COMP1_OUT			-	-	-	EVENT OUT
PA1	RTC_REFIN	TIM2_CH2	-	TSC_G1_IO2	-	-	-	USART2_RTS_DE		TIM15_CH1N	-	-	-	-	EVENT OUT
PA2	-	TIM2_CH3	-	TSC_G1_IO3	-	-	-	USART2_TX	COMP2_OUT	TIM15_CH1	-	-	-	-	EVENT OUT
PA3	-	TIM2_CH4	-	TSC_G1_IO4	-	-	-	USART2_RX	-	TIM15_CH2	-	-	-	-	EVENT OUT
PA4	-	-	TIM3_CH2	TSC_G2_IO1	-	SPI1_NSS	SPI3_NSS, I2S3_WS	USART2_CK	-	-	-	-	-	-	EVENT OUT
PA5	-	TIM2_CH1_ETR	-	TSC_G2_IO2	-	SPI1_SCK	-	-	-	-	-	-	-	-	EVENT OUT
PA6	-	TIM16_CH1	TIM3_CH1	TSC_G2_IO3		SPI1_MISO	TIM1_BKIN	-	COMP1_OUT	-	-	-	-	-	EVENT OUT
PA7	-	TIM17_CH1	TIM3_CH2	TSC_G2_IO4		SPI1_MOSI	TIM1_CH1N	-	COMP2_OUT	-	-	-	-	-	EVENT OUT
PA8	MCO	-	-	-	I2C2_SMBA	I2S2_MCK	TIM1_CH1	USART1_CK		-	TIM4_ETR	-	-	-	EVENT OUT
PA9	-	-	-	TSC_G4_IO1	I2C2_SCL	I2S3_MCK	TIM1_CH2	USART1_TX		TIM15_BKIN	TIM2_CH3	-	-	-	EVENT OUT
PA10	-	TIM17_BKIN	-	TSC_G4_IO2	I2C2_SDA	-	TIM1_CH3	USART1_RX	COMP6_OUT	-	TIM2_CH4		-	-	EVENT OUT
PA11	-	-	-	-	-	-	TIM1_CH1N	USART1_CTS	COMP1_OUT	CAN_RX	TIM4_CH1	TIM1_CH4	TIM1_BKIN2	USB_DM	EVENT OUT

Table 14. Alternate functions for port A (continued)

Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF14	AF15
PA12	-	TIM16_CH1	-	-	-	-	TIM1_CH2N	USART1_RTS_DE	COMP2_OUT	CAN_TX	TIM4_CH2	TIM1_ETR	-	USB_DP	EVENT OUT
PA13	SWDIO-JTMS	TIM16_CH1N	-	TSC_G4_IO3	-	IR_OUT	-	USART3_CTS	-	-	TIM4_CH3	-	-	-	EVENT OUT
PA14	SWCLK-JTCK	-	-	TSC_G4_IO4	I2C1_SDA		TIM1_BKIN	USART2_TX	-	-	-	-	-	-	EVENT OUT
PA15	JTDI	TIM2_CH1_ETR		-	I2C1_SCL	SPI1_NSS	SPI3_NSS, I2S3_WS	USART2_RX	-	TIM1_BKIN	-	-	-	-	EVENT OUT

Table 16. Alternate functions for port C

Port & Pin Name	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0	EVENTOUT	-	-	-	-	-	-
PC1	EVENTOUT	-	-	-	-	-	-
PC2	EVENTOUT	-	COMP7_OUT	-	-	-	-
PC3	EVENTOUT	-	-	-	-	TIM1_BKIN2	-
PC4	EVENTOUT	-	-	-	-	-	USART1_TX
PC5	EVENTOUT	-	TSC_G3_IO1	-	-	-	USART1_RX
PC6	EVENTOUT	TIM3_CH1	-		-	I2S2_MCK	COMP6_OUT
PC7	EVENTOUT	TIM3_CH2	-		-	I2S3_MCK	
PC8	EVENTOUT	TIM3_CH3	-		-	-	
PC9	EVENTOUT	TIM3_CH4	-		I2S_CKIN		-
PC10	EVENTOUT	-	-		UART4_TX	SPI3_SCK, I2S3_CK	USART3_TX
PC11	EVENTOUT	-	-		UART4_RX	SPI3_MISO, I2S3ext_SD	USART3_RX
PC12	EVENTOUT	-	-		UART5_TX	SPI3_MOSI, I2S3_SD	USART3_CK
PC13	-	-	-	TIM1_CH1N	-	-	-
PC14	-	-	-	-	-	-	-
PC15	-	-	-	-	-	-	-

Table 18. Alternate functions for port E

Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF6	AF7
PE0	-	EVENTOUT	TIM4_ETR	-	TIM16_CH1	-	USART1_TX
PE1	-	EVENTOUT	-	-	TIM17_CH1	-	USART1_RX
PE2	TRACECK	EVENTOUT	TIM3_CH1	TSC_G7_IO1	-	-	-
PE3	TRACED0	EVENTOUT	TIM3_CH2	TSC_G7_IO2	-	-	-
PE4	TRACED1	EVENTOUT	TIM3_CH3	TSC_G7_IO3	-	-	-
PE5	TRACED2	EVENTOUT	TIM3_CH4	TSC_G7_IO4	-	-	-
PE6	TRACED3	EVENTOUT		-	-	-	-
PE7	-	EVENTOUT	TIM1_ETR	-	-	-	-
PE8	-	EVENTOUT	TIM1_CH1N	-	-	-	-
PE9	-	EVENTOUT	TIM1_CH1	-	-	-	-
PE10	-	EVENTOUT	TIM1_CH2N	-	-	-	-
PE11	-	EVENTOUT	TIM1_CH2	-	-	-	-
PE12	-	EVENTOUT	TIM1_CH3N	-	-	-	-
PE13	-	EVENTOUT	TIM1_CH3	-	-	-	-
PE14	-	EVENTOUT	TIM1_CH4	-	-	TIM1_BKIN2	-
PE15	-	EVENTOUT	TIM1_BKIN	-	-	-	USART3_RX

Table 19. Alternate functions for port F

Port & Pin Name	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0	-	-	-	I2C2_SDA	-	TIM1_CH3N	-
PF1	-	-	-	I2C2_SCL	-	-	-
PF2	EVENTOUT	-	-	-	-	-	-
PF4	EVENTOUT	COMP1_OUT	-	-	-	-	-
PF6	EVENTOUT	TIM4_CH4	-	I2C2_SCL	-	-	USART3_RTS_DE
PF9	EVENTOUT	-	TIM15_CH1	-	SPI2_SCK	-	-
PF10	EVENTOUT	-	TIM15_CH2	-	SPI2_SCK	-	-

Table 27. Programmable voltage detector characteristics

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ	Max ⁽¹⁾	Unit
V _{PVD0}	PVD threshold 0	Rising edge	2.1	2.18	2.26	V
		Falling edge	2	2.08	2.16	
V _{PVD1}	PVD threshold 1	Rising edge	2.19	2.28	2.37	
		Falling edge	2.09	2.18	2.27	
V _{PVD2}	PVD threshold 2	Rising edge	2.28	2.38	2.48	
		Falling edge	2.18	2.28	2.38	
V _{PVD3}	PVD threshold 3	Rising edge	2.38	2.48	2.58	
		Falling edge	2.28	2.38	2.48	
V _{PVD4}	PVD threshold 4	Rising edge	2.47	2.58	2.69	
		Falling edge	2.37	2.48	2.59	
V _{PVD5}	PVD threshold 5	Rising edge	2.57	2.68	2.79	
		Falling edge	2.47	2.58	2.69	
V _{PVD6}	PVD threshold 6	Rising edge	2.66	2.78	2.9	
		Falling edge	2.56	2.68	2.8	
V _{PVD7}	PVD threshold 7	Rising edge	2.76	2.88	3	
		Falling edge	2.66	2.78	2.9	
V _{PVDhyst} ⁽²⁾	PVD hysteresis	-	-	100	-	mV
IDD(PVD)	PVD current consumption	-	-	0.15	0.26	μA

1. Guaranteed by characterization results.

2. Guaranteed by design.

Table 30. Typical and maximum current consumption from V_{DD} supply at $V_{DD} = 3.6V$ (continued)

Symbol	Parameter	Conditions	f _{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T _A ⁽¹⁾			Typ	Max @ T _A ⁽¹⁾			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I _{DD}	Supply current in Sleep mode, executing from Flash or RAM	External clock (HSE bypass)	72 MHz	44.0	48.4	49.4	50.5	6.6	7.5	7.9	8.7	mA
			64 MHz	39.2	43.3	44.0	45.2	6.0	6.8	7.2	7.9	
			48 MHz	29.6	32.7	33.3	34.3	4.5	5.2	5.6	6.3	
			32 MHz	19.7	23.3	23.3	23.5	3.1	3.5	4.0	4.8	
			24 MHz	14.9	17.6	17.8	18.3	2.4	2.8	3.3	3.9	
			8 MHz	4.9	5.7	6.1	6.9	0.8	1.0	1.4	2.2	
			1 MHz	0.6	0.9	1.2	2.1	0.1	0.3	0.6	1.5	
		Internal clock (HSI)	64 MHz	34.2	38.1	39.2	40.3	5.7	6.3	6.8	7.5	
			48 MHz	25.8	28.7	29.6	30.3	4.3	4.8	5.2	5.9	
			32 MHz	17.4	19.4	19.9	20.7	2.9	3.2	3.7	4.5	
			24 MHz	13.2	15.1	15.6	15.9	1.5	1.8	2.2	2.9	
			8 MHz	4.5	5.0	5.6	6.2	0.7	0.9	1.2	2.1	

1. Guaranteed by characterization results unless otherwise specified.

2. Data based on characterization results and tested in production with code executing from RAM.

Table 31. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Parameter	Conditions (1)	f _{HCLK}	V _{DDA} = 2.4 V				V _{DDA} = 3.6 V				Unit
				Typ	Max @ T _A ⁽²⁾			Typ	Max @ T _A ⁽²⁾			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I _{DDA}	Supply current in Run/Sleep mode, code executing from Flash or RAM	HSE bypass	72 MHz	225	276	289	297	245	302	319	329	μA
			64 MHz	198	249	261	268	216	270	284	293	
			48 MHz	149	195	204	211	159	209	222	230	
			32 MHz	102	145	152	157	110	154	162	169	
			24 MHz	80	119	124	128	86	126	131	135	
			8 MHz	2	3	4	6	3	4	5	9	
			1 MHz	2	3	5	7	3	4	6	9	
		HSI clock	64 MHz	270	323	337	344	299	354	371	381	
			48 MHz	220	269	280	286	244	293	309	318	
			32 MHz	173	218	228	233	193	239	251	257	
			24 MHz	151	194	200	204	169	211	219	225	
			8 MHz	73	97	99	103	88	105	110	116	

1. Current consumption from the V_{DDA} supply is independent of whether the peripherals are on or off. Furthermore when the PLL is off, I_{DDA} is independent from the frequency.

2. Guaranteed by characterization results.

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in [Table 42](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 42. HSE oscillator characteristics

Symbol	Parameter	Conditions ⁽¹⁾	Min ⁽²⁾	Typ	Max ⁽²⁾	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistor	-	-	200	-	k Ω
I_{DD}	HSE current consumption	During startup ⁽³⁾	-	-	8.5	mA
		$V_{DD}=3.3\text{ V}$, $R_m=30\Omega$, $CL=10\text{ pF}@8\text{ MHz}$	-	0.4	-	
		$V_{DD}=3.3\text{ V}$, $R_m=45\Omega$, $CL=10\text{ pF}@8\text{ MHz}$	-	0.5	-	
		$V_{DD}=3.3\text{ V}$, $R_m=30\Omega$, $CL=5\text{ pF}@32\text{ MHz}$	-	0.8	-	
		$V_{DD}=3.3\text{ V}$, $R_m=30\Omega$, $CL=10\text{ pF}@32\text{ MHz}$	-	1	-	
		$V_{DD}=3.3\text{ V}$, $R_m=30\Omega$, $CL=20\text{ pF}@32\text{ MHz}$	-	1.5	-	
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 23](#) and [Table 56](#), respectively.

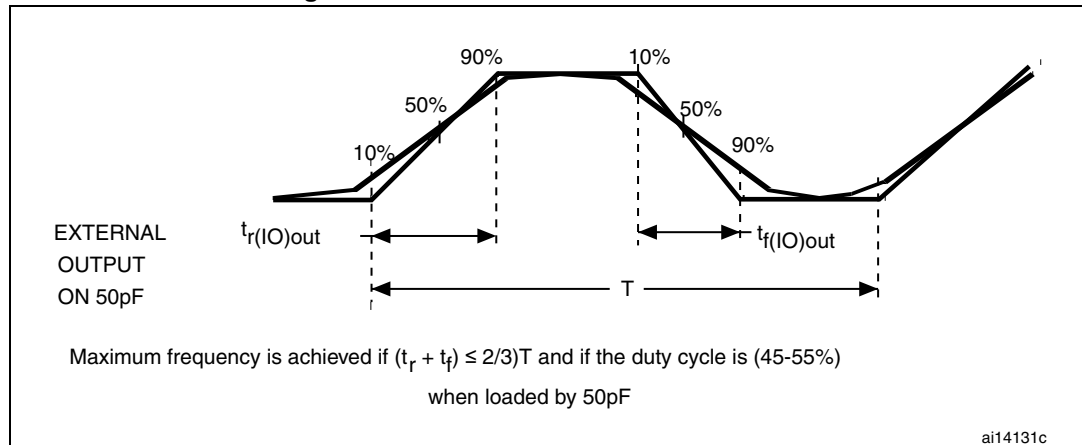
Unless otherwise specified, the parameters given are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 24](#).

Table 56. I/O AC characteristics⁽¹⁾

OSPEEDRx[1:0] value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽²⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	-	$2^{(3)}$	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	-	$125^{(3)}$	ns
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time		-	$125^{(3)}$	
01	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽²⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	-	$10^{(3)}$	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	-	$25^{(3)}$	ns
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time		-	$25^{(3)}$	
11	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽²⁾	$C_L = 30 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	$50^{(3)}$	MHz
			$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	$30^{(3)}$	MHz
			$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 2.7 \text{ V}$	-	$20^{(3)}$	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time	$C_L = 30 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	$5^{(3)}$	ns
			$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	$8^{(3)}$	
			$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 2.7 \text{ V}$	-	$12^{(3)}$	
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time	$C_L = 30 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	$5^{(3)}$	
			$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	$8^{(3)}$	
			$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 2.7 \text{ V}$	-	$12^{(3)}$	
FM+ configuration ⁽⁴⁾	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽²⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	-	$2^{(4)}$	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time		-	$12^{(4)}$	ns
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time		-	$34^{(4)}$	
-	$t_{\text{EXTI}pw}$	Pulse width of external signals detected by the EXTI controller	-	$10^{(3)}$	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the RM0365 reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in [Figure 23](#).
3. Guaranteed by design.
4. The I/O speed configuration is bypassed in FM+ I/O mode. Refer to the STM32F302xx STM32F312xx reference manual RM0365 for a description of FM+ I/O mode configuration.

Figure 23. I/O AC characteristics definition



6.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see [Table 54](#)).

Unless otherwise specified, the parameters given in [Table 57](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 24](#).

Table 57. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}^{(1)}$	NRST Input low level voltage	-	-	-	$0.3V_{DD} + 0.07^{(1)}$	V
$V_{IH(NRST)}^{(1)}$	NRST Input high level voltage	-	$0.445V_{DD} + 0.398^{(1)}$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor ⁽²⁾	$V_{IN} = V_{SS}$	25	40	55	k Ω
$V_{F(NRST)}^{(1)}$	NRST Input filtered pulse	-	-	-	$100^{(1)}$	ns
$V_{NF(NRST)}^{(1)}$	NRST Input not filtered pulse	-	$500^{(1)}$	-	-	ns

1. Guaranteed by design.

2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Table 72. ADC accuracy - limited test conditions, 64-pin packages⁽¹⁾⁽²⁾ (continued)

Symbol	Parameter	Conditions			Min (3)	Typ	Max (3)	Unit
SNR ⁽⁴⁾	Signal-to-noise ratio	ADC clock freq. ≤ 72 MHz Sampling freq ≤ 5 Msps V _{DDA} = 3.3 V 25°C 64-pin package	Single ended	Fast channel 5.1 Ms	66	67	-	dB
				Slow channel 4.8 Ms	66	67	-	
			Differential	Fast channel 5.1 Ms	69	70	-	
				Slow channel 4.8 Ms	69	70	-	
THD ⁽⁴⁾	Total harmonic distortion		Single ended	Fast channel 5.1 Ms	-	-80	-80	
				Slow channel 4.8 Ms	-	-78	-77	
			Differential	Fast channel 5.1 Ms	-	-83	-82	
				Slow channel 4.8 Ms	-	-81	-80	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in [Section 6.3.14](#) does not affect the ADC accuracy.
3. Guaranteed by characterization results.
4. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

Figure 34. ADC accuracy characteristics

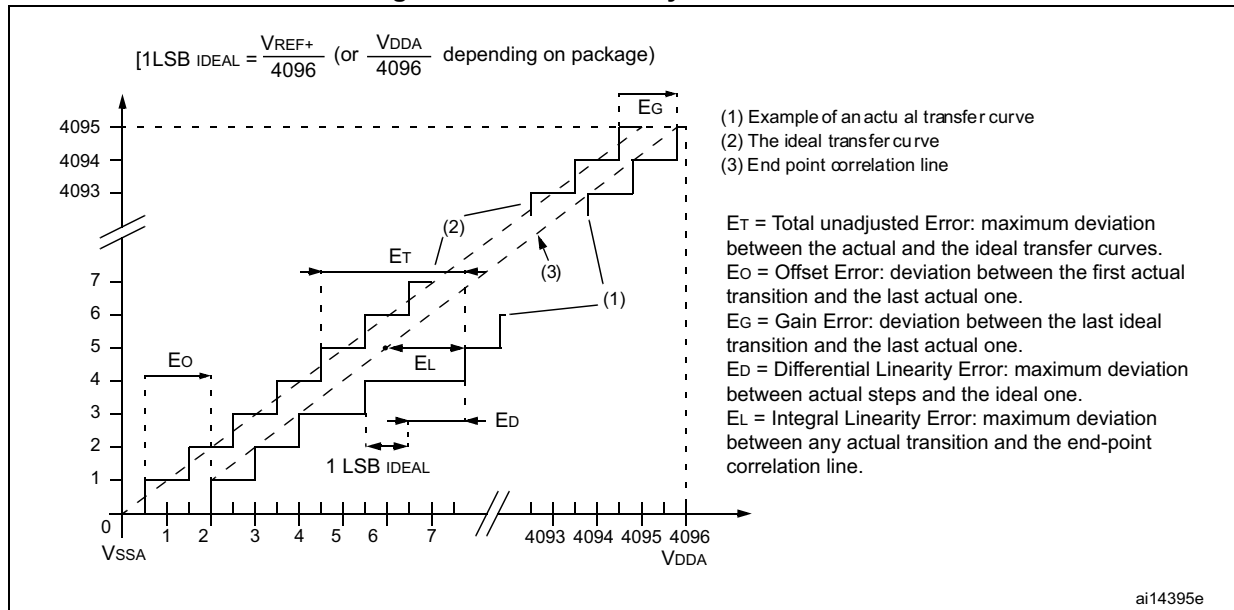
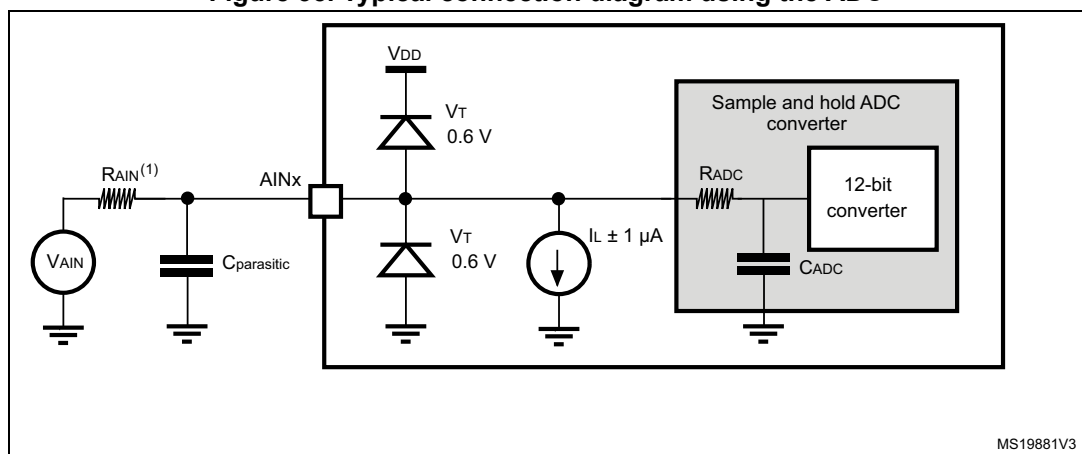


Figure 35. Typical connection diagram using the ADC



1. Refer to [Table 68](#) for the values of R_{AIN} .
2. $C_{\text{parasitic}}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{\text{parasitic}}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in [Figure 11](#). The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

Table 88. Document revision history (continued)

Date	Revision	Changes
29-Jan-2015	4	Updated cover page with ADC up to 17 channels. Updated Section 6.3.20: Comparator characteristics modifying ts_sc characteristics in Table 76 and adding Figure 37: Maximum VREFINT scaler startup time from power down. Updated I_{DD} data in Table 42: HSE oscillator characteristics.
17-Apr-2015	5	Updated Figure 1: STM32F302xB/STM32F302xC block diagram changing 32 KB of SRAM by 40 KB of SRAM. Updated Section 7: Package information: with new package information structure adding 1 sub paragraph for each package. Updated Figure 41: LQFP100 – 14 x 14 mm, low-profile quad flat package top view example removing gate mark. Added note for all package device markings: “the following figure gives an example of topside marking orientation versus pin 1 identifier location”. Updated Table 82: LQFP64 – 10 x 10 mm, low-profile quad flat package mechanical data. Updated Table 7: STM32F302xB/STM32F302xC peripheral interconnect matrix removing TIM8 reference and updating note below the table, replacing by a reference to RM0365.
22-Feb-2016	6	Added WLCSP100: – Updated cover page. – Updated Table 2: STM32F302xx family device features and peripheral counts. – Added Figure 7: STM32F302xB/STM32F302xC WLCSP100 pinout. – Updated Table 13: STM32F302xB/STM32F302xC pin definitions. – Updated Table 24: General operating conditions. – Added Section 7.4: WLCSP100 - 0.4 mm pitch wafer level chip scale package information. – Updated Table 86: Package thermal characteristics. – Updated Table 87: Ordering information scheme. Updated Figure 4, Figure 5, Figure 6, Table 13 and Table 22 removing all VDD and VSS indexes. Updated all the notes removing ‘not tested in production’. Updated Table 68: ADC characteristics adding V_{REF-} negative voltage reference. Updated Table 21: Voltage characteristics adding table note 4. Updated Table 43: LSE oscillator characteristics (fLSE = 32.768 kHz) LSEDRV[1:0] bits. Updated Table 28: Embedded internal reference voltage V_{REFINT} internal reference voltage (min and typ values). Updated Table 51: ESD absolute maximum ratings ESD CDM at class 3 and 4 including WLCSP100 package information.