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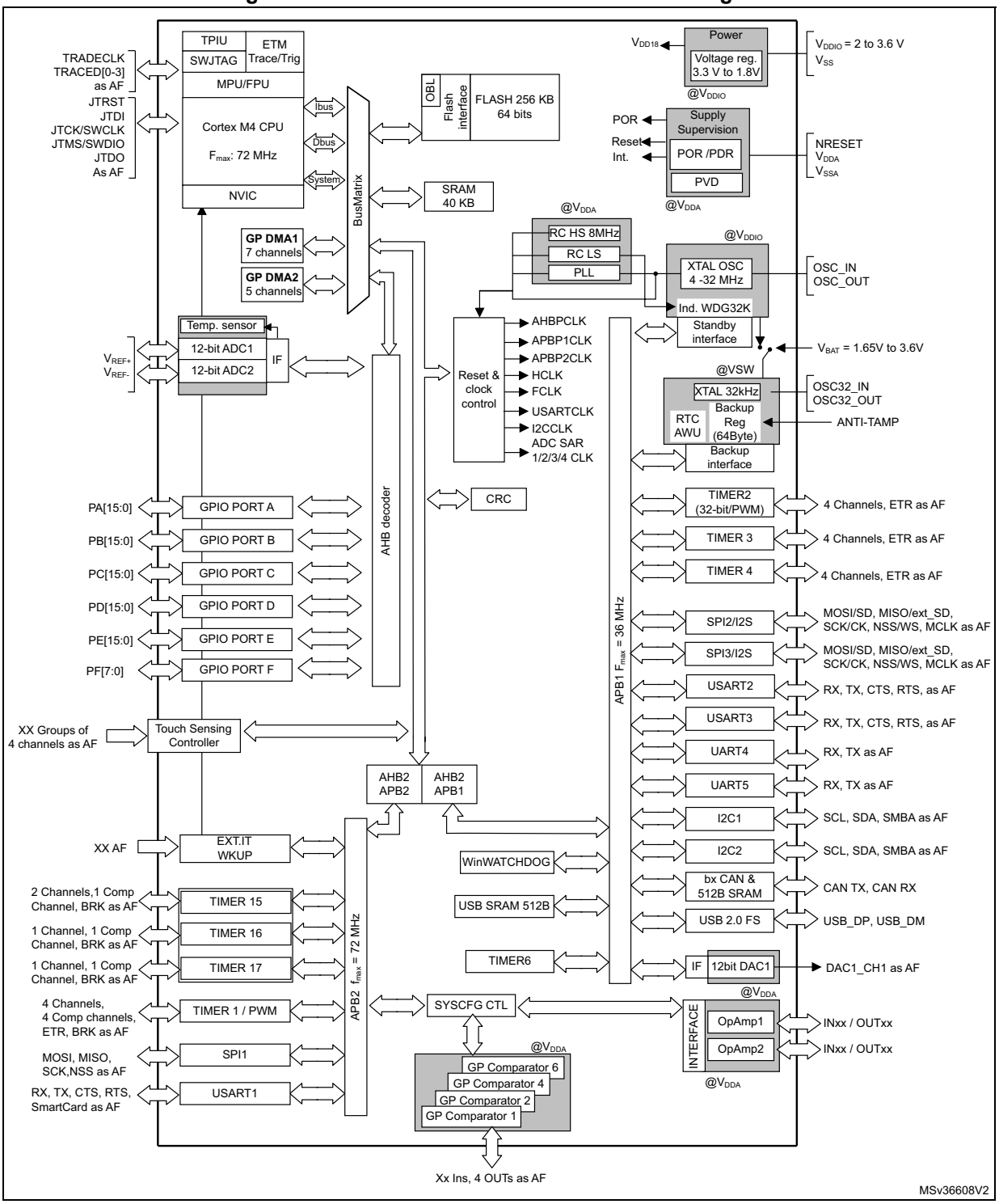
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | DMA, I²S, POR, PWM, WDT |
| Number of I/O | 87 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 40K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 17x12b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f302vct6 |

**Figure 1. STM32F302xB/STM32F302xC block diagram**




1. AF: alternate function on I/O pins.

# 3 Functional overview

## 3.1 ARM® Cortex®-M4 core with FPU with embedded Flash and SRAM

The ARM Cortex-M4 processor with FPU is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM Cortex-M4 32-bit RISC processor with FPU features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32F302xB/STM32F302xC family is compatible with all ARM tools and software.

*Figure 1* shows the general block diagram of the STM32F302xB/STM32F302xC family devices.

## 3.2 Memory protection unit (MPU)

The memory protection unit (MPU) is used to separate the processing of tasks from the data protection. The MPU can manage up to 8 protection areas that can all be further divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The memory protection unit is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

## 3.3 Embedded Flash memory

All STM32F302xB/STM32F302xC devices feature up to 256 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

### 3.7.4 Low-power modes

The STM32F302xB/STM32F302xC supports three low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- Sleep mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- Stop mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the USB wakeup, the RTC alarm, COMPx, I2Cx or U(S)ARTx.

- Standby mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin or an RTC alarm occurs.

*Note: The RTC, the IWDG and the corresponding clock sources are not stopped by entering Stop or Standby mode.*

## 3.8 Interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

**Table 4. STM32F302xB/STM32F302xC peripheral interconnect matrix**

| Interconnect source | Interconnect destination | Interconnect action |
|---|---|---|
| TIMx | TIMx | Timers synchronization or chaining |
| | ADCx<br>DAC1 | Conversion triggers |
| | DMA | Memory to memory transfer trigger |
| | Compx | Comparator output blanking |
| COMPx | TIMx | Timer input: OCREF_CLR input, input capture |
| ADCx | TIMx | Timer triggered by analog watchdog |

**Table 4. STM32F302xB/STM32F302xC peripheral interconnect matrix (continued)**

| Interconnect source | Interconnect destination | Interconnect action |
|---|---|---|
| GPIO<br>RTCCLK<br>HSE/32<br>MC0 | TIM16 | Clock source used as input channel for HSI and LSI calibration |
| CSS<br>CPU (hard fault)<br>COMPx<br>PVD<br>GPIO | TIM1,<br>TIM15, 16, 17 | Timer break |
| GPIO | TIMx | External trigger, timer break |
| | ADCx<br>DAC1 | Conversion external trigger |
| DAC1 | COMPx | Comparator inverting input |

*Note: For more details about the interconnect actions, please refer to the corresponding sections in the reference manual (RM0365.*

## 3.9 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

# 4 Pinouts and pin description

**Figure 4. STM32F302xB/STM32F302xC LQFP48 pinout**

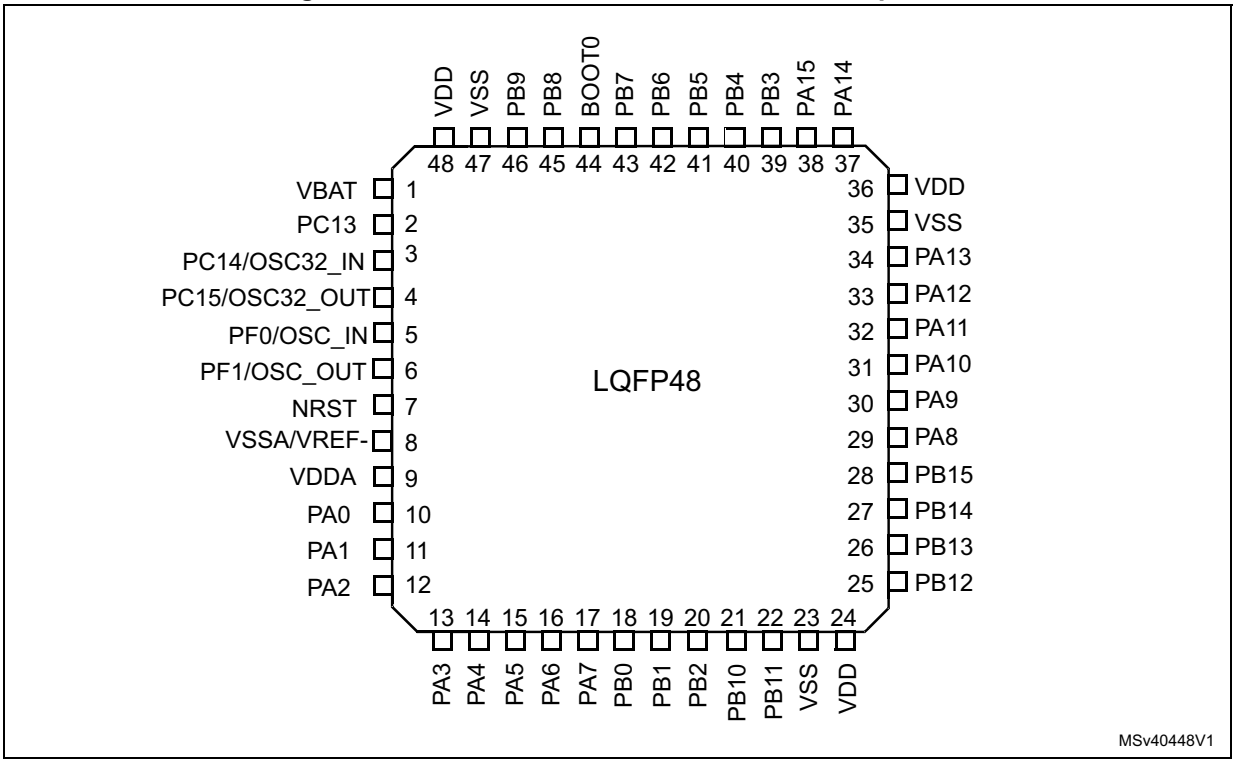


**Figure 6. STM32F302xB/STM32F302xC LQFP100 pinout**

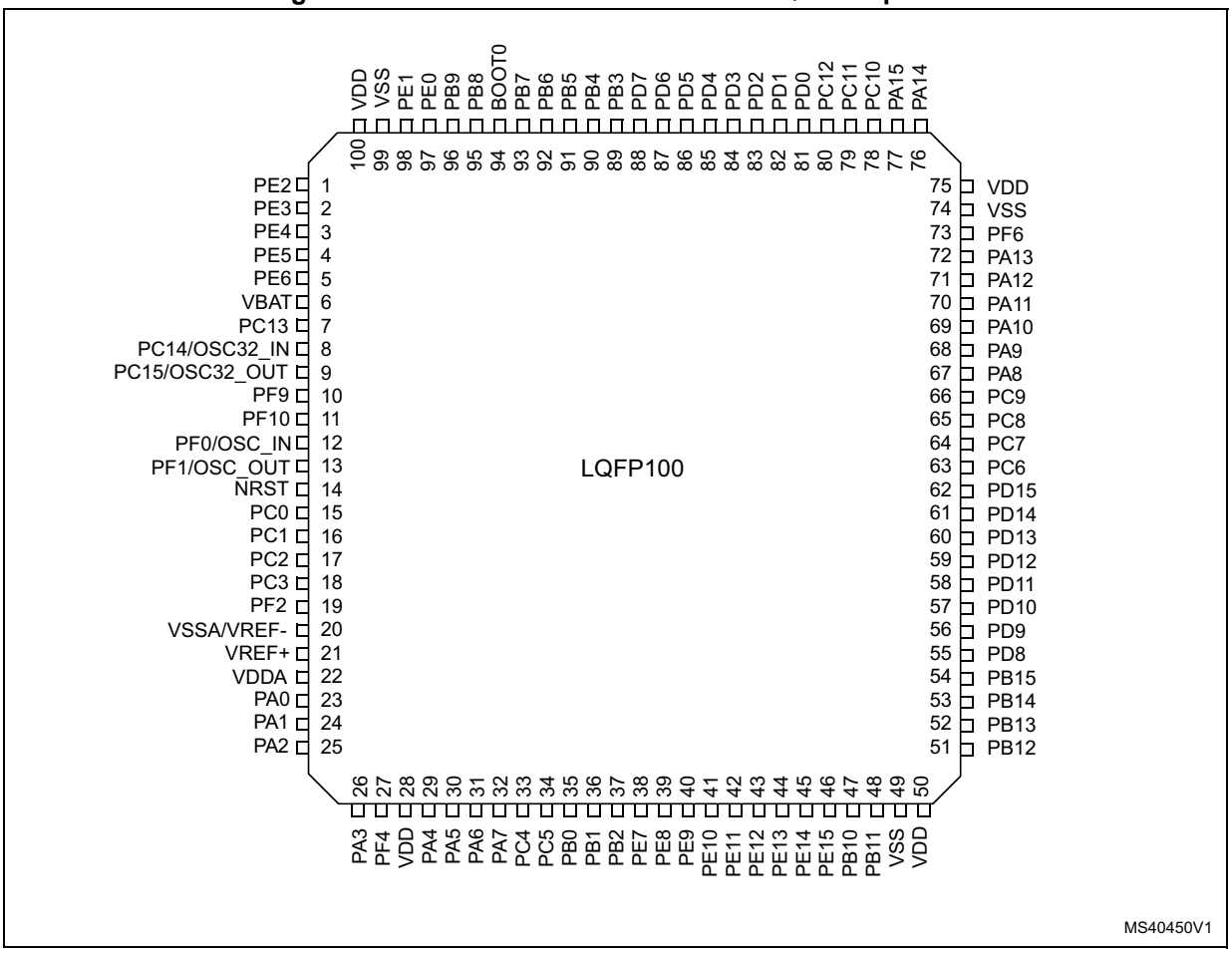


**Table 13. STM32F302xB/STM32F302xC pin definitions (continued)**

| Pin number | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|
| WLCSP100 | LQFP100 | LQFP64 | LQFP48 | | | | | Alternate functions | Additional functions |
| C9 | 7 | 2 | 2 | PC13(2) | I/O | TC | - | TIM1_CH1N | WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT |
| C10 | 8 | 3 | 3 | PC14(2) OSC32_IN (PC14) | I/O | TC | - | - | OSC32_IN |
| D9 | 9 | 4 | 4 | PC15(2) OSC32_ OUT (PC15) | I/O | TC | - | - | OSC32_OUT |
| D10 | 10 | - | - | PF9 | I/O | FT | (1) | TIM15_CH1, SPI2_SCK, EVENTOUT | - |
| E10 | 11 | - | - | PF10 | I/O | FT | (1) | TIM15_CH2, SPI2_SCK, EVENTOUT | - |
| F10 | 12 | 5 | 5 | PF0- OSC_IN (PF0) | I/O | FTf | - | TIM1_CH3N, I2C2_SDA, | OSC_IN |
| F9 | 13 | 6 | 6 | PF1- OSC_OUT (PF1) | I/O | FTf | - | I2C2_SCL | OSC_OUT |
| E9 | 14 | 7 | 7 | NRST | I/O | RST | | Device reset input / internal reset output (active low) | |
| G10 | 15 | 8 | - | PC0 | I/O | TTa | (1) | EVENTOUT | ADC12_IN6 |
| G9 | 16 | 9 | - | PC1 | I/O | TTa | (1) | EVENTOUT | ADC12_IN7 |
| G8 | 17 | 10 | - | PC2 | I/O | TTa | (1) | EVENTOUT | ADC12_IN8 |
| H10 | 18 | 11 | - | PC3 | I/O | TTa | (1) | TIM1_BKIN2, EVENTOUT | ADC12_IN9 |
| E8 | 19 | - | - | PF2 | I/O | TTa | (1) | EVENTOUT | ADC12_IN10 |
| H8 | 20 | 12 | 8 | VSSA/ VREF- | S | - | - | Analog ground/Negative reference voltage | |
| J8 | 21 | - | - | VREF+(3) | S | - | - | Positive reference voltage | |
| J10 | 22 | - | - | VDDA | S | - | - | Analog power supply | |
| - | - | 13 | 9 | VDDA/ VREF+ | S | - | - | Analog power supply/Positive reference voltage | |
| H9 | 23 | 14 | 10 | PA0 | I/O | TTa | (4) | USART2_CTS, TIM2_CH1_ETR, TSC_G1_IO1, COMP1_OUT, EVENTOUT | ADC1_IN1, COMP1_INM, RTC_ TAMP2, WKUP1 |

Table 13. STM32F302xB/STM32F302xC pin definitions (continued)

| Pin number | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|
| WLCSP100 | LQFP100 | LQFP64 | LQFP48 | | | | | Alternate functions | Additional functions |
| J9 | 24 | 15 | 11 | PA1 | I/O | TTa | (4) | USART2_RTS_DE, TIM2_CH2, TSC_G1_IO2, TIM15_CH1N, RTC_REFIN, EVENTOUT | ADC1_IN2, COMP1_INP, OPAMP1_VINP |
| F7 | 25 | 16 | 12 | PA2 | I/O | TTa | (4) (5) | USART2_TX, TIM2_CH3, TIM15_CH1, TSC_G1_IO3, COMP2_OUT, EVENTOUT | ADC1_IN3, COMP2_INM, OPAMP1_VOUT |
| G7 | 26 | 17 | 13 | PA3 | I/O | TTa | (4) | USART2_RX, TIM2_CH4, TIM15_CH2, TSC_G1_IO4, EVENTOUT | ADC1_IN4, OPAMP1_VINP, COMP2_INP, OPAMP1_VINM |
| - | 27 | 18 | - | PF4 | I/O | TTa | **(1)** (4) | COMP1_OUT, EVENTOUT | ADC1_IN5 |
| K9, K10 | - | - | - | VSS | S | - | - | Digital ground | |
| K8 | 28 | 19 | - | VDD | S | **-** | **-** | Digital power supply | |
| J7 | 29 | 20 | 14 | PA4 | I/O | TTa | (4) (5) | SPI1_NSS, SPI3_NSS,I2S3_WS, USART2_CK, TSC_G2_IO1, TIM3_CH2, EVENTOUT | ADC2_IN1, DAC1_OUT1, COMP1_INM, COMP2_INM, COMP4_INM, COMP6_INM |
| H7 | 30 | 21 | 15 | PA5 | I/O | TTa | (4) (5) | SPI1_SCK, TIM2_CH1_ETR, TSC_G2_IO2, EVENTOUT | ADC2_IN2 OPAMP1_VINP, OPAMP2_VINM COMP1_INM, COMP2_INM, COMP4_INM, COMP6_INM |
| H6 | 31 | 22 | 16 | PA6 | I/O | TTa | (4) (5) | SPI1_MISO, TIM3_CH1, TIM1_BKIN, TIM16_CH1, COMP1_OUT, TSC_G2_IO3, EVENTOUT | ADC2_IN3, OPAMP2_VOUT |
| K7 | 32 | 23 | 17 | PA7 | I/O | TTa | (4) | SPI1_MOSI, TIM3_CH2, TIM17_CH1, TIM1_CH1N, , TSC_G2_IO4, COMP2_OUT, EVENTOUT | ADC2_IN4, COMP2_INP, OPAMP2_VINP, OPAMP1_VINP |
| G6 | 33 | 24 | - | PC4 | I/O | TTa | **(1)** (4) | USART1_TX, EVENTOUT | ADC2_IN5 |
| F6 | 34 | 25 | - | PC5 | I/O | TTa | **(1)** | USART1_RX, TSC_G3_IO1, EVENTOUT | ADC2_IN11, OPAMP2_VINM, OPAMP1_VINM |
| J6 | 35 | 26 | 18 | PB0 | I/O | TTa | - | TIM3_CH3, TIM1_CH2N, TSC_G3_IO2, EVENTOUT | COMP4_INP, OPAMP2_VINP |

### 6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 25* are derived from tests performed under the ambient temperature condition summarized in *Table 24*.

**Table 25. Operating conditions at power-up / power-down**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | - | 0 | ∞ | µs/V |
| | $V_{DD}$ fall time rate | | 20 | ∞ | |
| $t_{VDDA}$ | $V_{DDA}$ rise time rate | - | 0 | ∞ | |
| | $V_{DDA}$ fall time rate | | 20 | ∞ | |

### 6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 26* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 24*.

**Table 26. Embedded reset and power control block characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{POR/PDR}$(1) | Power on/power down reset threshold | Falling edge | 1.8(2) | 1.88 | 1.96 | V |
| | | Rising edge | 1.84 | 1.92 | 2.0 | V |
| $V_{PDRhyst}$(1) | PDR hysteresis | - | - | 40 | - | mV |
| $t_{RSTTEMPO}$(3) | POR reset temporization | - | 1.5 | 2.5 | 4.5 | ms |

1. The PDR detector monitors $V_{DD}$ and also $V_{DDA}$ (if kept enabled in the option bytes). The POR detector monitors only $V_{DD}$.
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
3. Guaranteed by design.

### 6.3.4 Embedded reference voltage

The parameters given in *Table 28* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 24*.

**Table 28. Embedded internal reference voltage**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT}$ | Internal reference voltage | –40 °C < $T_A$ < +105 °C | 1.2 | 1.23 | 1.25 | V |
| | | –40 °C < $T_A$ < +85 °C | 1.2 | 1.23 | 1.24(1) | V |
| $T_{S\_vrefint}$ | ADC sampling time when reading the internal reference voltage | - | 2.2 | - | - | µs |
| $V_{RERINT}$ | Internal reference voltage spread over the temperature range | $V_{DD}$ = 3 V ±10 mV | - | - | 10(2) | mV |
| $T_{Coeff}$ | Temperature coefficient | - | - | - | 100(2) | ppm/°C |

1. Guaranteed by characterization results.
2. Guaranteed by design.

**Table 29. Internal reference voltage calibration values**

| Calibration value name | Description | Memory address |
|---|---|---|
| $V_{REFINT\_CAL}$ | Raw data acquired at temperature of 30 °C $V_{DDA}$= 3.3 V | 0x1FFF F7BA - 0x1FFF F7BB |

### 6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 12: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

#### Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the $f_{HCLK}$ frequency (0 wait state from 0 to 24 MHz,1 wait state from 24 to 48 MHz and 2 wait states from 48 to 72 MHz)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK2} = f_{HCLK}$ and $f_{PCLK1} = f_{HCLK/2}$
- When $f_{HCLK}$ > 8 MHz, the PLL is ON and the PLL input is equal to HSI/2 (4 MHz) or HSE (8 MHz) in bypass mode.

### I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

**I/O static current consumption**

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 54: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

**Caution:** Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

**I/O dynamic current consumption**

In addition to the internal peripheral current consumption (see *Table 38: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

$I_{SW}$ is the current sunk by a switching I/O to charge/discharge the capacitive load

$V_{DD}$ is the MCU supply voltage

$f_{SW}$ is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

### High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 42*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 42. HSE oscillator characteristics**

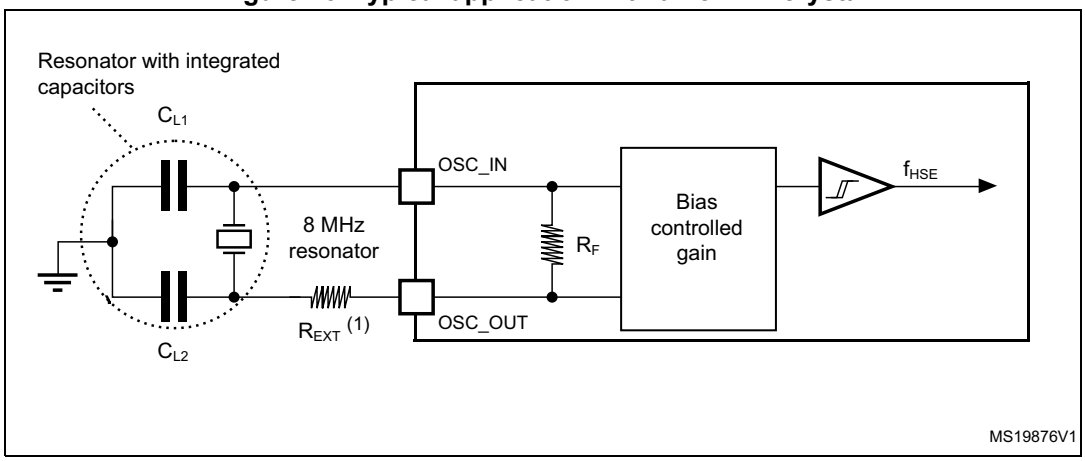
| Symbol | Parameter | Conditions(1) | Min(2) | Typ | Max(2) | Unit |
|---|---|---|---|---|---|---|
| $f_{OSC\_IN}$ | Oscillator frequency | - | 4 | 8 | 32 | MHz |
| $R_F$ | Feedback resistor | - | - | 200 | | kΩ |
| $I_{DD}$ | HSE current consumption | During startup(3) | - | - | 8.5 | mA |
| | | $V_{DD}$=3.3 V, Rm= 30Ω, CL=10 pF@8 MHz | - | 0.4 | - | |
| | | $V_{DD}$=3.3 V, Rm= 45Ω, CL=10 pF@8 MHz | - | 0.5 | - | |
| | | $V_{DD}$=3.3 V, Rm= 30Ω, CL=5 pF@32 MHz | - | 0.8 | - | |
| | | $V_{DD}$=3.3 V, Rm= 30Ω, CL=10 pF@32 MHz | - | 1 | - | |
| | | $V_{DD}$=3.3 V, Rm= 30Ω, CL=20 pF@32 MHz | - | 1.5 | - | |
| $g_m$ | Oscillator transconductance | Startup | 10 | - | - | mA/V |
| $t_{SU(HSE)}$(4) | Startup time | $V_{DD}$ is stabilized | - | 2 | - | ms |

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For $C_{L1}$ and $C_{L2}$, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 16*). $C_{L1}$ and $C_{L2}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of $C_{L1}$ and $C_{L2}$. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing $C_{L1}$ and $C_{L2}$.

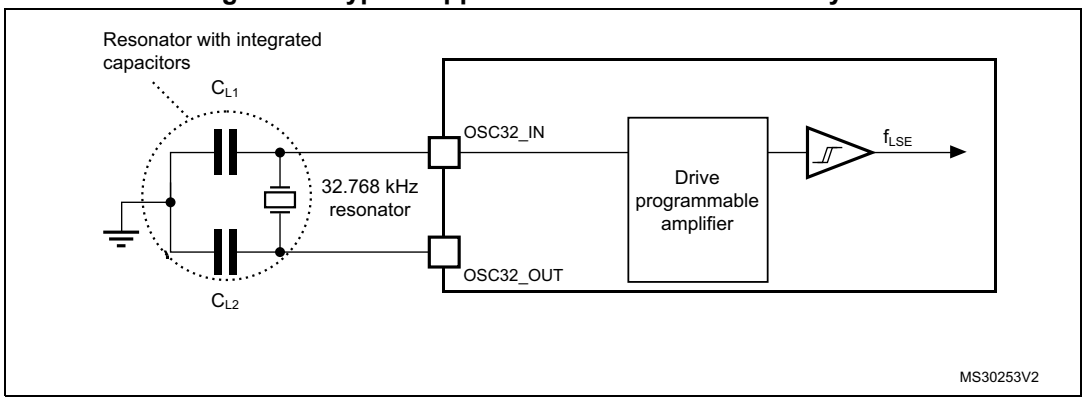
*Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.*

**Figure 16. Typical application with an 8 MHz crystal**




1. $R_{EXT}$ value depends on the crystal characteristics.

**Figure 17. Typical application with a 32.768 kHz crystal**




*Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.*

## 6.3.8 Internal clock source characteristics

The parameters given in *Table 44* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 24*.

### High-speed internal (HSI) RC oscillator

**Table 44. HSI oscillator characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI}$ | Frequency | - | - | 8 | - | MHz |
| TRIM | HSI user trimming step | - | - | - | 1(2) | % |
| $DuCy_{(HSI)}$ | Duty cycle | - | 45(2) | - | 55(2) | % |
| $ACC_{HSI}$ | Accuracy of the HSI oscillator | $T_A$ = -40 to 105°C | -2.8(3) | - | 3.8(3) | % |
| | | $T_A$ = -10 to 85°C | -1.9(3) | - | 2.3(3) | |
| | | $T_A$ = 0 to 85°C | -1.9(3) | - | 2(3) | |
| | | $T_A$ = 0 to 70°C | -1.3(3) | - | 2(3) | |
| | | $T_A$ = 0 to 55°C | -1(3) | - | 2(3) | |
| | | $T_A$ = 25°C(4) | -1 | - | 1 | |
| $t_{su(HSI)}$ | HSI oscillator startup time | - | 1(2) | - | 2(2) | µs |
| $I_{DDA(HSI)}$ | HSI oscillator power consumption | - | - | 80 | 100(2) | µA |

1. $V_{DDA}$ = 3.3 V, $T_A$ = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Factory calibrated, parts not soldered.

### Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

### Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

**Table 50. EMI characteristics**

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. [$f_{HSE}/f_{HCLK}$] | Unit |
|---|---|---|---|---|---|
| | | | | 8/72 MHz | |
| $S_{EMI}$ | Peak level | $V_{DD}$ = 3.6 V, $T_A$ = 25 °C, LQFP100 package compliant with IEC 61967-2 | 0.1 to 30 MHz | **7** | dBµV |
| | | | 30 to 130 MHz | **20** | |
| | | | 130 MHz to 1GHz | **27** | |
| | | | SAE EMI Level | **4** | - |

## 6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114, ANSI/ESD STM5.3.1 standard.

**Table 51. ESD absolute maximum ratings**

| Symbol | Ratings | Conditions | | Class | Maximum value(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$ = +25 °C, conforming to JESD22-A114 | | 2 | 2000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$ = +25 °C, conforming to ANSI/ESD STM5.3.1 | WLCSP100 package | 3 | 250 | |
| | | | Packages except WLCSP100 | 4 | 500 | |

1. Guaranteed by characterization results.

### Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed $V_{OL}/V_{OH}$).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $\Sigma I_{VDD}$ (see *Table 22*).
- The sum of the currents sunk by all the I/Os on $V_{SS}$ plus the maximum Run consumption of the MCU sunk on $V_{SS}$ cannot exceed the absolute maximum rating $\Sigma I_{VSS}$ (see *Table 22*).

### Output voltage levels

Unless otherwise specified, the parameters given in *Table 55* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 24*. All I/Os (FT, TTa and TC unless otherwise specified) are CMOS and TTL compliant.

**Table 55. Output voltage characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$(1) | Output low level voltage for an I/O pin | CMOS port(2) $I_{IO}$ = +8 mA 2.7 V < $V_{DD}$ < 3.6 V | - | 0.4 | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin | | $V_{DD}$–0.4 | - | |
| $V_{OL}$ (1) | Output low level voltage for an I/O pin | TTL port(2) $I_{IO}$ = +8 mA 2.7 V < $V_{DD}$ < 3.6 V | - | 0.4 | |
| $V_{OH}$ (3) | Output high level voltage for an I/O pin | | 2.4 | - | |
| $V_{OL}$(1)(4) | Output low level voltage for an I/O pin | $I_{IO}$ = +20 mA 2.7 V < $V_{DD}$ < 3.6 V | - | 1.3 | |
| $V_{OH}$(3)(4) | Output high level voltage for an I/O pin | | $V_{DD}$–1.3 | - | |
| $V_{OL}$(1)(4) | Output low level voltage for an I/O pin | $I_{IO}$ = +6 mA 2 V < $V_{DD}$ < 2.7 V | - | 0.4 | |
| $V_{OH}$(3)(4) | Output high level voltage for an I/O pin | | $V_{DD}$–0.4 | - | |
| $V_{OLFM+}$(1)(4) | Output low level voltage for an FTf I/O pin in FM+ mode | $I_{IO}$ = +20 mA 2.7 V < $V_{DD}$ < 3.6 V | - | 0.4 | |

1. The $I_{IO}$ current sunk by the device must always respect the absolute maximum rating specified in *Table 22* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $\Sigma I_{IO(PIN)}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The $I_{IO}$ current sourced by the device must always respect the absolute maximum rating specified in *Table 22* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $\Sigma I_{IO(PIN)}$.
4. Data based on design simulation.

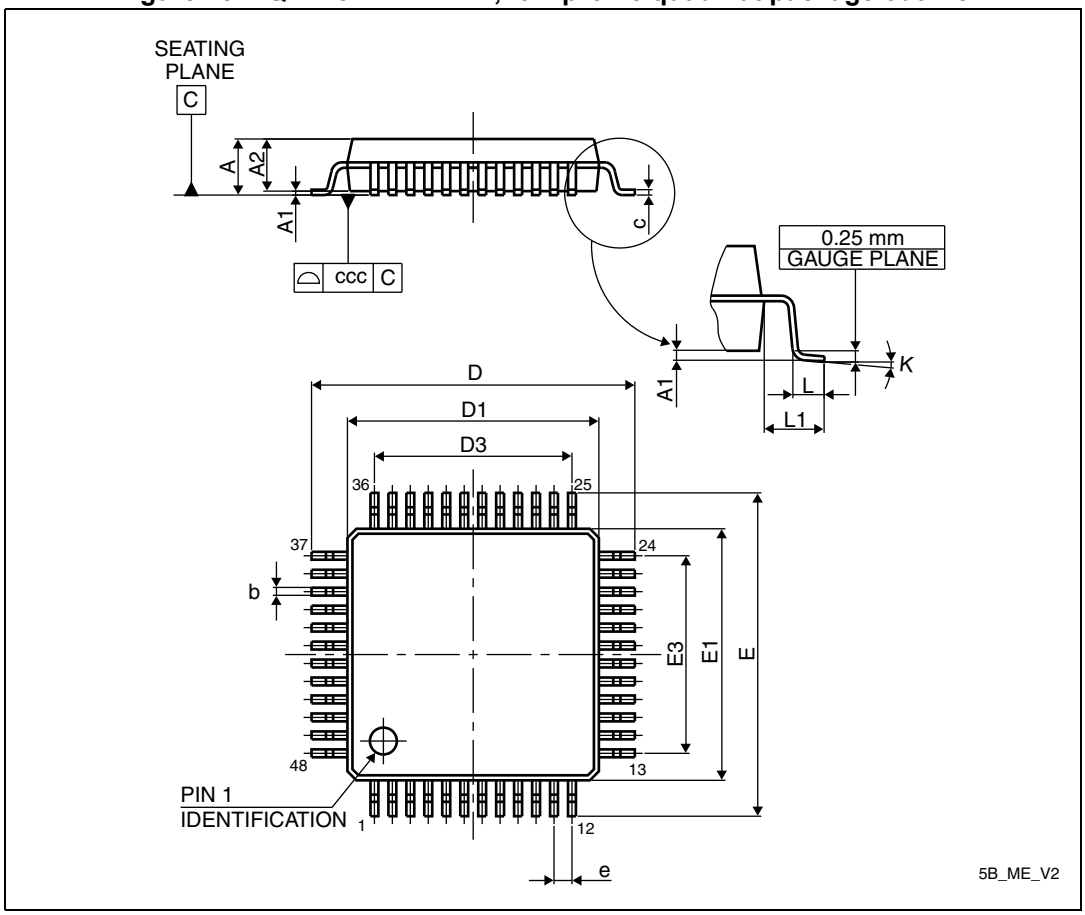
### 6.3.21 Operational amplifier characteristics

**Table 77. Operational amplifier characteristics(1)**

| Symbol | Parameter | | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | | - | 2.4 | - | 3.6 | V |
| CMIR | Common mode input range | | - | 0 | - | $V_{DDA}$ | V |
| $VI_{OFFSET}$ | Input offset voltage | Maximum calibration range | 25°C, No Load on output. | - | - | 4 | mV |
| | | | All voltage/Temp. | - | - | 6 | |
| | | After offset calibration | 25°C, No Load on output. | - | - | 1.6 | |
| | | | All voltage/Temp. | - | - | 3 | |
| $\Delta VI_{OFFSET}$ | Input offset voltage drift | | - | - | 5 | - | µV/°C |
| $I_{LOAD}$ | Drive current | | - | - | - | 500 | µA |
| IDDOPAMP | Consumption | | No load, quiescent mode | - | 690 | 1450 | µA |
| TS_OPAMP_VOUT | ADC sampling time when reading the OPAMP output. | | - | 400 | - | - | ns |
| CMRR | Common mode rejection ratio | | - | - | 90 | - | dB |
| PSRR | Power supply rejection ratio | | DC | 73 | 117 | - | dB |
| GBW | Bandwidth | | - | - | 8.2 | - | MHz |
| SR | Slew rate | | - | - | 4.7 | - | V/µs |
| $R_{LOAD}$ | Resistive load | | - | 4 | - | - | kΩ |
| $C_{LOAD}$ | Capacitive load | | - | - | - | 50 | pF |
| $VOH_{SAT}$ | High saturation voltage(2) | | $R_{load}$ = min, Input at $V_{DDA}$. | $V_{DDA}$ -100 | - | - | mV |
| | | | $R_{load}$ = 20K, Input at $V_{DDA}$. | $V_{DDA}$ -20 | - | - | |
| $VOL_{SAT}$ | High saturation voltage(2) | | Rload = min, input at 0V | - | - | 100 | |
| | | | Rload = 20K, input at 0V. | - | - | 20 | |
| φm | Phase margin | | - | - | 62 | - | ° |
| $t_{OFFTRIM}$ | Offset trim time: during calibration, minimum time needed between two steps to have 1 mV accuracy | | - | - | - | 2 | ms |
| $t_{WAKEUP}$ | Wake up time from OFF state. | | $C_{LOAD}$ ≤50 pf, $R_{LOAD}$ ≥ 4 kΩ, Follower configuration | - | 2.8 | 5 | µs |

## 7.3 LQFP48 – 7 x 7 mm, low-profile quad flat package information

**Figure 45. LQFP48 – 7 x 7 mm, low-profile quad flat package outline**




1. Drawing is not to scale.

**Table 83. LQFP48 – 7 x 7 mm, low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.60 | - | - | 0.0630 |
| A1 | 0.05 | - | 0.15 | 0.0020 | - | 0.0059 |
| A2 | 1.35 | 1.40 | 1.45 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.17 | 0.22 | 0.27 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.09 | - | 0.20 | 0.0035 | - | 0.0079 |
| D | 8.80 | 9.00 | 9.20 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.80 | 7.00 | 7.20 | 0.2677 | 0.2756 | 0.2835 |
| D3 | - | 5.50 | - | - | 0.2165 | - |
| E | 8.80 | 9.00 | 9.20 | 0.3465 | 0.3543 | 0.3622 |

# 8 Ordering information

**Table 87. Ordering information scheme**

Example: STM32 F 302 R B T 6 xxx

**Device family**

STM32 = ARM-based 32-bit microcontroller

**Product type**

F = general-purpose

**Device subfamily**

302 = STM32F302xx

**Pin count**

C = 48 pins
R = 64 pins
V = 100 pins

**Flash memory size**

B = 128 Kbytes of Flash memory
C = 256 Kbytes of Flash memory

**Package**

T = LQFP
Y = WLCSP

**Temperature range**

6 = Industrial temperature range, –40 to 85 °C
7 = Industrial temperature range, –40 to 105 °C

**Options**

xxx = programmed parts
TR = tape and reel

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

**Table 88. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 29-Jan-2015 | 4 | Updated cover page with ADC up to 17 channels.<br>Updated *Section 6.3.20: Comparator characteristics* modifying ts_sc characteristics in *Table 76* and adding *Figure 37: Maximum VREFINT scaler startup time from power down*.<br>Updated $I_{DD}$ data in *Table 42: HSE oscillator characteristics*. |
| 17-Apr-2015 | 5 | Updated *Figure 1: STM32F302xB/STM32F302xC block diagram* changing 32 KB of SRAM by 40 KB of SRAM.<br>Updated *Section 7: Package information*: with new package information structure adding 1 sub paragraph for each package.<br>Updated *Figure 41: LQFP100 – 14 x 14 mm, low-profile quad flat package top view example* removing gate mark.<br>Added note for all package device markings: “the following figure gives an example of topside marking orientation versus pin 1 identifier location”.<br>Updated *Table 82: LQFP64 – 10 x 10 mm, low-profile quad flat package mechanical data*.<br>Updated *Table 7: STM32F302xB/STM32F302xC peripheral interconnect matrix* removing TIM8 reference and updating note below the table, replacing by a reference to RM0365. |
| 22-Feb-2016 | 6 | Added WLCSP100:<br>– Updated cover page.<br>– Updated *Table 2: STM32F302xx family device features and peripheral counts*.<br>– Added *Figure 7: STM32F302xB/STM32F302xC WLCSP100 pinout*.<br>– Updated *Table 13: STM32F302xB/STM32F302xC pin definitions*.<br>– Updated *Table 24: General operating conditions*.<br>– Added *Section 7.4: WLCSP100 - 0.4 mm pitch wafer level chip scale package information*.<br>– Updated *Table 86: Package thermal characteristics*.<br>– Updated *Table 87: Ordering information scheme*.<br>Updated *Figure 4*, *Figure 5*, *Figure 6*, *Table 13* and *Table 22* removing all VDD and VSS indexes.<br>Updated all the notes removing ‘not tested in production’.<br>Updated *Table 68: ADC characteristics* adding $V_{REF}$- negative voltage reference.<br>Updated *Table 21: Voltage characteristics* adding table note 4.<br>Updated *Table 43: LSE oscillator characteristics (fLSE = 32.768 kHz)* LSEDRV[1:0] bits.<br>Updated *Table 28: Embedded internal reference voltage* $V_{REFINT}$ internal reference voltage (min and typ values).<br>Updated *Table 51: ESD absolute maximum ratings* ESD CDM at class 3 and 4 including WLCSP100 package information. |