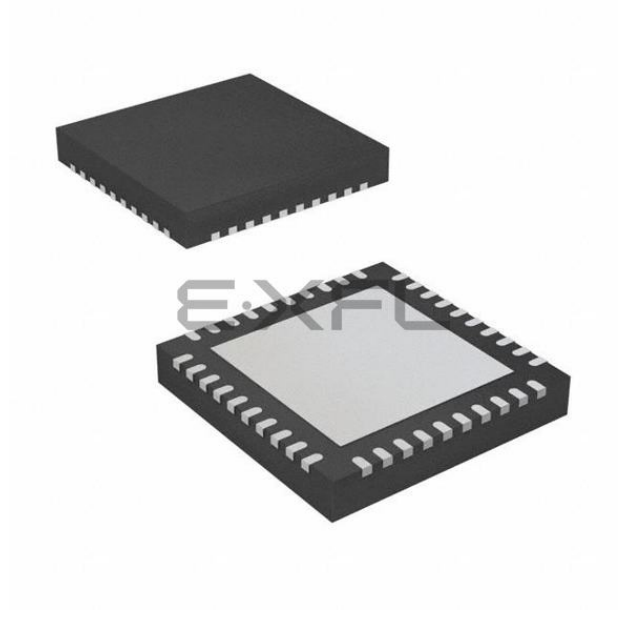

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	28
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 20x10/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/sim3l134-c-gm

Table 3.5. On-Chip Regulators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC-DC Buck Converter						
Input Voltage Range	V_{DCIN}		1.8	—	3.8	V
Input Supply to Output Voltage Differential (for regulation)	V_{DCREG}		0.45	—	—	V
Output Voltage Range	V_{DCOUT}		1.25	—	3.8	V
Output Voltage Accuracy	V_{DCACC}		—	±25	—	mV
Output Current	I_{DCOUT}		—	—	90	mA
Inductor Value[1]	L_{DC}		0.47	0.56	0.68	µH
Inductor Current Rating	I_{LDC}	I_{load} < 50 mA	450	—	—	mA
		I_{load} > 50 mA	550	—	—	mA
Output Capacitor Value	C_{DCOUT}		1	2.2	10	µF
Input Capacitor Value[2]	C_{DCIN}		—	4.7	—	µF
Load Regulation	R_{load}		—	0.03	—	mV/mA
Maximum DC Load Current During Startup	I_{DCMAX}		—	—	5	mA
Switching Clock Frequency	F_{DCCLK}		1.9	2.9	3.8	MHz
Local Oscillator Frequency	F_{DCOSC}		2.4	2.9	3.4	MHz
LDO Regulators						
Input Voltage Range[3]	V_{LDOIN}	Sourced from VBAT	1.8	—	3.8	V
		Sourced from VDC	1.9	—	3.8	V
Output Voltage Range[4]	V_{LDO}		0.8	—	1.9	V
LDO Output Voltage Accuracy	V_{LDOACC}		—	±25	—	mV
Output Settings in PM8 (All LDOs)	V_{LDO}	1.8 V ≤ V_{BAT} ≤ 2.9 V	1.5			V
		1.95 V ≤ V_{BAT} ≤ 3.5 V	1.8			V
		2.0 V ≤ V_{BAT} ≤ 3.8 V	1.9			V

Notes:

1. See reference manual for recommended inductors.
2. Recommended: X7R or X5R ceramic capacitors with low ESR. Example: Murata GRM21BR71C225K with ESR < 10 mΩ (@ frequency > 1 MHz).
3. Input voltage specification accounts for the internal LDO dropout voltage under the maximum load condition to ensure that the LDO output voltage will remain at a valid level as long as V_{LDOIN} is at or above the specified minimum.
4. The memory LDO output should always be set equal to or lower than the output of the analog LDO. When lowering both LDOs (for example to go into PM8 under low supply conditions), first adjust the memory LDO and then the analog LDO. When raising the output of both LDOs, adjust the analog LDO before adjusting the memory LDO.
5. Output range represents the programmable output range, and does not reflect the minimum voltage under all conditions. Dropout when the input supply is close to the output setting is normal, and accounted for.
6. Analog peripheral specifications assume a 1.8 V output on the analog LDO.

Table 3.5. On-Chip Regulators (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Memory LDO Output Setting[5]	V_{LDOMEM}	During Programming	1.8	—	1.9	V
		During Normal Operation	1.5	—	1.9	V
Digital LDO Output Setting	V_{LDODIG}	$F_{AHB} \leq 20$ MHz	1.0	—	1.9	V
		$F_{AHB} > 20$ MHz	1.2	—	1.9	V
Analog LDO Output Setting During Normal Operation[6]	V_{LDOANA}		1.8			V

Notes:

1. See reference manual for recommended inductors.
2. Recommended: X7R or X5R ceramic capacitors with low ESR. Example: Murata GRM21BR71C225K with ESR < 10 mΩ (@ frequency > 1 MHz).
3. Input voltage specification accounts for the internal LDO dropout voltage under the maximum load condition to ensure that the LDO output voltage will remain at a valid level as long as V_{LDOIN} is at or above the specified minimum.
4. The memory LDO output should always be set equal to or lower than the output of the analog LDO. When lowering both LDOs (for example to go into PM8 under low supply conditions), first adjust the memory LDO and then the analog LDO. When raising the output of both LDOs, adjust the analog LDO before adjusting the memory LDO.
5. Output range represents the programmable output range, and does not reflect the minimum voltage under all conditions. Dropout when the input supply is close to the output setting is normal, and accounted for.
6. Analog peripheral specifications assume a 1.8 V output on the analog LDO.

Table 3.6. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Write Time[1]	t_{WRITE}	One 16-bit Half Word	20	21	22	µs
Erase Time[1]	t_{ERASE}	One Page	20	21	22	ms
	t_{ERALL}	Full Device	20	21	22	ms
Endurance (Write/Erase Cycles)	N_{WE}		20k	100k	—	Cycles
Retention[2]	t_{RET}	T_A = 25 °C, 1k Cycles	10	100	—	Years

Notes:
1. Does not include sequencing time before and after the write/erase operation, which may take up to 35 µs. During sequential write operations, this extra time is only taken prior to the first write and after the last write.
2. Additional Data Retention Information is published in the Quarterly Quality and Reliability Report.

Table 3.9. SAR ADC (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset Temperature Coefficient	TC_{OFF}		—	0.004	—	LSB/°C
Slope Error	E_M		–0.07	–0.02	0.02	%
Dynamic Performance (10 kHz Sine Wave Input 1dB below full scale, Max throughput)						
Signal-to-Noise	SNR	12 Bit Mode	62	66	—	dB
		10 Bit Mode	58	60	—	dB
Signal-to-Noise Plus Distortion	SNDR	12 Bit Mode	62	66	—	dB
		10 Bit Mode	58	60	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD	12 Bit Mode	—	78	—	dB
		10 Bit Mode	—	77	—	dB
Spurious-Free Dynamic Range	SFDR	12 Bit Mode	—	–79	—	dB
		10 Bit Mode	—	–74	—	dB
***Note:** Absolute input pin voltage is limited by the lower of the supply at VBAT and VIO.						

Table 3.16. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (PB0, PB1, PB3, or PB4)	V_{OH}	Low Drive, I_{OH} = –1 mA	V_{IO} – 0.7	—	—	V
		Low Drive, I_{OH} = –10 µA	V_{IO} – 0.1	—	—	V
		High Drive, I_{OH} = –3 mA	V_{IO} – 0.7	—	—	V
		High Drive, I_{OH} = –10 µA	V_{IO} – 0.1	—	—	V
Output High Voltage (PB2)	V_{OH}	Low Drive, I_{OH} = –1 mA	V_{IORF} – 0.7	—	—	V
		Low Drive, I_{OH} = –10 µA	V_{IORF} – 0.1	—	—	V
		High Drive, I_{OH} = –3 mA	V_{IORF} – 0.7	—	—	V
		High Drive, I_{OH} = –10 µA	V_{IORF} – 0.1	—	—	V
Output Low Voltage (any Port I/O pin or $\overline{\text{RESET}}$[1])	V_{OL}	Low Drive, I_{OL} = 1.4 mA	—	—	0.6	V
		Low Drive, I_{OL} = 10 µA	—	—	0.1	V
		High Drive, I_{OL} = 8.5 mA	—	—	0.6	V
		High Drive, I_{OL} = 10 µA	—	—	0.1	V
Input High Voltage (PB0, PB1, PB3, PB4 or $\overline{\text{RESET}}$)	V_{IH}		V_{IO} – 0.6	—	—	V
Input High Voltage (PB2)	V_{IH}		V_{IORF} – 0.6	—	—	V
Input Low Voltage any Port I/O pin or $\overline{\text{RESET}}$)	V_{IL}		—	—	0.6	V
Weak Pull-Up Current[2] (per pin)	I_{PU}	V_{IO} or V_{IORF} = 1.8	-6	-3.5	-2	µA
		V_{IO} or V_{IORF} = 3.8	-32	-20	-10	µA
Input Leakage (Pullups off or Analog)	I_{LK}	$0 \le V_{IN} \le V_{IO}$ or V_{IORF}	-1	—	1	µA

Notes:

1. Specifications for $\overline{\text{RESET}}$ V_{OL} adhere to the low drive setting.
2. On the SiM3L1x6 and SiM3L1x4 devices, the SWV pin will have double the weak pull-up current specified whenever the device is held in reset.

4. Precision32™ SiM3L1xx System Overview

The SiM3L1xx Precision32™ devices are fully integrated, mixed-signal system-on-a-chip MCUs. Highlighted features are listed below. Refer to Table 5.1 for specific product feature selection and part ordering numbers.

- **Core:**
  - 32-bit ARM Cortex-M3 CPU.
  - 50 MHz maximum operating frequency.
  - Branch target cache and prefetch buffers to minimize wait states.
- **Memory:** 32–256 kB flash; in-system programmable, 8–32 kB SRAM configurable to retention mode in 4 kB blocks. Blocks configured to retention mode preserve state in the low power PM8 mode.
- **Power:**
  - Three adjustable low drop-out (LDO) regulators.
  - DC-DC buck converter allows dynamic voltage scaling for maximum efficiency (250 mW output).
  - Power-on reset circuit and brownout detectors.
  - Power Management Unit (PMU).
  - Specialized charge pump reduces power consumption in low power modes.
  - Process/Voltage/Temperature (PVT) Monitor.
  - Register state retention in lowest power mode.
- **I/O:** Up to 62 contiguous 5 V tolerant I/O pins and one flexible peripheral crossbar.
- **Clock Sources:**
  - Internal oscillator with PLL: 23–50 MHz with ± 1.5% accuracy in free-running mode.
  - Low-power internal oscillator: 20 MHz.
  - Low-frequency internal oscillator: 16.4 kHz.
  - External RTC crystal oscillator: 32.768 kHz.
  - External oscillator: Crystal, RC, C, CMOS clock.
- **Integrated LCD Controller (4x40).**
- **Data Peripherals:**
  - 10-Channel DMA Controller.
  - 3 x Data Transfer Managers.
  - 128/192/256-bit Hardware AES Encryption.
  - CRC with programmable 16-bit polynomial, one 32-bit polynomial, and bus snooping capability.
  - Encoder / Decoder.
- **Timers/Counters:**
  - 3 x 32-bit Timers.
  - 1 x Enhanced Programmable Counter Array (EPCA).
  - Real Time Clock (RTC0).
  - Low Power Timer.
  - Watchdog Timer.
  - Low Power Mode Advanced Capture Counter (ACCTR).
- **Communications Peripherals:**
  - 1 x USART with IrDA and ISO7816 SmartCard support.
  - 1 x UART that operates in low power mode (PM8).
  - 2 x SPIs.
  - 1 x I2C.
- **Analog:**
  - 1 x 12-Bit Analog-to-Digital Converter (SARADC).
  - 1 x 10-Bit Digital-to-Analog Converter (IDAC).
  - 2 x Low-Current Comparators (CMP).
- **On-Chip Debugging**

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillators, the SiM3L1xx devices are truly stand-alone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing non-volatile data storage and allowing field upgrades of the firmware. User firmware has complete control of all

- Supports synchronizing the regulator switching with the system clock.
- Automatically limits the peak inductor current if the load current rises beyond a safe limit.
- Automatically goes into bypass mode if the battery voltage cannot provide sufficient headroom.
- Sources current, but cannot sink current.

4.1.2. Three Low Dropout LDO Regulators (LDO0)

The SiM3L1xx devices include one LDO0 module with three low dropout regulators. Each of these regulators have independent switches to select the battery voltage or the output of the dc-dc converter as the input to each LDO, and an adjustable output voltage.

The LDOs consume little power and provide flexibility in choosing a power supply for the system. Each regulator can be independently adjusted between 0.8 and 1.9 V output.

4.1.3. Voltage Supply Monitor (VMON0)

The SiM3L1xx devices include a voltage supply monitor that can monitor the main supply voltage. This module includes the following features:

- Main supply “VBAT Low” (VBAT below the early warning threshold) notification.
- Holds the device in reset if the main VBAT supply drops below the VBAT Reset threshold.

The voltage supply monitor allows devices to function in known, safe operating conditions without the need for external hardware.

4.1.4. Power Management Unit (PMU)

The Power Management Unit on the SiM3L1xx manages the power systems of the device. It manages the power-up sequence during power on and the wake up sources for PM8. On power-up, the PMU ensures the core voltages are a proper value before core instruction execution begins.

The VDRV pin powers external circuitry from either the VBAT battery input voltage or the output of the dc-dc converter on VDC. The PMU includes an internal switch to select one of these sources for the VDRV pin.

The PMU has a specialized VBAT-divided-by-2 charge pump that can power some internal modules while in PM8 to save power.

The PMU module includes the following features:

- Provides the enable or disable for the analog power system, including the three LDO regulators.
- Up to 14 pin wake inputs can wake the device from Power Mode 8.
- The Low Power Timer, RTC0 (alarms and oscillator failure), Comparator 0, Advanced Capture Counter, LCD0 VBAT monitor, UART0, low power mode charge pump failure, and the RESET pin can also serve as wake sources for Power Mode 8.
- Controls which 4 kB RAM blocks are retained while in Power Mode 8.
- Provides a PMU_Asleep signal to a pin as an indicator that the device is in PM8.
- Specialized charge pump to reduce power consumption in PM8.

Provides control for the internal switch between VBAT and VDC to power the VDRV pin for external circuitry.

4.1.5. Device Power Modes

The SiM3L1xx devices feature seven low power modes in addition to normal operating mode. Several peripherals provide wake up sources for these low power modes, including the Low Power Timer (LPTIMER0), RTC0 (alarms and oscillator failure notification), Comparator 0 (CMP0), Advanced Capture Counter (ACCTR0), LCD VBAT monitor (LCD0), UART0, low power mode charge pump failure, and PMU Pin Wake.

In addition, all peripherals can have their clocks disabled to reduce power consumption whenever a peripheral is not being used using the clock control (CLKCTRL) registers.

4.1.5.1. Normal Mode (Power Mode 0) and Power Mode 4

Normal Mode and Power Mode 4 are fully operational modes with code executing from flash memory. PM4 is the same as Normal Mode, but with the clocks operating at a lower speed. This enables power to be conserved by reducing the LDO regulator outputs.

4.1.6. Process/Voltage/Temperature Monitor (TIMER2 and PVTOSC0)

The Process/Voltage/Temperature monitor consists of two modules (TIMER2 and PVTOSC0) designed to monitor the digital circuit performance of the SiM3L1xx device.

The PVT oscillator (PVTOSC0) consists of two oscillators, one operating from the memory LDO and one operating from the digital LDO. These oscillators have two independent speed options and provide the clocks for two 16-bit timers in the TIMER2 module using the EX input. By monitoring the resulting counts of the TIMER2 timers, firmware can monitor the current device performance and increase the scalable LDO regulator (LDO0) output voltages as needed or decrease the output voltages to save power.

The PVT monitor has the following features:

- Two separate oscillators and timers for the memory and digital logic voltage domains.
- Two oscillator output divider settings.
- Provides a method for monitoring digital performance to allow firmware to adjust the scalable LDO regulator output voltages to the lowest level possible, saving power.

4.5. Data Peripherals

4.5.1. 10-Channel DMA Controller

The DMA facilitates autonomous peripheral operation, allowing the core to finish tasks more quickly without spending time polling or waiting for peripherals to interrupt. This helps reduce the overall power consumption of the system, as the device can spend more time in low-power modes.

The DMA controller has the following features:

- Utilizes ARM PrimeCell uDMA architecture.
- Implements 10 channels.
- DMA crossbar supports DTM0, DTM1, DTM2, SARADC0, IDAC0, I2C0, SPI0, SPI1, USART0, AES0, ENCDEC0, EPCA0, external pin triggers, and timers.
- Supports primary, alternate, and scatter-gather data structures to implement various types of transfers.
- Access allowed to all AHB and APB memory space.

4.5.2. Data Transfer Managers (DTM0, DTM1, DTM2)

The Data Transfer Manager is a module that collects DMA request signals from various peripherals and generates a series of master DMA requests based on a state-driven configuration. This master request drives a set of DMA channels to perform functions such as assembling and transferring communication packets to external devices. This capability saves power by allowing the core to remain in a low power mode during complex transfer operations. A combination of simple and peripheral scatter-gather DMA configurations can be used to perform complex operations while reducing memory requirements.

The DTM acts as a side channel for the peripheral's DMA control signals. When active, it manages the DMA control signals for the peripherals. When the DTMn module is inactive, the peripherals communicate directly to the DMA module.

The DTMn module has the following features:

- State descriptions stored in RAM with up to 15 states supported per module.
- Supports up to 15 source peripherals and up to 15 destination peripherals per module, in addition to memory or peripherals that do not require a data request.
- Includes error detection and an optional transfer timeout.
- Includes notifications for state transitions.

4.5.3. 128/192/256-bit Hardware AES Encryption (AES0)

The basic AES block cipher is implemented in hardware. The integrated hardware support for Cipher Block Chaining (CBC) and Counter (CTR) algorithms results in identical performance, memory bandwidth, and memory footprint between the most basic Electronic Codebook (ECB) algorithm and these more complex algorithms. This hardware accelerator translates to more core bandwidth available for other functions or a power savings for low-power applications.

The AES module includes the following features:

- Operates on 4-word (16-byte) blocks.
- Supports key sizes of 128, 192, and 256 bits for both encryption and decryption.
- Generates the round key for decryption operations.
- All cipher operations can be performed without any firmware intervention for multiple 4-word blocks (up to 32 kB).
- Support for various chained and stream-ciphering configurations with XOR paths on both the input and output.
- Internal 4-word FIFOs to facilitate DMA operations.
- Integrated key storage.
- Hardware acceleration for Electronic Codebook (ECB), Cipher-Block Chaining (CBC), and Counter (CTR) algorithms utilizing integrated counterblock generation and previous-block caching.

4.5.4. 16/32-bit Enhanced CRC (ECRC0)

The ECRC module is designed to provide hardware calculations for flash memory verification and communications protocols. In addition to calculating a result from direct writes from firmware, the ECRC module can automatically snoop the APB bus and calculate a result from data written to or read from a particular peripheral. This allows for an automatic CRC result without directly feeding data through the ECRC module.

The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3). The 16-bit polynomial is fully programmable.

The ECRC module includes the following features:

- Support for a programmable 16-bit polynomial and one fixed 32-bit polynomial.
- Byte-level bit reversal for the CRC input.
- Byte-order reorientation of words for the CRC input.
- Word or half-word bit reversal of the CRC result.
- Ability to configure and seed an operation in a single register write.
- Support for single-cycle parallel (unrolled) CRC computation for 32-, 16-, or 8-bit blocks.
- Capability to CRC 32 bits of data per peripheral bus (APB) clock.
- Automatic APB bus snooping.
- Support for DMA writes using firmware request mode.

4.5.5. Encoder / Decoder (ENCDEC0)

The encoder / decoder module supports Manchester and Three-out-of-Six encoding and decoding from either firmware or DMA operations.

This module has the following features:

- Supports Manchester and Three-out-of-Six encoding and decoding.
- Automatic flag clearing when writing the input or reading the output data registers.
- Writing to the input data register automatically initiates an encode or decode operation.
- Optional output in one’s complement format.
- Hardware error detection for invalid input data during decode operations, which helps reduce power consumption and packet turn-around time.
- Flexible byte swapping on the input or output data.

4.6.6. Low Power Mode Advanced Capture Counter (ACCTR0)

The SiM3L1xx devices contain a low-power Advanced Capture Counter module that runs from the RTC0 clock domain and can be used with digital inputs, switch topology circuits (reed switches), or with LC resonant circuits. For switch topology circuits, the module charges one or two external lines by pulsing internal pull-up resistors and detecting whether the reed switch is open or closed. For LC resonant circuits, the inputs are periodically energized to produce a dampened sine wave and configurable discriminator circuits detect the resulting decay time-constant.

The advanced capture counter has the following general features:

- Single or differential inputs supporting single, dual, and quadrature modes of operation.
- Variety of interrupt and PM8 wake up sources.
- Provides feedback of the direction history, current and previous states, and condition flags.

The advanced capture counter has the following features for switch circuit topologies:

- Ultra low power input comparators.
- Supports a wide range of pull-up resistor values with a self-calibration engine.
- Asymmetrical integrators for low-pass filtering and switch debounce.
- Two 24-bit counters and two 24-bit digital threshold comparators.
- Supports switch flutter detection.

For LC resonant circuit topologies, the advanced capture counter includes:

- Separate minimum and maximum count registers and polarity, pulse, and toggle controls.
- Zone-based programmable timing.
- Two input comparators with support for a positive side input bias at VIO divided by 2.
- Supports a configurable excitation pulse width based on a 40 MHz oscillator and timer or an external digital stop signal.
- Two 8-bit peak counters that saturate at full scale for detecting the number of LC resonant peaks.
- Two discriminators with programmable thresholds.
- Supports a sample and hold mode for Wheatstone bridges.

All devices in the SiM3L1xx family include the low power mode advanced capture counter (ACCTR0). Table 4.2 lists the supported inputs and outputs for each of the packages.

Table 4.2. SiM3L1xx Supported Advanced Capture Counter Inputs and Outputs

Input/Output	SiM3L1x7	SiM3L1x6	SiM3L1x4
ACCTR0_IN0	✓	✓	✓
ACCTR0_IN1	✓	✓	✓
ACCTR0_LCIN0	✓	✓	
ACCTR0_LCIN1	✓	✓	✓
ACCTR0_STOP0	✓	✓	✓
ACCTR0_STOP1	✓	✓	✓
ACCTR0_LCPUL0	✓	✓	
ACCTR0_LCPUL1	✓	✓	
ACCTR0_LCBIAS0	✓	✓	
ACCTR0_LCBIAS1	✓	✓	
ACCTR0_DBG0	✓	✓	
ACCTR0_DBG1	✓	✓	

4.8. Analog

4.8.1. 12-Bit Analog-to-Digital Converter (SARADC0)

The SARADC0 module on SiM3L1xx devices implements the Successive Approximation Register (SAR) ADC architecture. The key features of the module are as follows:

- Single-ended 12-bit and 10-bit modes.
- Supports an output update rate of 250 k samples per second in 12-bit mode or 1 M samples per second in 10-bit mode.
- Operation in low power modes at lower conversion speeds.
- Selectable asynchronous hardware conversion trigger with hardware channel select.
- DC offset cancellation.
- Automatic result notification with multiple programmable thresholds.
- Support for Burst Mode, which produces one set of accumulated data per conversion-start trigger with programmable power-on settling and tracking time.
- Non-burst mode operation can also automatically accumulate multiple conversions, but a conversion start is required for each conversion.
- Conversion complete, multiple conversion complete, and FIFO overflow and underflow flags and interrupts supported.
- Flexible output data formatting.
- Sequencer allows up to eight sources to be automatically scanned using one of four channel characteristic profiles without software intervention.
- Eight-word conversion data FIFO for DMA operations.
- Includes two internal references (1.65 V fast-settling, 1.2/2.4 V precision), support for an external reference, and support for an external signal ground.

4.8.2. 10-Bit Digital-to-Analog Converter (IDAC0)

The IDAC module takes a digital value as an input and outputs a proportional constant current on a pin. The IDAC module includes the following features:

- 10-bit current DAC with support for four timer, up to seven external I/O and on demand output update triggers.
- Ability to update on rising, falling, or both edges for any of the external I/O trigger sources.
- Supports an output update rate greater than 600 k samples per second.
- Support for three full-scale output modes: 0.5 mA, 1.0 mA and 2.0 mA.
- Four-word FIFO to aid with high-speed waveform generation or DMA interactions.
- Individual FIFO overrun, underrun, and went-empty interrupt status sources.
- Support for multiple data packing formats, including: single 10-bit sample per word, dual 10-bit samples per word, or four 8-bit samples per word.
- Support for left- and right-justified data.

4.8.3. Low Current Comparators (CMP0, CMP1)

The Comparators take two analog input voltages and output the relationship between these voltages (less than or greater than) as a digital signal. The low power comparator module includes the following features:

- Multiple sources for the positive and negative inputs, including VBAT, VREF, and 8 I/O pins.
- Two outputs available: a digital synchronous latched output and a digital asynchronous raw output.
- Programmable hysteresis and response time.
- Falling or rising edge interrupt options on the comparator output.
- 6-bit programmable reference divider.

4.9. Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.
- AHB peripheral clocks to flash and RAM are enabled.
- Clocks to all APB peripherals other than the Watchdog Timer and DMAXBAR are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost.

The Port I/O latches are reset to 1 in open-drain mode. Weak pullups are enabled during and after the reset. For VBAT Supply Monitor and power-on resets, the RESET pin is driven low until the device exits the reset state.

On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to the internal low-power oscillator. The Watchdog Timer is enabled with the low frequency oscillator as its clock source. Program execution begins at location 0x00000000.

All RSTSRC0 registers may be locked against writes by setting the CLKRSTL bit in the LOCK0_PERIPHLOCK0 register to 1.

The reset sources can also optionally reset individual modules, including the low power mode charge pump, UART0, LCD0, advanced capture counter (ACCTR0), and RTC0.

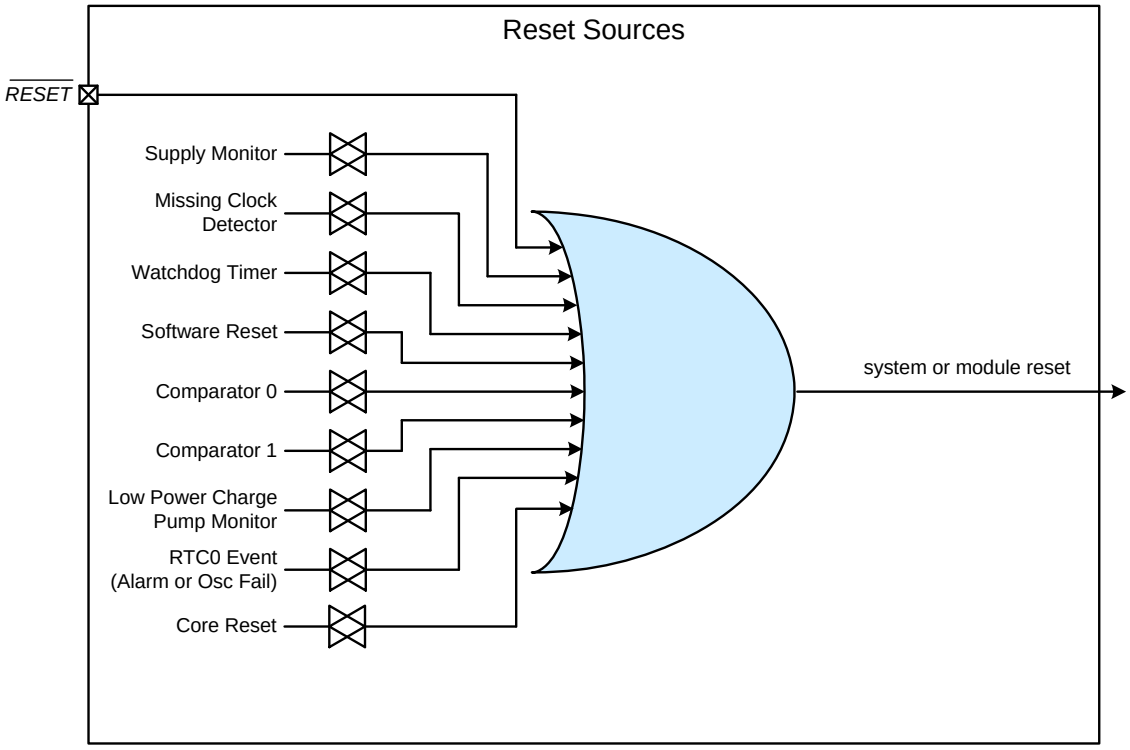


Figure 4.4. SiM3L1xx Reset Sources Block Diagram

4.10. Security

The peripherals on the SiM3L1xx devices have a register lock and key mechanism that prevents undesired accesses of the peripherals from firmware. Each bit in the PERIPHLOCKx registers controls a set of peripherals. A key sequence must be written to the KEY register to modify bits in PERIPHLOCKx. Any subsequent write to KEY will then inhibit accesses of PERIPHLOCKx until it is unlocked again through KEY. Reading the KEY register indicates the current status of the PERIPHLOCKx lock state.

If a peripheral's registers are locked, all writes will be ignored. The registers can be read, regardless of the peripheral's lock state.

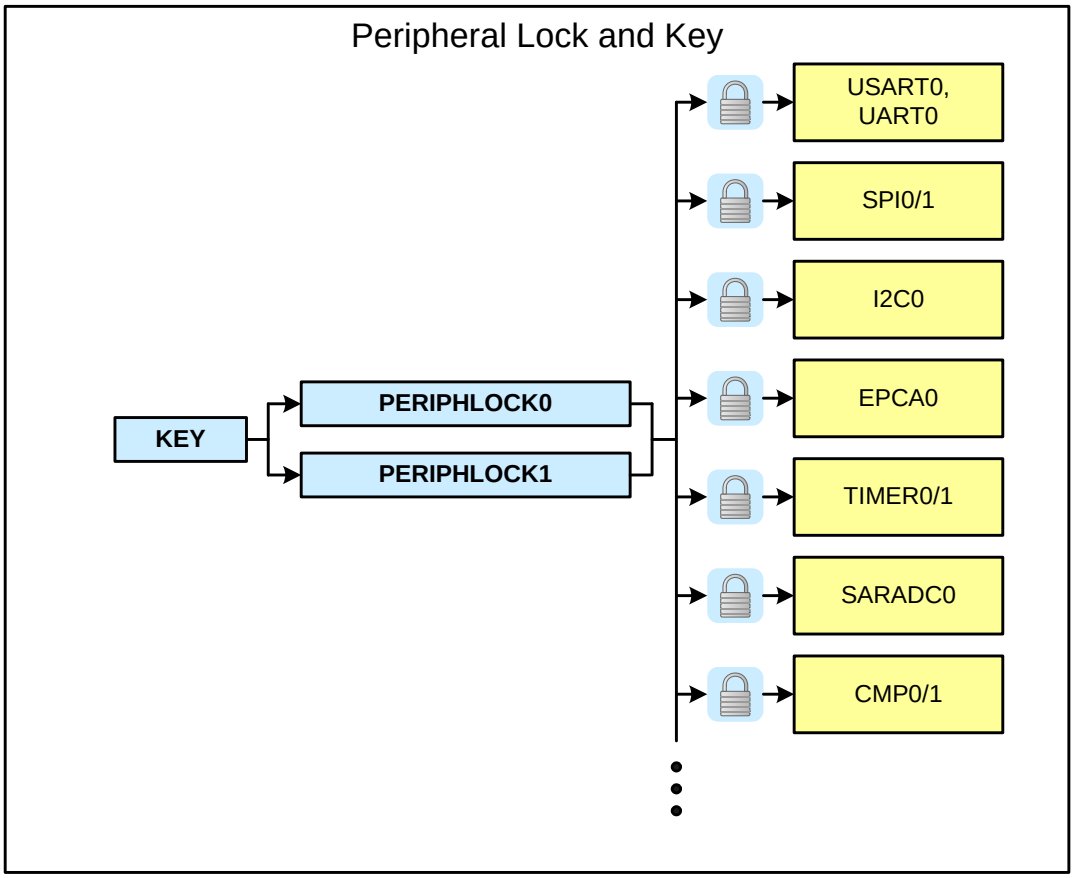


Figure 4.5. SiM3L1xx Security Block Diagram

4.11. On-Chip Debugging

The SiM3L1xx devices include JTAG and Serial Wire programming and debugging interfaces and ETM for instruction trace. The JTAG interface is supported on SiM3L1x7 devices only, and does not include boundary scan capabilites. The ETM interface is supported on SiM3L1x7, and SiM3L1x6 devices only. The JTAG and ETM interfaces can be optionally enabled to provide more visibility while debugging at the cost of using several Port I/O pins. Additionally, if the core is configured for Serial Wire (SW) mode and not JTAG, then the Serial Wire Viewer (SWV) is available to provide a single pin to send out TPIU messages. Serial Wire Viewer is supported on all SiM3Lxxx devices.

Most peripherals on SiM3L1xx devices have the option to halt or continue functioning when the core halts in debug mode.

Table 6.1. Pin Definitions and Alternate Functions for SiM3L1x7 (Continued)

Pin Name	Type	Pin Numbers (TQFP-80)	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB0.9	Standard I/O	75	VIO	✓	✓		✓	LPT0T1 INT0.9 WAKE.9 ACCTR0_LCPUL0	ADC0.1 CMP0N.1
PB0.10	Standard I/O	74	VIO	✓	✓		✓	LPT0T2 INT0.10 WAKE.10 ACCTR0_LCPUL1	ADC0.2 CMP1P.1
PB0.11/ TDO/SWV	Standard I/O / JTAG / Serial Wire Viewer	73	VIO	✓	✓		✓	LPT0T3 LPT0OUT1 INT0.11 WAKE.11	ADC0.3 CMP1N.1
PB1.0	Standard I/O	66	VIO	✓	✓	LCD0.39		LPT0T4 INT0.12 ACCTR0_LCBIAS0	CMP0P.2
PB1.1	Standard I/O	65	VIO	✓	✓	LCD0.38		LPT0T5 INT0.13 ACCTR0_LCBIAS1	CMP0N.2
PB1.2	Standard I/O	64	VIO	✓	✓	LCD0.37		LPT0T6 INT0.14 UART0_TX	CMP1P.2
PB1.3	Standard I/O	63	VIO	✓	✓	LCD0.36		LPT0T7 INT0.15 UART0_RX	CMP1N.2
PB1.4	Standard I/O	62	VIO	✓	✓	LCD0.35		ACCTR0_DBG0	ADC0.4
PB1.5	Standard I/O	61	VIO	✓	✓	LCD0.34		ACCTR0_DBG1	ADC0.5
PB1.6/TDI	Standard I/O / JTAG	60	VIO	✓	✓	LCD0.33			ADC0.6
PB1.7	Standard I/O	59	VIO	✓	✓	LCD0.32		RTC0TCLK_OUT	ADC0.7

Table 6.3. Pin Definitions and Alternate Functions for SiM3L1x4 (Continued)

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB0.2	Standard I/O	40	VIO	XBR0	✓	✓	INT0.2 WAKE.3	ADC0.23 CMP0N.1 CMP1N.0 XTAL1
PB0.3	Standard I/O	39	VIO	XBR0	✓	✓	INT0.3 WAKE.4	ADC0.0 CMP0P.1 IDAC0
PB0.4	Standard I/O	38	VIO	XBR0	✓	✓	INT0.4 WAKE.5	ACCTR0_IN0
PB0.5	Standard I/O	37	VIO	XBR0	✓	✓	INT0.5 WAKE.6	ACCTR0_IN1
PB0.6/SWV	Standard I/O /Serial Wire Viewer	36	VIO	XBR0	✓	✓	LPT0T0 LPT0OUT0 INT0.6 WAKE.8	
PB0.7	Standard I/O	32	VIO	XBR0	✓	✓	LPT0T6 INT0.7 UART0_TX	CMP1P.2
PB0.8	Standard I/O	31	VIO	XBR0	✓	✓	LPT0T7 INT0.8 UART0_RX	CMP1N.2
PB0.9	Standard I/O	30	VIO	XBR0	✓	✓	LPT0T1 INT0.9 RTC0TCLK_OUT	ADC0.1
PB2.0	Standard I/O	29	VIORF	XBR0	✓		LPT0T8 INT1.0 WAKE.12 SPI1_CTS	ADC0.2 CMP0P.4

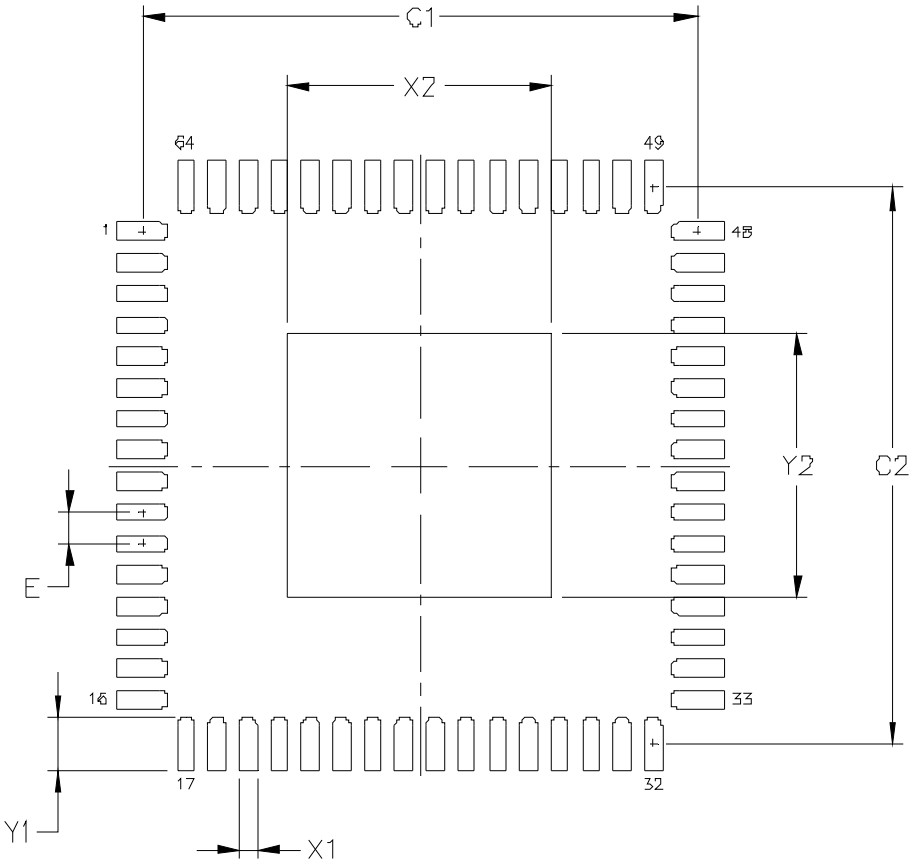


Figure 6.8. QFN-64 Landing Diagram

Table 6.7. QFN-64 Landing Diagram Dimensions

Dimension	mm
C1	8.90
C2	8.90
E	0.50
X1	0.30
Y1	0.85
X2	4.25
Y2	4.25

Notes:
1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

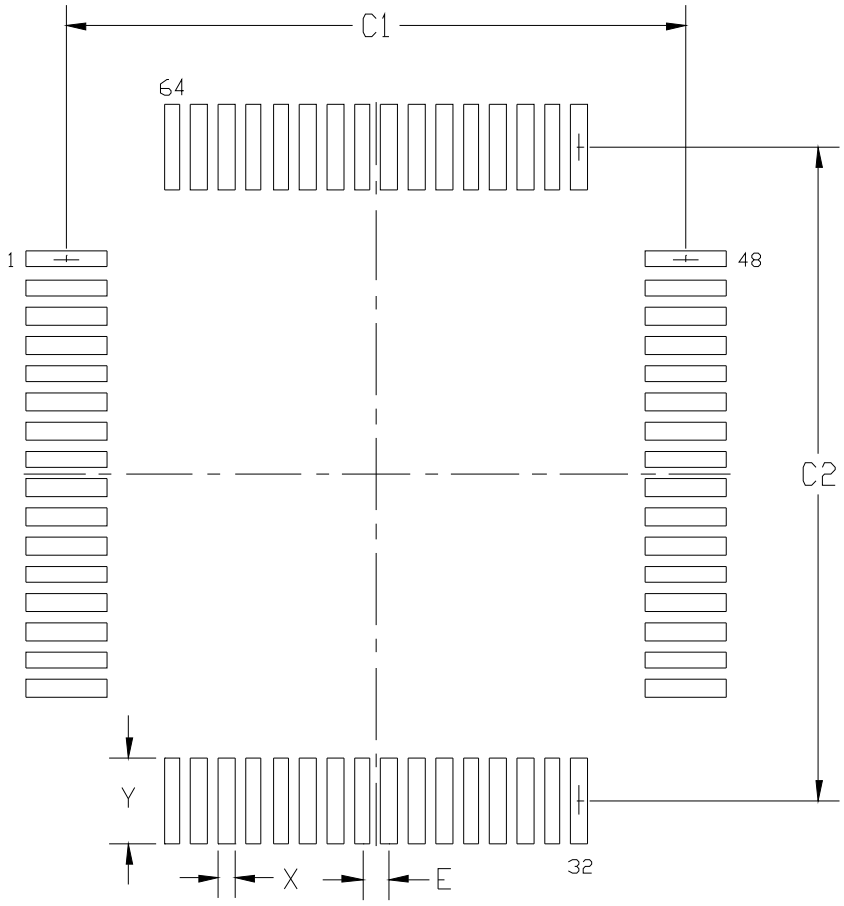
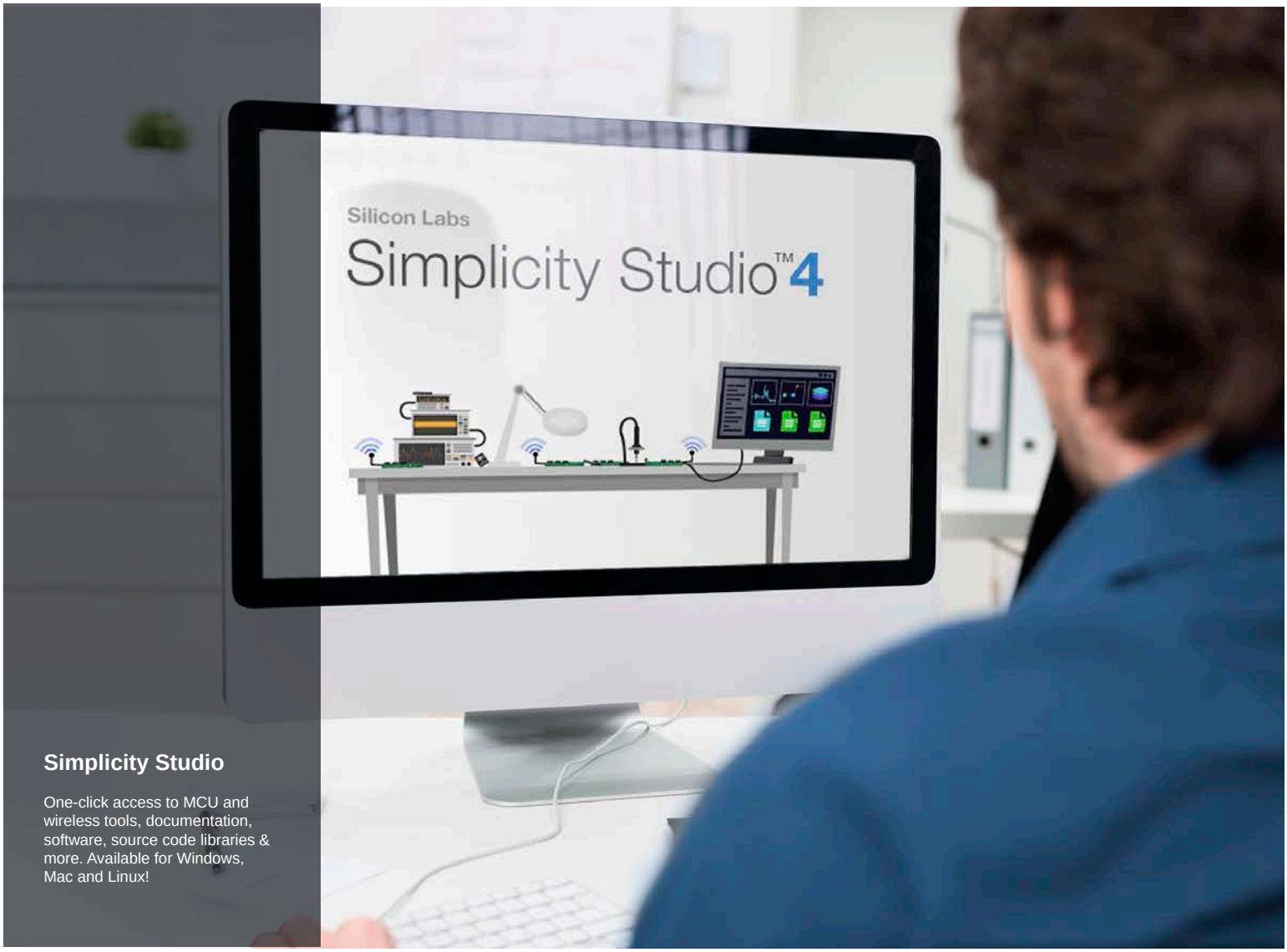


Figure 6.10. TQFP-64 Landing Diagram

Table 6.9. TQFP-64 Landing Diagram Dimensions

Dimension	Min	Max
C1	11.30	11.40
C2	11.30	11.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.



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