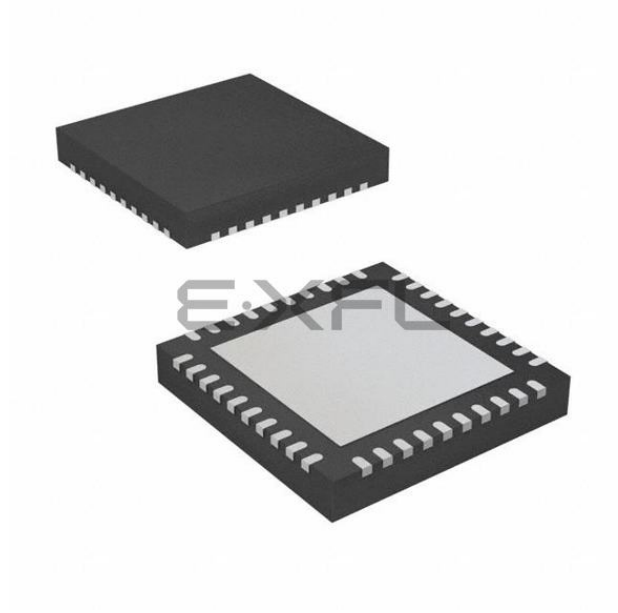

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | I²C, IrDA, SmartCard, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 28 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.8V |
| Data Converters | A/D 20x10/12b; D/A 1x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 40-VFQFN Exposed Pad |
| Supplier Device Package | 40-QFN (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/sim3l134-c-gmr |

# 2. Typical Connection Diagrams

This section provides typical connection diagrams for SiM3L1xx devices.

## 2.1. Power

Figure 2.1 shows a typical connection diagram for the power pins of the SiM3L1xx devices when the dc-dc buck converter is not used.

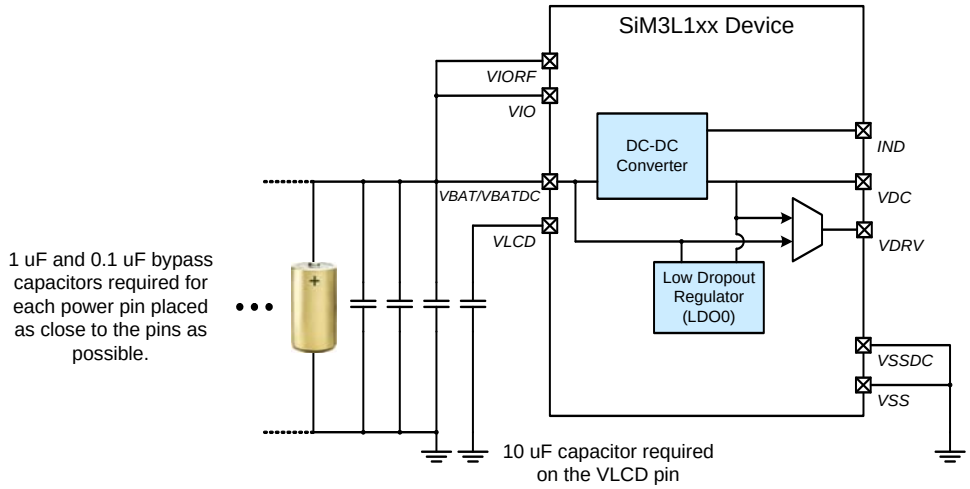


**Figure 2.1. Connection Diagram with DC-DC Converter Unused**

Figure 2.2 shows a typical connection diagram for the power pins of the SiM3L1xx devices when the internal dc-dc buck converter is in use and I/O are powered directly from the battery.

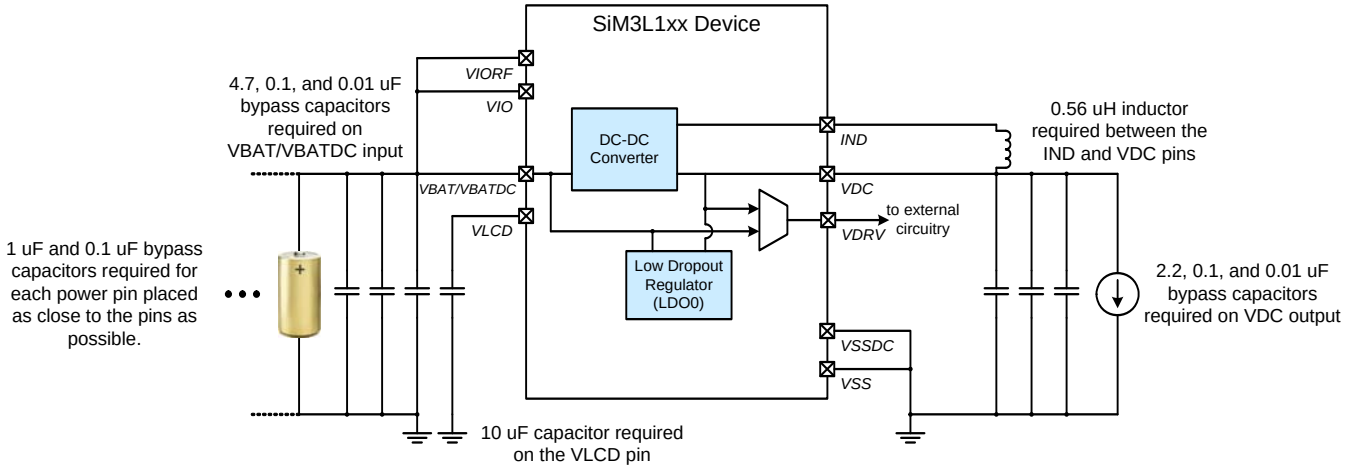


**Figure 2.2. Connection Diagram with DC-DC Converter Used and I/O Powered from Battery**

Figure 2.3 shows a typical connection diagram for the power pins of the SiM3L1xx devices when used with an external radio device like the Silicon Labs EZRadio® or EZRadioPRO® devices.

# 3. Electrical Specifications

## 3.1. Electrical Characteristics

All electrical parameters in all Tables are specified under the conditions listed in Table 3.1, unless stated otherwise.

**Table 3.1. Recommended Operating Conditions**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Supply Voltage on VBAT/VBATDC | $V_{BAT}$ | | 1.8 | — | 3.8 | V |
| Operating Supply Voltage on VDC | $V_{DC}$ | | 1.25 | — | 3.8 | V |
| Operating Supply Voltage on VDRV | $V_{DRV}$ | | 1.25 | — | 3.8 | V |
| Operating Supply Voltage on VIO | $V_{IO}$ | | 1.8 | — | $V_{BAT}$ | V |
| Operation Supply Voltage on VIORF | $V_{IORF}$ | | 1.8 | — | $V_{BAT}$ | V |
| Operation Supply Voltage on VLCD | $V_{LCD}$ | | 1.8 | — | 3.8 | V |
| System Clock Frequency (AHB) | $f_{AHB}$ | | 0 | — | 50 | MHz |
| Peripheral Clock Frequency (APB) | $f_{APB}$ | | 0 | — | 50 | MHz |
| Operating Ambient Temperature | $T_A$ | | –40 | — | +85 | °C |
| Operating Junction Temperature | $T_J$ | | –40 | — | 105 | °C |

**Note:** All voltages with respect to $V_{SS}$.

**Table 3.5. On-Chip Regulators**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DC-DC Buck Converter** | | | | | | |
| Input Voltage Range | $V_{DCIN}$ | | 1.8 | — | 3.8 | V |
| Input Supply to Output Voltage Differential (for regulation) | $V_{DCREG}$ | | 0.45 | — | — | V |
| Output Voltage Range | $V_{DCOUT}$ | | 1.25 | — | 3.8 | V |
| Output Voltage Accuracy | $V_{DCACC}$ | | — | ±25 | — | mV |
| Output Current | $I_{DCOUT}$ | | — | — | 90 | mA |
| Inductor Value[1] | $L_{DC}$ | | 0.47 | 0.56 | 0.68 | µH |
| Inductor Current Rating | $I_{LDC}$ | $I_{load}$ < 50 mA | 450 | — | — | mA |
| | | $I_{load}$ > 50 mA | 550 | — | — | mA |
| Output Capacitor Value | $C_{DCOUT}$ | | 1 | 2.2 | 10 | µF |
| Input Capacitor Value[2] | $C_{DCIN}$ | | — | 4.7 | — | µF |
| Load Regulation | $R_{load}$ | | — | 0.03 | — | mV/mA |
| Maximum DC Load Current During Startup | $I_{DCMAX}$ | | — | — | 5 | mA |
| Switching Clock Frequency | $F_{DCCLK}$ | | 1.9 | 2.9 | 3.8 | MHz |
| Local Oscillator Frequency | $F_{DCOSC}$ | | 2.4 | 2.9 | 3.4 | MHz |
| **LDO Regulators** | | | | | | |
| Input Voltage Range[3] | $V_{LDOIN}$ | Sourced from VBAT | 1.8 | — | 3.8 | V |
| | | Sourced from VDC | 1.9 | — | 3.8 | V |
| Output Voltage Range[4] | $V_{LDO}$ | | 0.8 | — | 1.9 | V |
| LDO Output Voltage Accuracy | $V_{LDOACC}$ | | — | ±25 | — | mV |
| Output Settings in PM8 (All LDOs) | $V_{LDO}$ | 1.8 V ≤ $V_{BAT}$ ≤ 2.9 V | 1.5 | | | V |
| | | 1.95 V ≤ $V_{BAT}$ ≤ 3.5 V | 1.8 | | | V |
| | | 2.0 V ≤ $V_{BAT}$ ≤ 3.8 V | 1.9 | | | V |

**Notes:**

1. See reference manual for recommended inductors.
2. Recommended: X7R or X5R ceramic capacitors with low ESR. Example: Murata GRM21BR71C225K with ESR < 10 mΩ (@ frequency > 1 MHz).
3. Input voltage specification accounts for the internal LDO dropout voltage under the maximum load condition to ensure that the LDO output voltage will remain at a valid level as long as $V_{LDOIN}$ is at or above the specified minimum.
4. The memory LDO output should always be set equal to or lower than the output of the analog LDO. When lowering both LDOs (for example to go into PM8 under low supply conditions), first adjust the memory LDO and then the analog LDO. When raising the output of both LDOs, adjust the analog LDO before adjusting the memory LDO.
5. Output range represents the programmable output range, and does not reflect the minimum voltage under all conditions. Dropout when the input supply is close to the output setting is normal, and accounted for.
6. Analog peripheral specifications assume a 1.8 V output on the analog LDO.

**Table 3.11. ACCTR (Advanced Capture Counter)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| LC Comparator Response Time, CMPMD = 11 (Highest Speed) | $t_{RESP0}$ | +100 mV Differential | — | 100 | — | ns |
| | | –100 mV Differential | — | 150 | — | ns |
| LC Comparator Response Time, CMPMD = 00 (Lowest Power) | $t_{RESP3}$ | +100 mV Differential | — | 1.4 | — | µs |
| | | –100 mV Differential | — | 3.5 | — | µs |
| LC Comparator Positive Hysteresis Mode 0 (CPMD = 11) | $HYS_{CP+}$ | CMPHYP = 00 | — | 0.37 | — | mV |
| | | CMPHYP = 01 | — | 7.9 | — | mV |
| | | CMPHYP = 10 | — | 16.7 | — | mV |
| | | CMPHYP = 11 | — | 32.8 | — | mV |
| LC Comparator Negative Hysteresis Mode 0 (CPMD = 11) | $HYS_{CP-}$ | CMPHYN = 00 | — | 0.37 | — | mV |
| | | CMPHYN = 01 | — | –7.9 | — | mV |
| | | CMPHYN = 10 | — | –16.1 | — | mV |
| | | CMPHYN = 11 | — | –32.7 | — | mV |
| LC Comparator Positive Hysteresis Mode 1 (CPMD = 10) | $HYS_{CP+}$ | CMPHYP = 00 | — | 0.47 | — | mV |
| | | CMPHYP = 01 | — | 5.85 | — | mV |
| | | CMPHYP = 10 | — | 12 | — | mV |
| | | CMPHYP = 11 | — | 24.4 | — | mV |
| LC Comparator Negative Hysteresis Mode 1 (CPMD = 10) | $HYS_{CP-}$ | CMPHYN = 00 | — | 0.47 | — | mV |
| | | CMPHYN = 01 | — | –6.0 | — | mV |
| | | CMPHYN = 10 | — | –12.1 | — | mV |
| | | CMPHYN = 11 | — | –24.6 | — | mV |
| LC Comparator Positive Hysteresis Mode 2 (CPMD = 01) | $HYS_{CP+}$ | CMPHYP = 00 | — | 0.66 | — | mV |
| | | CMPHYP = 01 | — | 4.55 | — | mV |
| | | CMPHYP = 10 | — | 9.3 | — | mV |
| | | CMPHYP = 11 | — | 19 | — | mV |
| LC Comparator Negative Hysteresis Mode 2 (CPMD = 01) | $HYS_{CP-}$ | CMPHYN = 00 | — | 0.6 | — | mV |
| | | CMPHYN = 01 | — | –4.5 | — | mV |
| | | CMPHYN = 10 | — | –9.5 | — | mV |
| | | CMPHYN = 11 | — | –19 | — | mV |

**Table 3.11. ACCTR (Advanced Capture Counter) (Continued)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| LC Comparator Positive Hysteresis Mode 3 (CPMD = 00) | $HYS_{CP+}$ | CMPHYP = 00 | — | 1.37 | — | mV |
| | | CMPHYP = 01 | — | 3.8 | — | mV |
| | | CMPHYP = 10 | — | 7.8 | — | mV |
| | | CMPHYP = 11 | — | 15.6 | — | mV |
| LC Comparator Negative Hysteresis Mode 3 (CPMD = 00) | $HYS_{CP-}$ | CMPHYN = 00 | — | 1.37 | — | mV |
| | | CMPHYN = 01 | — | –3.9 | — | mV |
| | | CMPHYN = 10 | — | –7.9 | — | mV |
| | | CMPHYN = 11 | — | –16 | — | mV |
| LC Comparator Input Range (ACCTR0_LCIN pin) | $V_{IN}$ | | –0.25 | — | $V_{BAT}$ + 0.25 | V |
| LC Comparator Common-Mode Rejection Ratio | $CMRR_{CP}$ | | — | 75 | — | dB |
| LC Comparator Power Supply Rejection Ratio | $PSRR_{CP}$ | | — | 72 | — | dB |
| LC Comparator Input Offset Voltage | $V_{OFF}$ | $T_A$ = 25 °C | –10 | 0 | 10 | mV |
| LC Comparator Input Offset Tempco | $TC_{OFF}$ | | — | 3.5 | — | µV/°C |
| Reference DAC Offset Error | $DAC_{EOFF}$ | | –1 | — | 1 | LSB |
| Reference DAC Full Scale Output | $DAC_{FS}$ | Low Range | — | $V_{IO}$/8 | — | V |
| | | High Range | — | $V_{IO}$ | — | V |
| Reference DAC Step Size | $DAC_{LSB}$ | Low Range (48 steps) | — | $V_{IO}$/384 | — | V |
| | | High Range (64 steps) | — | $V_{IO}$/64 | — | V |
| LC Oscillator Period | $T_{LCOSC}$ | | — | 25 | — | ns |
| LC Bias Output Impedance | $R_{LCBIAS}$ | 10 µA Load | — | 1 | — | kΩ |
| LC Bias Drive Strength | $I_{LCBIAS}$ | | — | — | 2 | mA |
| Pull-Up Resistor Tolerance | $R_{TOL}$ | PUVAL[4:2] = 0 to 6 | -15 | — | 15 | % |
| | | PUVAL[4:2] = 7 | -10 | — | 10 | % |

**Table 3.16. Port I/O**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output High Voltage (PB0, PB1, PB3, or PB4) | $V_{OH}$ | Low Drive, $I_{OH}$ = –1 mA | $V_{IO}$ – 0.7 | — | — | V |
| | | Low Drive, $I_{OH}$ = –10 µA | $V_{IO}$ – 0.1 | — | — | V |
| | | High Drive, $I_{OH}$ = –3 mA | $V_{IO}$ – 0.7 | — | — | V |
| | | High Drive, $I_{OH}$ = –10 µA | $V_{IO}$ – 0.1 | — | — | V |
| Output High Voltage (PB2) | $V_{OH}$ | Low Drive, $I_{OH}$ = –1 mA | $V_{IORF}$ – 0.7 | — | — | V |
| | | Low Drive, $I_{OH}$ = –10 µA | $V_{IORF}$ – 0.1 | — | — | V |
| | | High Drive, $I_{OH}$ = –3 mA | $V_{IORF}$ – 0.7 | — | — | V |
| | | High Drive, $I_{OH}$ = –10 µA | $V_{IORF}$ – 0.1 | — | — | V |
| Output Low Voltage (any Port I/O pin or $\overline{\text{RESET}}$[1]) | $V_{OL}$ | Low Drive, $I_{OL}$ = 1.4 mA | — | — | 0.6 | V |
| | | Low Drive, $I_{OL}$ = 10 µA | — | — | 0.1 | V |
| | | High Drive, $I_{OL}$ = 8.5 mA | — | — | 0.6 | V |
| | | High Drive, $I_{OL}$ = 10 µA | — | — | 0.1 | V |
| Input High Voltage (PB0, PB1, PB3, PB4 or $\overline{\text{RESET}}$) | $V_{IH}$ | | $V_{IO}$ – 0.6 | — | — | V |
| Input High Voltage (PB2) | $V_{IH}$ | | $V_{IORF}$ – 0.6 | — | — | V |
| Input Low Voltage any Port I/O pin or $\overline{\text{RESET}}$) | $V_{IL}$ | | — | — | 0.6 | V |
| Weak Pull-Up Current[2] (per pin) | $I_{PU}$ | $V_{IO}$ or $V_{IORF}$ = 1.8 | -6 | -3.5 | -2 | µA |
| | | $V_{IO}$ or $V_{IORF}$ = 3.8 | -32 | -20 | -10 | µA |
| Input Leakage (Pullups off or Analog) | $I_{LK}$ | $0 \le V_{IN} \le V_{IO}$ or $V_{IORF}$ | -1 | — | 1 | µA |

**Notes:**

1. Specifications for $\overline{\text{RESET}}$ $V_{OL}$ adhere to the low drive setting.
2. On the SiM3L1x6 and SiM3L1x4 devices, the SWV pin will have double the weak pull-up current specified whenever the device is held in reset.

## 4.1. Power

The SiM3L1xx devices include a dc-dc buck converter that can take an input from 1.8–3.8 V and create an output from 1.25–3.8 V. In addition, SiM3L1xx devices include three low dropout regulators as part of the LDO0 module: one LDO powers the analog subsystems, one LDO powers the flash and SRAM memory at 1.8 V, and one LDO powers the digital and core circuitry. Each of these regulators can be independently powered from the dc-dc converter or directly from the battery voltage, and their outputs are adjustable to conserve system power. SiM3L1xx devices also include a low power charge pump in the PMU module for use in low power modes (PM8) to further reduce the power consumption of the device.

Figure 4.2 shows the power system configuration of these devices.

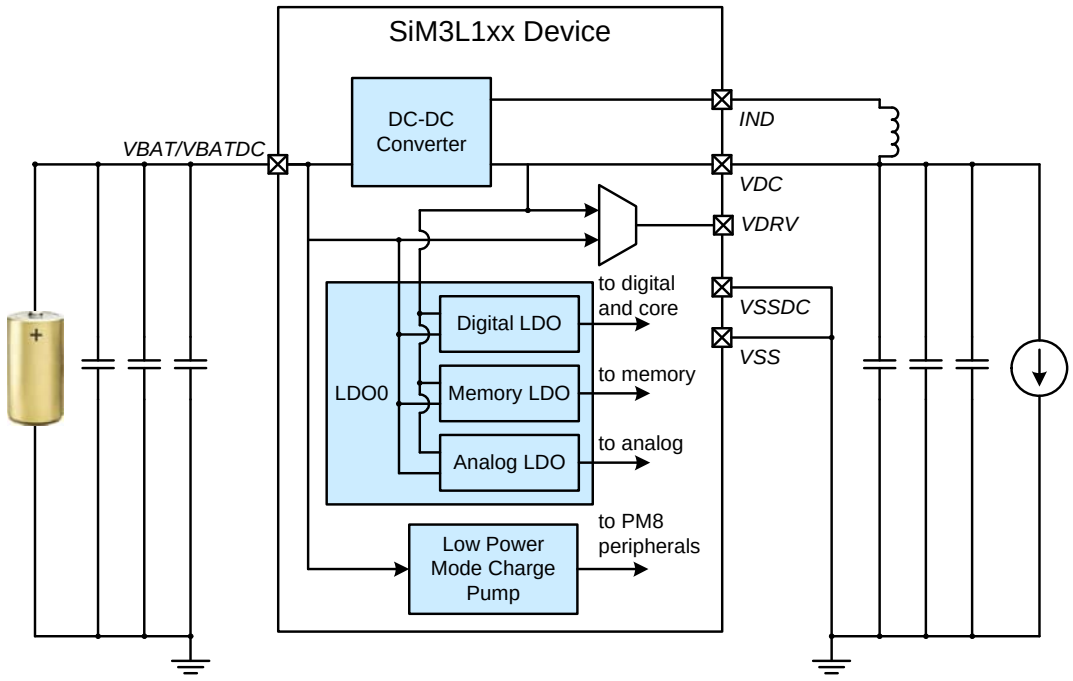


**Figure 4.2. SiM3L1xx Power**

### 4.1.1. DC-DC Buck Converter (DCDC0)

SiM3L1xx devices include an on-chip step-down dc-dc converter to efficiently utilize the energy stored in the battery, thus extending the operational life time. The dc-dc converter is a switching buck converter with a programmable output voltage that should be at least 0.45 V lower than the input battery voltage; if this criteria is not met and the converter can no longer operate, the output of the dc-dc converter automatically connects to the battery. The dc-dc converter can supply up to 100 mA and can be used to power the MCU and/or external devices in the system.

The dc-dc converter has a built in voltage reference and oscillator and will automatically limit or turn off the switching activity in case the peak inductor current rises beyond a safe limit or the output voltage rises above the programmed target value. This allows the dc-dc converter output to be safely overdriven by a secondary power source (when available) in order to preserve battery life. When enabled, the dc-dc converter can source current into the output capacitor, but cannot sink current.

The dc-dc converter includes the following features:

- Efficiently utilizes the energy stored in a battery, extending its operational lifetime.
- Input range: 1.8 to 3.8 V.
- Output range: 1.25 to 3.8 V in 50 mV (1.25–1.8 V) or 100 mV (1.8–3.8 V) steps.
- Supplies up to 100 mA.
- Includes a voltage reference and an oscillator.

#### 4.1.5.6. Power Mode Summary

The power modes described above are summarized in Table 4.1. Table 3.2 and Table 3.3 provide more information on the power consumption and wake up times for each mode.

**Table 4.1. SiM3L1xx Power Modes**

| Mode | Description | Notes |
|---|---|---|
| Normal | ■ Core operating at full speed<br>■ Code executing from flash | ■ Full device operation |
| Power Mode 1 (PM1) | ■ Core operating at full speed<br>■ Code executing from RAM | ■ Full device operation<br>■ Higher CPU bandwidth than PM0 (RAM can operate with zero wait states at any frequency) |
| Power Mode 2 (PM2) | ■ Core halted<br>■ AHB, APB and all peripherals operational at full speed | ■ Fast wakeup from any interrupt source |
| Power Mode 3 (PM3) | ■ All clocks to core and peripherals stopped<br>■ Faster wake enabled by keeping LFOSC0 or RTC0TCLK active | ■ Wake on any wake source or reset source defined in the PMU |
| Power Mode 4 (PM4) | ■ Core operating at low speed<br>■ Code executing from flash | ■ Same capabilities as PM0, operating at lower speed<br>■ Lower clock speed enables lower LDO output settings to save power |
| Power Mode 5 (PM5) | ■ Core operating at low speed<br>■ Code executing from RAM | ■ Same capabilities as PM1, operating at lower speed<br>■ Lower clock speed enables lower LDO output settings to save power |
| Power Mode 6 (PM6) | ■ Core halted<br>■ AHB, APB and all peripherals operational at low speed | ■ Same capabilities as PM2, operating at lower speed<br>■ Lower clock speed enables lower LDO output settings to save power<br>■ When running from LFOSC0, power is similar to PM3, but the device wakes much faster |
| Power Mode 8 (PM8) | ■ Low power sleep<br>■ LDO regulators are disabled and all active circuitry operates directly from VBAT<br>■ The following functions are available: ACCTR0, RTC0, UART0 running from RTC0TCLK, LPTIMER0, port match, and the LCD controller<br>■ Register and RAM state retention | ■ Lowest power consumption<br>■ Wake on any wake source or reset source defined in the PMU |

## 4.2. I/O

### 4.2.1. General Features

The SiM3L1xx ports have the following features:

- 5 V tolerant.
- Push-pull or open-drain output modes to the VIO or VIORF voltage level.
- Analog or digital modes.
- Option for high or low output drive strength.
- Port Match allows the device to recognize a change on a port pin value.
- Internal pull-up resistors are enabled or disabled on a port-by-port basis.
- Two external interrupts with up to 16 inputs each provide monitoring capability for external signals.
- Internal Pulse Generator Timer (PB0 only) to generate simple square waves and pulses.

### 4.2.2. Crossbar

The SiM3L1xx devices have one crossbar with the following features:

- Flexible peripheral assignment to port pins.
- Pins can be individually skipped to move peripherals as needed for design or layout considerations.

The crossbar has a fixed priority for each I/O function and assigns these functions to the port pins. When a digital resource is selected, the least-significant unassigned port pin is assigned to that resource. If a port pin is assigned, the crossbar skips that pin when assigning the next selected resource. Additionally, the crossbar will skip port pins whose associated bits in the PBSKIPEN registers are set. This provides flexibility when designing a system: pins involved with sensitive analog measurements can be moved away from digital I/O, and peripherals can be moved around the chip as needed to ease layout constraints.

## 4.5. Data Peripherals

### 4.5.1. 10-Channel DMA Controller

The DMA facilitates autonomous peripheral operation, allowing the core to finish tasks more quickly without spending time polling or waiting for peripherals to interrupt. This helps reduce the overall power consumption of the system, as the device can spend more time in low-power modes.

The DMA controller has the following features:

- Utilizes ARM PrimeCell uDMA architecture.
- Implements 10 channels.
- DMA crossbar supports DTM0, DTM1, DTM2, SARADC0, IDAC0, I2C0, SPI0, SPI1, USART0, AES0, ENCDEC0, EPCA0, external pin triggers, and timers.
- Supports primary, alternate, and scatter-gather data structures to implement various types of transfers.
- Access allowed to all AHB and APB memory space.

### 4.5.2. Data Transfer Managers (DTM0, DTM1, DTM2)

The Data Transfer Manager is a module that collects DMA request signals from various peripherals and generates a series of master DMA requests based on a state-driven configuration. This master request drives a set of DMA channels to perform functions such as assembling and transferring communication packets to external devices. This capability saves power by allowing the core to remain in a low power mode during complex transfer operations. A combination of simple and peripheral scatter-gather DMA configurations can be used to perform complex operations while reducing memory requirements.

The DTM acts as a side channel for the peripheral's DMA control signals. When active, it manages the DMA control signals for the peripherals. When the DTMn module is inactive, the peripherals communicate directly to the DMA module.

The DTMn module has the following features:

- State descriptions stored in RAM with up to 15 states supported per module.
- Supports up to 15 source peripherals and up to 15 destination peripherals per module, in addition to memory or peripherals that do not require a data request.
- Includes error detection and an optional transfer timeout.
- Includes notifications for state transitions.

### 4.5.3. 128/192/256-bit Hardware AES Encryption (AES0)

The basic AES block cipher is implemented in hardware. The integrated hardware support for Cipher Block Chaining (CBC) and Counter (CTR) algorithms results in identical performance, memory bandwidth, and memory footprint between the most basic Electronic Codebook (ECB) algorithm and these more complex algorithms. This hardware accelerator translates to more core bandwidth available for other functions or a power savings for low-power applications.

The AES module includes the following features:

- Operates on 4-word (16-byte) blocks.
- Supports key sizes of 128, 192, and 256 bits for both encryption and decryption.
- Generates the round key for decryption operations.
- All cipher operations can be performed without any firmware intervention for multiple 4-word blocks (up to 32 kB).
- Support for various chained and stream-ciphering configurations with XOR paths on both the input and output.
- Internal 4-word FIFOs to facilitate DMA operations.
- Integrated key storage.
- Hardware acceleration for Electronic Codebook (ECB), Cipher-Block Chaining (CBC), and Counter (CTR) algorithms utilizing integrated counterblock generation and previous-block caching.

### 4.6.6. Low Power Mode Advanced Capture Counter (ACCTR0)

The SiM3L1xx devices contain a low-power Advanced Capture Counter module that runs from the RTC0 clock domain and can be used with digital inputs, switch topology circuits (reed switches), or with LC resonant circuits. For switch topology circuits, the module charges one or two external lines by pulsing internal pull-up resistors and detecting whether the reed switch is open or closed. For LC resonant circuits, the inputs are periodically energized to produce a dampened sine wave and configurable discriminator circuits detect the resulting decay time-constant.

The advanced capture counter has the following general features:

- Single or differential inputs supporting single, dual, and quadrature modes of operation.
- Variety of interrupt and PM8 wake up sources.
- Provides feedback of the direction history, current and previous states, and condition flags.

The advanced capture counter has the following features for switch circuit topologies:

- Ultra low power input comparators.
- Supports a wide range of pull-up resistor values with a self-calibration engine.
- Asymmetrical integrators for low-pass filtering and switch debounce.
- Two 24-bit counters and two 24-bit digital threshold comparators.
- Supports switch flutter detection.

For LC resonant circuit topologies, the advanced capture counter includes:

- Separate minimum and maximum count registers and polarity, pulse, and toggle controls.
- Zone-based programmable timing.
- Two input comparators with support for a positive side input bias at VIO divided by 2.
- Supports a configurable excitation pulse width based on a 40 MHz oscillator and timer or an external digital stop signal.
- Two 8-bit peak counters that saturate at full scale for detecting the number of LC resonant peaks.
- Two discriminators with programmable thresholds.
- Supports a sample and hold mode for Wheatstone bridges.

All devices in the SiM3L1xx family include the low power mode advanced capture counter (ACCTR0). Table 4.2 lists the supported inputs and outputs for each of the packages.

**Table 4.2. SiM3L1xx Supported Advanced Capture Counter Inputs and Outputs**

| Input/Output | SiM3L1x7 | SiM3L1x6 | SiM3L1x4 |
|---|---|---|---|
| ACCTR0_IN0 | ✓ | ✓ | ✓ |
| ACCTR0_IN1 | ✓ | ✓ | ✓ |
| ACCTR0_LCIN0 | ✓ | ✓ | |
| ACCTR0_LCIN1 | ✓ | ✓ | ✓ |
| ACCTR0_STOP0 | ✓ | ✓ | ✓ |
| ACCTR0_STOP1 | ✓ | ✓ | ✓ |
| ACCTR0_LCPUL0 | ✓ | ✓ | |
| ACCTR0_LCPUL1 | ✓ | ✓ | |
| ACCTR0_LCBIAS0 | ✓ | ✓ | |
| ACCTR0_LCBIAS1 | ✓ | ✓ | |
| ACCTR0_DBG0 | ✓ | ✓ | |
| ACCTR0_DBG1 | ✓ | ✓ | |

## 4.7. Communications Peripherals

### 4.7.1. USART (USART0)

The USART uses two signals (TX and RX) to communicate serially with an external device. In addition to these signals, the USART module can optionally use a clock (UCLK) or hardware handshaking (RTS and CTS).

The USART module provides the following features:

- Independent transmitter and receiver configurations with separate 16-bit baud rate generators.
- Synchronous or asynchronous transmissions and receptions.
- Clock master or slave operation with programmable polarity and edge controls.
- Up to 5 Mbaud (synchronous or asynchronous, TX or RX, and master or slave) or 1 Mbaud Smartcard (TX or RX).
- Individual enables for generated clocks during start, stop, and idle states.
- Internal transmit and receive FIFOs with flush capability and support for byte, half-word, and word reads and writes.
- Data bit lengths from 5 to 9 bits.
- Programmable inter-packet transmit delays.
- Auto-baud detection with support for the LIN SYNC byte.
- Automatic parity generation (with enable).
- Automatic start and stop generation (with separate enables).
- Transmit and receive hardware flow-control.
- Independent inversion correction for TX, RX, RTS, and CTS signals.
- IrDA modulation and demodulation with programmable pulse widths.
- Smartcard ACK/NACK support.
- Parity error, frame error, overrun, and underrun detection.
- Multi-master and half-duplex support.
- Multiple loop-back modes supported.
- Multi-processor communications support.

### 4.7.2. UART (UART0)

The low-power UART uses two signals (TX and RX) to communicate serially with an external device.

The UART0 module can operate in PM8 mode by taking the clock directly from the RTC0 time clock (RTC0TCLK) and running from the low power mode charge pump. This will allow the system to conserve power while transmitting or receiving UART traffic. The UART supports standard baud-rates of 9600, 4800, 2400 and 1200 in this low power mode.

The UART0 module provides the following features:

- Independent transmitter and receiver configurations with separate 16-bit baud rate generators.
- Asynchronous transmissions and receptions.
- Up to 5 Mbaud (TX or RX).
- Internal transmit and receive FIFOs with flush capability and support for byte, half-word, and word reads and writes.
- Data bit lengths from 5 to 9 bits.
- Programmable inter-packet transmit delays.
- Auto-baud detection with support for the LIN SYNC byte.
- Automatic parity generation (with enable).
- Automatic start and stop generation (with separate enables).
- Independent inversion correction for TX and RX signals.
- Parity error, frame error, overrun, and underrun detection.
- Half-duplex support.

## 4.10. Security

The peripherals on the SiM3L1xx devices have a register lock and key mechanism that prevents undesired accesses of the peripherals from firmware. Each bit in the PERIPHLOCKx registers controls a set of peripherals. A key sequence must be written to the KEY register to modify bits in PERIPHLOCKx. Any subsequent write to KEY will then inhibit accesses of PERIPHLOCKx until it is unlocked again through KEY. Reading the KEY register indicates the current status of the PERIPHLOCKx lock state.

If a peripheral's registers are locked, all writes will be ignored. The registers can be read, regardless of the peripheral's lock state.

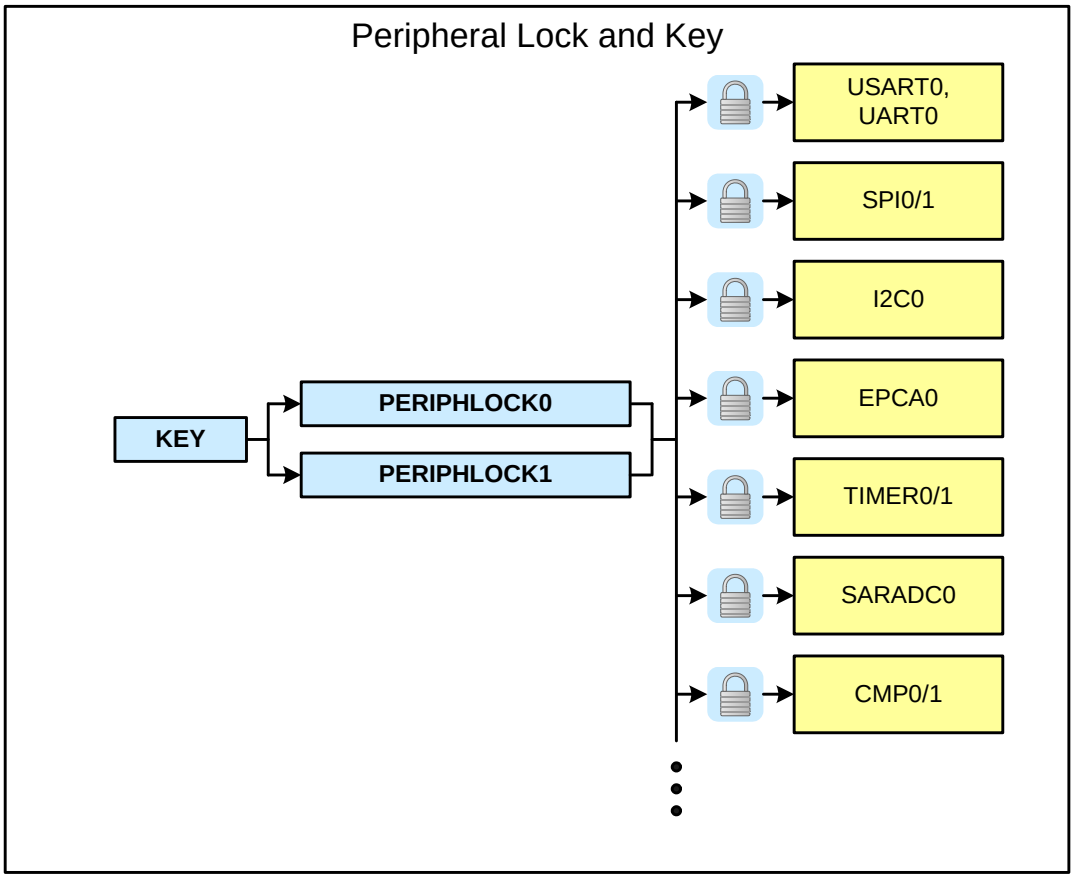


**Figure 4.5. SiM3L1xx Security Block Diagram**

## 4.11. On-Chip Debugging

The SiM3L1xx devices include JTAG and Serial Wire programming and debugging interfaces and ETM for instruction trace. The JTAG interface is supported on SiM3L1x7 devices only, and does not include boundary scan capabilites. The ETM interface is supported on SiM3L1x7, and SiM3L1x6 devices only. The JTAG and ETM interfaces can be optionally enabled to provide more visibility while debugging at the cost of using several Port I/O pins. Additionally, if the core is configured for Serial Wire (SW) mode and not JTAG, then the Serial Wire Viewer (SWV) is available to provide a single pin to send out TPIU messages. Serial Wire Viewer is supported on all SiM3Lxxx devices.

Most peripherals on SiM3L1xx devices have the option to halt or continue functioning when the core halts in debug mode.

**Table 6.1. Pin Definitions and Alternate Functions for SiM3L1x7 (Continued)**

| Pin Name | Type | Pin Numbers (TQFP-80) | I/O Voltage Domain | Crossbar Capability | Port Match | LCD Interface | Output Toggle Logic | External Trigger Inputs / Digital Functions | Analog Functions |
|---|---|---|---|---|---|---|---|---|---|
| PB3.4 | Standard I/O | 43 | VIO | ✓ | ✓ | LCD0.23 | | INT1.12 | CMP0P.6 |
| PB3.5 | Standard I/O | 42 | VIO | ✓ | ✓ | LCD0.22 | | INT1.13 | CMP0N.6 |
| PB3.6 | Standard I/O | 41 | VIO | ✓ | ✓ | LCD0.21 | | INT1.14 | CMP1P.6 |
| PB3.7 | Standard I/O | 40 | VIO | ✓ | ✓ | LCD0.20 | | INT1.15 | CMP1N.6 |
| PB3.8 | Standard I/O | 39 | VIO | | ✓ | LCD0.19 | | | CMP0P.7 |
| PB3.9 | Standard I/O | 38 | VIO | | ✓ | LCD0.18 | | | CMP0N.7 |
| PB3.10 | Standard I/O | 37 | VIO | | ✓ | LCD0.17 | | | CMP1P.7 |
| PB3.11 | Standard I/O | 36 | VIO | | ✓ | LCD0.16 | | | CMP1N.7 |
| PB3.12 | Standard I/O | 35 | VIO | | ✓ | LCD0.15 | | | ADC0.18 |
| PB3.13 | Standard I/O | 34 | VIO | | ✓ | LCD0.14 | | | ADC0.19 |
| PB3.14 | Standard I/O | 33 | VIO | | ✓ | COM0.3 | | | |
| PB3.15 | Standard I/O | 32 | VIO | | ✓ | COM0.2 | | | |
| PB4.0 | Standard I/O | 29 | VIO | | ✓ | COM0.1 | | | |
| PB4.1 | Standard I/O | 28 | VIO | | ✓ | COM0.0 | | | |
| PB4.2 | Standard I/O | 27 | VIO | | ✓ | LCD0.13 | | | |
| PB4.3 | Standard I/O | 26 | VIO | | ✓ | LCD0.12 | | | |
| PB4.4 | Standard I/O | 25 | VIO | | ✓ | LCD0.11 | | | |
| PB4.5 | Standard I/O | 24 | VIO | | ✓ | LCD0.10 | | | |
| PB4.6 | Standard I/O | 23 | VIO | | ✓ | LCD0.9 | | PMU_Asleep | |
| PB4.7 | Standard I/O | 22 | VIO | | ✓ | LCD0.8 | | | |
| PB4.8 | Standard I/O | 21 | VIO | | ✓ | LCD0.7 | | | |

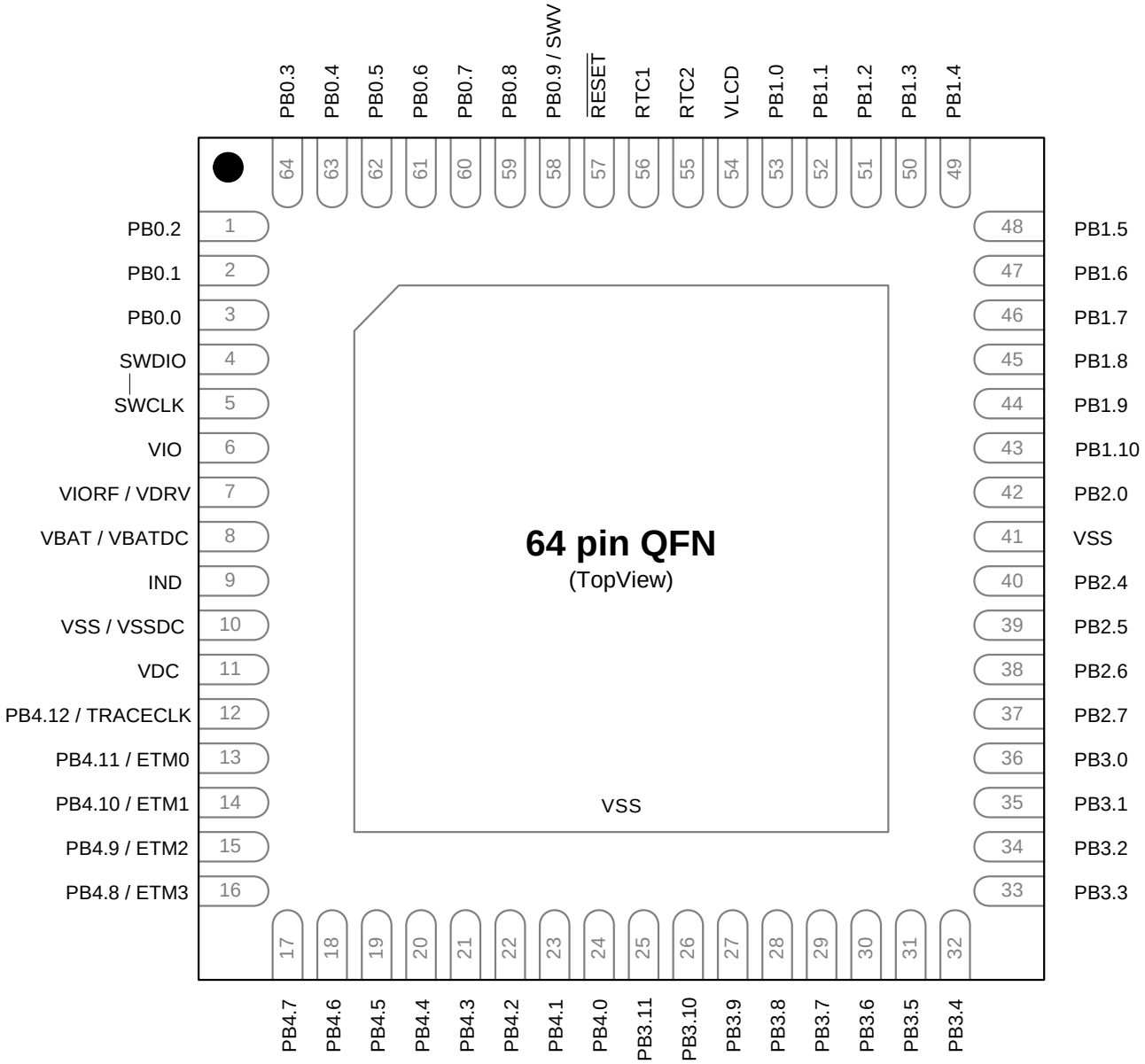


**Figure 6.3. SiM3L1x6-GM Pinout**

### 6.4.1. TQFP-80 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

### 6.4.2. TQFP-80 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.

### 6.4.3. TQFP-80 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

### 6.5.1. QFN-64 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

### 6.5.2. QFN-64 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 3x3 array of 1.0 mm square openings on a 1.5 mm pitch should be used for the center ground pad.

### 6.5.3. QFN-64 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

### 6.7.1. QFN-40 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

### 6.7.2. QFN-40 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 3x3 array of 1.1 mm square openings on a 1.6 mm pitch should be used for the center ground pad.

### 6.7.3. QFN-40 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.