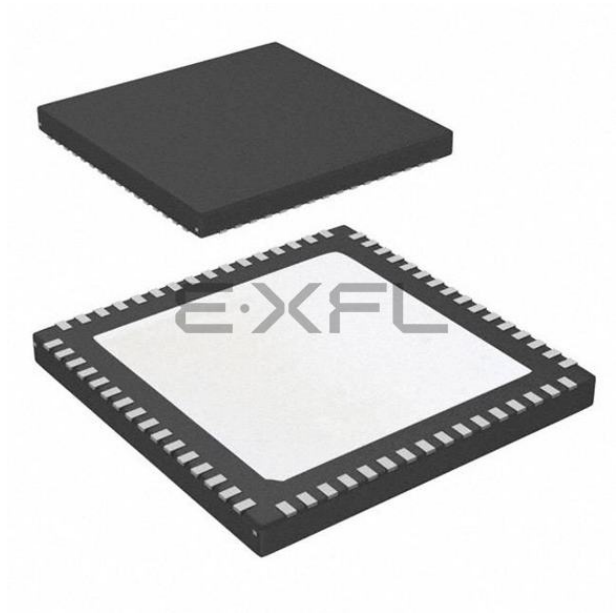

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 23x10/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/sim3l136-c-gm

1. Related Documents and Conventions

1.1. Related Documents

This data sheet accompanies several documents to provide the complete description of the SiM3L1xx devices.

1.1.1. SiM3L1xx Reference Manual

The Silicon Laboratories SiM3L1xx Reference Manual provides the detailed description for each peripheral on the SiM3L1xx devices.

1.1.2. Hardware Access Layer (HAL) API Description

The Silicon Laboratories Hardware Access Layer (HAL) API provides C-language functions to modify and read each bit in the SiM3L1xx devices. This description can be found in the SiM3xxxx HAL API Reference Manual.

1.1.3. ARM Cortex-M3 Reference Manual

The ARM-specific features like the Nested Vectored Interrupt Controller are described in the ARM Cortex-M3 reference documentation. The online reference manual can be found here:
http://infocenter.arm.com/help/topic/com.arm.doc.subset.cortexm3/index.html#cortexm3.

1.2. Conventions

The block diagrams in this document use the following formatting conventions:

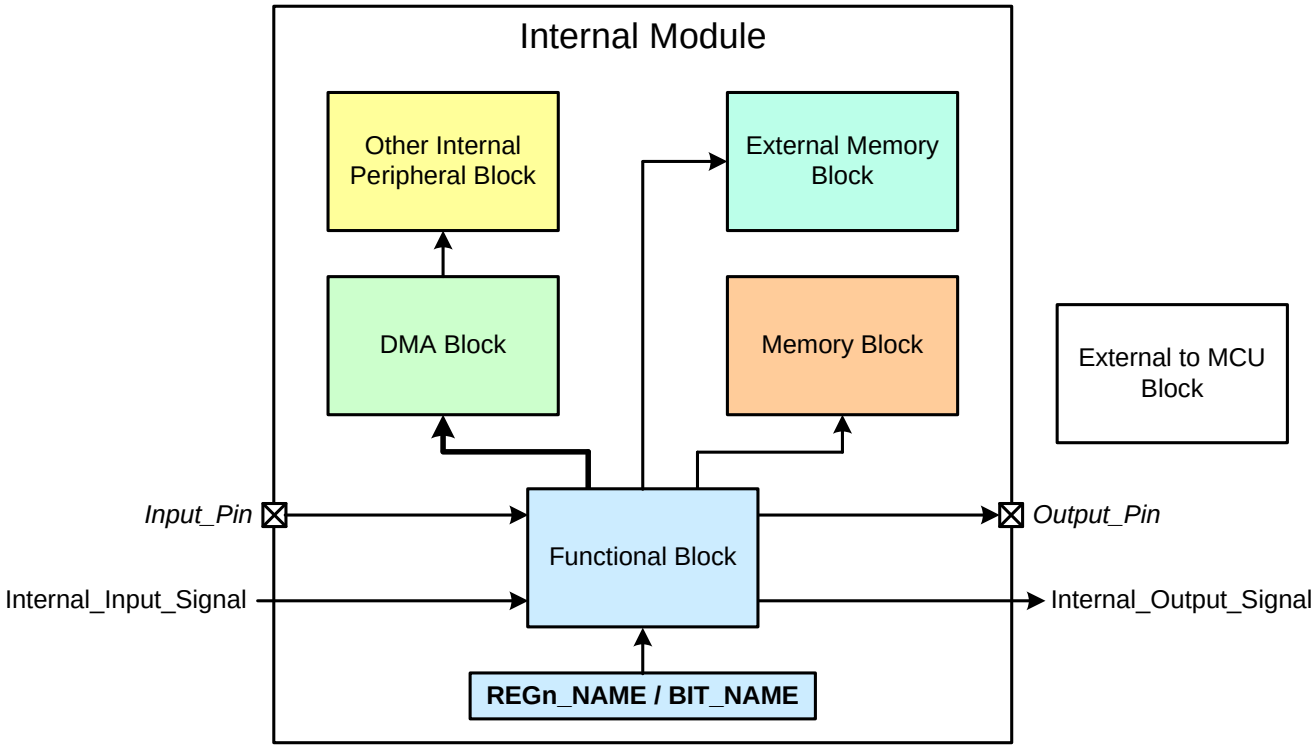


Figure 1.1. Block Diagram Conventions

Table 3.10. IDAC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static Performance						
Resolution	N_{bits}			10		Bits
Integral Nonlinearity	INL		—	±0.5	±2	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL		—	±0.5	±1	LSB
Output Compliance Range	V_{OCR}		—	—	V_{BAT} – 1.0	V
Full Scale Output Current	I_{OUT}	2 mA Range, T_A = 25 °C	1.98	2.046	2.1	mA
		1 mA Range, T_A = 25 °C	0.99	1.023	1.05	mA
		0.5 mA Range, T_A = 25 °C	491	511.5	525	µA
Offset Error	E_{OFF}		—	250	—	nA
Full Scale Error Tempco	TC_{FS}	2 mA Range	—	100	—	ppm/°C
VBAT Power Supply Rejection Ratio		2 mA Range	—	–220	—	ppm/V
Test Load Impedance (to V_{SS})	R_{TEST}		—	1	—	kΩ
Dynamic Performance						
Output Settling Time to 1/2 LSB		min output to max output	—	1.2	—	µs
Startup Time			—	3	—	µs

Table 3.14. Comparator (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CMPHYP = 00	—	1.37	—	mV
		CMPHYP = 01	—	3.8	—	mV
		CMPHYP = 10	—	7.8	—	mV
		CMPHYP = 11	—	15.6	—	mV
Negative Hysteresis Mode 3 (CPMD = 11)	HYS_{CP-}	CMPHYN = 00	—	1.37	—	mV
		CMPHYN = 01	—	–3.9	—	mV
		CMPHYN = 10	—	–7.9	—	mV
		CMPHYN = 11	—	–16	—	mV
Input Range (CP+ or CP–)	V_{IN}		–0.25	—	V_{BAT} + 0.25	V
Input Pin Capacitance	C_{CP}		—	7.5	—	pF
Common-Mode Rejection Ratio	$CMRR_{CP}$		—	75	—	dB
Power Supply Rejection Ratio	$PSRR_{CP}$		—	72	—	dB
Input Offset Voltage	V_{OFF}	T_A = 25 °C	–10	0	10	mV
Input Offset Tempco	TC_{OFF}		—	3.5	—	µV/°C
Reference DAC Resolution	N_{Bits}			6		bits

Table 3.15. LCD0

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Charge Pump Output Voltage Error	V_{CPERR}		—	±50	—	mV
LCD Clock Frequency	F_{LCD}		16	—	33	kHz

peripherals and may individually shut down and gate the clocks of any or all peripherals for power savings.

The on-chip debugging interface (SWJ-DP) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging.

Each device is specified for 1.8 to 3.8 V operation over the industrial temperature range (–40 to +85 °C). The SiM3L1xx devices are available in 40-pin or 64-pin QFN and 64-pin or 80-pin TQFP packages. All package options are lead-free and RoHS compliant. See Table 5.1 for ordering information. A block diagram is included in Figure 4.1.

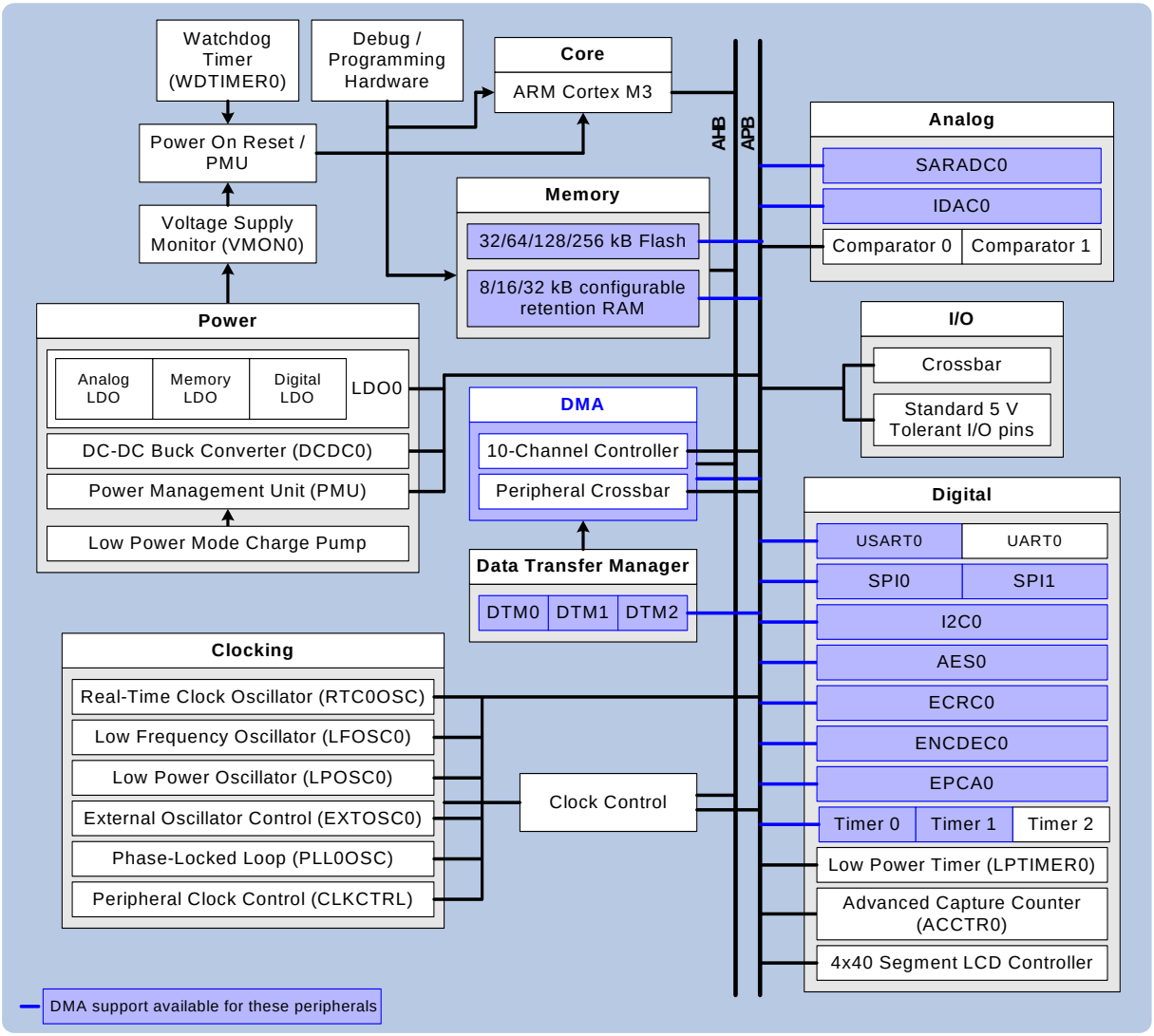


Figure 4.1. Precision32™ SiM3L1xx Family Block Diagram

- Supports synchronizing the regulator switching with the system clock.
- Automatically limits the peak inductor current if the load current rises beyond a safe limit.
- Automatically goes into bypass mode if the battery voltage cannot provide sufficient headroom.
- Sources current, but cannot sink current.

4.1.2. Three Low Dropout LDO Regulators (LDO0)

The SiM3L1xx devices include one LDO0 module with three low dropout regulators. Each of these regulators have independent switches to select the battery voltage or the output of the dc-dc converter as the input to each LDO, and an adjustable output voltage.

The LDOs consume little power and provide flexibility in choosing a power supply for the system. Each regulator can be independently adjusted between 0.8 and 1.9 V output.

4.1.3. Voltage Supply Monitor (VMON0)

The SiM3L1xx devices include a voltage supply monitor that can monitor the main supply voltage. This module includes the following features:

- Main supply “VBAT Low” (VBAT below the early warning threshold) notification.
- Holds the device in reset if the main VBAT supply drops below the VBAT Reset threshold.

The voltage supply monitor allows devices to function in known, safe operating conditions without the need for external hardware.

4.1.4. Power Management Unit (PMU)

The Power Management Unit on the SiM3L1xx manages the power systems of the device. It manages the power-up sequence during power on and the wake up sources for PM8. On power-up, the PMU ensures the core voltages are a proper value before core instruction execution begins.

The VDRV pin powers external circuitry from either the VBAT battery input voltage or the output of the dc-dc converter on VDC. The PMU includes an internal switch to select one of these sources for the VDRV pin.

The PMU has a specialized VBAT-divided-by-2 charge pump that can power some internal modules while in PM8 to save power.

The PMU module includes the following features:

- Provides the enable or disable for the analog power system, including the three LDO regulators.
- Up to 14 pin wake inputs can wake the device from Power Mode 8.
- The Low Power Timer, RTC0 (alarms and oscillator failure), Comparator 0, Advanced Capture Counter, LCD0 VBAT monitor, UART0, low power mode charge pump failure, and the RESET pin can also serve as wake sources for Power Mode 8.
- Controls which 4 kB RAM blocks are retained while in Power Mode 8.
- Provides a PMU_Asleep signal to a pin as an indicator that the device is in PM8.
- Specialized charge pump to reduce power consumption in PM8.

Provides control for the internal switch between VBAT and VDC to power the VDRV pin for external circuitry.

4.1.5. Device Power Modes

The SiM3L1xx devices feature seven low power modes in addition to normal operating mode. Several peripherals provide wake up sources for these low power modes, including the Low Power Timer (LPTIMER0), RTC0 (alarms and oscillator failure notification), Comparator 0 (CMP0), Advanced Capture Counter (ACCTR0), LCD VBAT monitor (LCD0), UART0, low power mode charge pump failure, and PMU Pin Wake.

In addition, all peripherals can have their clocks disabled to reduce power consumption whenever a peripheral is not being used using the clock control (CLKCTRL) registers.

4.1.5.1. Normal Mode (Power Mode 0) and Power Mode 4

Normal Mode and Power Mode 4 are fully operational modes with code executing from flash memory. PM4 is the same as Normal Mode, but with the clocks operating at a lower speed. This enables power to be conserved by reducing the LDO regulator outputs.

4.4. Integrated LCD Controller (LCD0)

SiM3L1xx devices contain an LCD segment driver and on-chip bias generation that supports static, 2-mux, 3-mux and 4-mux LCDs with 1/2 or 1/3 bias. The on-chip charge pump with programmable output voltage allows software contrast control which is independent of the supply voltage. LCD timing is derived from the RTC timer clock (RTC0TCLK) to allow precise control over the refresh rate.

The SiM3L1xx devices use registers to store the enabled/disabled state of individual LCD segments. All LCD waveforms are generated on-chip based on the contents of these registers with flexible waveform control to reduce power consumption wherever possible. An LCD blinking function is also supported on a subset of LCD segments.

The LCD0 module has the following features:

- Up to 40 segment pins and 4 common pins.
- Supports LCDs with 1/2 or 1/3 bias.
- Includes an on-chip charge pump with programmable output that allows firmware to control the contrast independent of the supply voltage.
- The RTC timer clock (RTC0TCLK) determines the LCD timing and refresh rate.
- All LCD waveforms are generated on-chip based on the contents of the LCD0 registers with flexible waveform control.
- LCD segments can be placed in a discharge state for a configurable number of RTC clock cycles before switching to the next state to reduce power consumption due to display loading.
- Includes a VBAT monitor that can serve as a wakeup source for Power Mode 8.
- Supports four hardware auto-contrast modes: bypass, constant, minimum, and auto-bypass.
- Supports hardware blinking for up to 8 segments.

4.6.3. Real-Time Clock (RTC0)

The RTC module includes a 32-bit timer that allows up to 36 hours of independent time-keeping when used with a 32.768 kHz watch crystal. The RTC provides three alarm events in addition to a missing clock event, which can also function as interrupt, reset, or wakeup sources on SiM3L1xx devices.

The RTC module includes internal loading capacitors that are programmable to 16 discrete levels, allowing compatibility with a wide range of crystals.

The RTC timer clock can be buffered and routed to a port bank pin to provide an accurate, low frequency clock to other devices while the core is in its lowest power down mode. The module also includes a low power internal low frequency oscillator that reduces low power mode current and is available for other modules to use as a clock source.

The RTC module includes the following features:

- 32-bit timer (supports up to 36 hours) with three separate alarms.
- Option for one alarm to automatically reset the RTC timer.
- Missing clock detector.
- Can be used with the internal Low Frequency Oscillator or with an external 32.768 kHz crystal (no additional resistors or capacitors necessary).
- Programmable internal loading capacitors support a wide range of external 32.768 kHz crystals.
- The RTC timer clock (RTC0CLK) can be buffered and routed to an I/O pin to provide an accurate, low frequency clock to other devices while the core is in its lowest power down mode.
- The RTC module can be powered from the low power mode charge pump for lowest possible power consumption while in PM8.

4.6.4. Low Power Timer (LPTIMER0)

The Low Power Timer (LPTIMER) module runs from the RTC timer clock (RTC0CLK), allowing the LPTIMER to operate even if the AHB and APB clocks are disabled. The LPTIMER counter can increment using one of two clock sources: the clock selected by the RTC0 module, or rising or falling edges of an external signal.

The Low Power Timer includes the following features:

- Runs on low-frequency RTC timer clock (RTC0TCLK).
- The LPTIMER counter can increment using one of two clock sources: the RTC0TCLK or rising or falling edges of an external signal.
- Overflow and threshold-match detection.
- Timer reset on threshold-match allows square-wave generation at a variable output frequency.
- Supports PWM with configurable period and duty cycle.
- The LPTIMER module can be powered from the low power mode charge pump for lowest possible power consumption while in PM8.

4.6.5. Watchdog Timer (WDTIMER0)

The WDTIMER module includes a 16-bit timer, a programmable early warning interrupt, and a programmable reset period. The timer registers are protected from inadvertent access by an independent lock and key interface.

The watchdog timer runs from the low frequency oscillator (LFOSC0).

The Watchdog Timer has the following features:

- Programmable timeout interval.
- Optional interrupt to warn when the Watchdog Timer is nearing the reset trip value.
- Lock-out feature to prevent any modification until a system reset.

4.6.6. Low Power Mode Advanced Capture Counter (ACCTR0)

The SiM3L1xx devices contain a low-power Advanced Capture Counter module that runs from the RTC0 clock domain and can be used with digital inputs, switch topology circuits (reed switches), or with LC resonant circuits. For switch topology circuits, the module charges one or two external lines by pulsing internal pull-up resistors and detecting whether the reed switch is open or closed. For LC resonant circuits, the inputs are periodically energized to produce a dampened sine wave and configurable discriminator circuits detect the resulting decay time-constant.

The advanced capture counter has the following general features:

- Single or differential inputs supporting single, dual, and quadrature modes of operation.
- Variety of interrupt and PM8 wake up sources.
- Provides feedback of the direction history, current and previous states, and condition flags.

The advanced capture counter has the following features for switch circuit topologies:

- Ultra low power input comparators.
- Supports a wide range of pull-up resistor values with a self-calibration engine.
- Asymmetrical integrators for low-pass filtering and switch debounce.
- Two 24-bit counters and two 24-bit digital threshold comparators.
- Supports switch flutter detection.

For LC resonant circuit topologies, the advanced capture counter includes:

- Separate minimum and maximum count registers and polarity, pulse, and toggle controls.
- Zone-based programmable timing.
- Two input comparators with support for a positive side input bias at VIO divided by 2.
- Supports a configurable excitation pulse width based on a 40 MHz oscillator and timer or an external digital stop signal.
- Two 8-bit peak counters that saturate at full scale for detecting the number of LC resonant peaks.
- Two discriminators with programmable thresholds.
- Supports a sample and hold mode for Wheatstone bridges.

All devices in the SiM3L1xx family include the low power mode advanced capture counter (ACCTR0). Table 4.2 lists the supported inputs and outputs for each of the packages.

Table 4.2. SiM3L1xx Supported Advanced Capture Counter Inputs and Outputs

Input/Output	SiM3L1x7	SiM3L1x6	SiM3L1x4
ACCTR0_IN0	✓	✓	✓
ACCTR0_IN1	✓	✓	✓
ACCTR0_LCIN0	✓	✓	
ACCTR0_LCIN1	✓	✓	✓
ACCTR0_STOP0	✓	✓	✓
ACCTR0_STOP1	✓	✓	✓
ACCTR0_LCPUL0	✓	✓	
ACCTR0_LCPUL1	✓	✓	
ACCTR0_LCBIAS0	✓	✓	
ACCTR0_LCBIAS1	✓	✓	
ACCTR0_DBG0	✓	✓	
ACCTR0_DBG1	✓	✓	

4.7. Communications Peripherals

4.7.1. USART (USART0)

The USART uses two signals (TX and RX) to communicate serially with an external device. In addition to these signals, the USART module can optionally use a clock (UCLK) or hardware handshaking (RTS and CTS).

The USART module provides the following features:

- Independent transmitter and receiver configurations with separate 16-bit baud rate generators.
- Synchronous or asynchronous transmissions and receptions.
- Clock master or slave operation with programmable polarity and edge controls.
- Up to 5 Mbaud (synchronous or asynchronous, TX or RX, and master or slave) or 1 Mbaud Smartcard (TX or RX).
- Individual enables for generated clocks during start, stop, and idle states.
- Internal transmit and receive FIFOs with flush capability and support for byte, half-word, and word reads and writes.
- Data bit lengths from 5 to 9 bits.
- Programmable inter-packet transmit delays.
- Auto-baud detection with support for the LIN SYNC byte.
- Automatic parity generation (with enable).
- Automatic start and stop generation (with separate enables).
- Transmit and receive hardware flow-control.
- Independent inversion correction for TX, RX, RTS, and CTS signals.
- IrDA modulation and demodulation with programmable pulse widths.
- Smartcard ACK/NACK support.
- Parity error, frame error, overrun, and underrun detection.
- Multi-master and half-duplex support.
- Multiple loop-back modes supported.
- Multi-processor communications support.

4.7.2. UART (UART0)

The low-power UART uses two signals (TX and RX) to communicate serially with an external device.

The UART0 module can operate in PM8 mode by taking the clock directly from the RTC0 time clock (RTC0TCLK) and running from the low power mode charge pump. This will allow the system to conserve power while transmitting or receiving UART traffic. The UART supports standard baud-rates of 9600, 4800, 2400 and 1200 in this low power mode.

The UART0 module provides the following features:

- Independent transmitter and receiver configurations with separate 16-bit baud rate generators.
- Asynchronous transmissions and receptions.
- Up to 5 Mbaud (TX or RX).
- Internal transmit and receive FIFOs with flush capability and support for byte, half-word, and word reads and writes.
- Data bit lengths from 5 to 9 bits.
- Programmable inter-packet transmit delays.
- Auto-baud detection with support for the LIN SYNC byte.
- Automatic parity generation (with enable).
- Automatic start and stop generation (with separate enables).
- Independent inversion correction for TX and RX signals.
- Parity error, frame error, overrun, and underrun detection.
- Half-duplex support.

4.8. Analog

4.8.1. 12-Bit Analog-to-Digital Converter (SARADC0)

The SARADC0 module on SiM3L1xx devices implements the Successive Approximation Register (SAR) ADC architecture. The key features of the module are as follows:

- Single-ended 12-bit and 10-bit modes.
- Supports an output update rate of 250 k samples per second in 12-bit mode or 1 M samples per second in 10-bit mode.
- Operation in low power modes at lower conversion speeds.
- Selectable asynchronous hardware conversion trigger with hardware channel select.
- DC offset cancellation.
- Automatic result notification with multiple programmable thresholds.
- Support for Burst Mode, which produces one set of accumulated data per conversion-start trigger with programmable power-on settling and tracking time.
- Non-burst mode operation can also automatically accumulate multiple conversions, but a conversion start is required for each conversion.
- Conversion complete, multiple conversion complete, and FIFO overflow and underflow flags and interrupts supported.
- Flexible output data formatting.
- Sequencer allows up to eight sources to be automatically scanned using one of four channel characteristic profiles without software intervention.
- Eight-word conversion data FIFO for DMA operations.
- Includes two internal references (1.65 V fast-settling, 1.2/2.4 V precision), support for an external reference, and support for an external signal ground.

4.8.2. 10-Bit Digital-to-Analog Converter (IDAC0)

The IDAC module takes a digital value as an input and outputs a proportional constant current on a pin. The IDAC module includes the following features:

- 10-bit current DAC with support for four timer, up to seven external I/O and on demand output update triggers.
- Ability to update on rising, falling, or both edges for any of the external I/O trigger sources.
- Supports an output update rate greater than 600 k samples per second.
- Support for three full-scale output modes: 0.5 mA, 1.0 mA and 2.0 mA.
- Four-word FIFO to aid with high-speed waveform generation or DMA interactions.
- Individual FIFO overrun, underrun, and went-empty interrupt status sources.
- Support for multiple data packing formats, including: single 10-bit sample per word, dual 10-bit samples per word, or four 8-bit samples per word.
- Support for left- and right-justified data.

4.8.3. Low Current Comparators (CMP0, CMP1)

The Comparators take two analog input voltages and output the relationship between these voltages (less than or greater than) as a digital signal. The low power comparator module includes the following features:

- Multiple sources for the positive and negative inputs, including VBAT, VREF, and 8 I/O pins.
- Two outputs available: a digital synchronous latched output and a digital asynchronous raw output.
- Programmable hysteresis and response time.
- Falling or rising edge interrupt options on the comparator output.
- 6-bit programmable reference divider.

Table 6.1. Pin Definitions and Alternate Functions for SiM3L1x7

Pin Name	Type	Pin Numbers (TQFP-80)	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
VSS	Ground	12 31 52 71							
VSSDC	Ground (DC-DC)	12							
VIO	Power (I/O)	7 30 68							
VIORF	Power (RF I/O)	8							
VBAT/ VBATDC		10							
VDRV		9							
VDC		13							
VLCD	Power (LCD Charge Pump)	67							
IND	DC-DC Inductor	11							
$\overline{\text{RESET}}$	Active-low Reset	72							
TCK/ SWCLK	JTAG / Serial Wire	6							
TMS/ SWDIO	JTAG / Serial Wire	5							
RTC1	RTC Oscillator Input	70							
RTC2	RTC Oscillator Output	69							

Table 6.1. Pin Definitions and Alternate Functions for SiM3L1x7 (Continued)

Pin Name	Type	Pin Numbers (TQFP-80)	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB0.0	Standard I/O	4	VIO	✓	✓		✓	INT0.0 WAKE.0	ADC0.20 VREF CMP0P.0
PB0.1	Standard I/O	3	VIO	✓	✓		✓	INT0.1 WAKE.1	ADC0.21 VREFGND CMP0N.0
PB0.2	Standard I/O	2	VIO	✓	✓		✓	INT0.2 WAKE.2	ADC0.22 CMP1P.0 XTAL2
PB0.3	Standard I/O	1	VIO	✓	✓		✓	INT0.3 WAKE.3	ADC0.23 CMP1N.0 XTAL1
PB0.4	Standard I/O	80	VIO	✓	✓		✓	INT0.4 WAKE.4	ADC0.0 CMP0P.1 IDAC0
PB0.5	Standard I/O	79	VIO	✓	✓		✓	INT0.5 WAKE.5 ACCTR0_STOP0	ACCTR0_IN0
PB0.6	Standard I/O	78	VIO	✓	✓		✓	INT0.6 WAKE.6 ACCTR0_STOP1	ACCTR0_IN1
PB0.7	Standard I/O	77	VIO	✓	✓		✓	INT0.7 WAKE.7	ACCTR0_LCIN0
PB0.8	Standard I/O	76	VIO	✓	✓		✓	LPT0T0 LPT0OUT0 INT0.8 WAKE.8	ACCTR0_LCIN1

Table 6.1. Pin Definitions and Alternate Functions for SiM3L1x7 (Continued)

Pin Name	Type	Pin Numbers (TQFP-80)	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB1.8	Standard I/O	58	VIO	✓	✓	LCD0.31			CMP0P.3
PB1.9	Standard I/O	57	VIO	✓	✓	LCD0.30			CMP0N.3
PB1.10	Standard I/O	56	VIO	✓	✓	LCD0.29			CMP1P.3
PB1.11	Standard I/O	55	VIO	✓	✓	LCD0.28			CMP1N.3
PB2.0	Standard I/O	54	VIORF	✓	✓			LPT0T8 INT1.0 WAKE.12 SPI1_CTS	ADC0.8 CMP0P.4
PB2.1	Standard I/O	53	VIORF	✓	✓			LPT0T9 INT1.1 WAKE.13 VIORFCLK	ADC0.9 CMP0N.4
PB2.4	Standard I/O	51	VIORF	✓	✓			LPT0T12 INT1.4 SPI1_SCLK	ADC0.10 CMP0P.5
PB2.5	Standard I/O	50	VIORF	✓	✓			LPT0T13 INT1.5 SPI1_MISO	ADC0.11 CMP0N.5
PB2.6	Standard I/O	49	VIORF	✓	✓			LPT0T14 INT1.6 SPI1_MOSI	ADC0.12 CMP1P.5
PB2.7	Standard I/O	48	VIORF	✓	✓			INT1.7 SPI1_NSS	ADC0.13 CMP1N.5
PB3.0	Standard I/O	47	VIO	✓	✓	LCD0.27		INT1.8	ADC0.14
PB3.1	Standard I/O	46	VIO	✓	✓	LCD0.26		INT1.9	ADC0.15
PB3.2	Standard I/O	45	VIO	✓	✓	LCD0.25		INT1.10	ADC0.16
PB3.3	Standard I/O	44	VIO	✓	✓	LCD0.24		INT1.11	ADC0.17

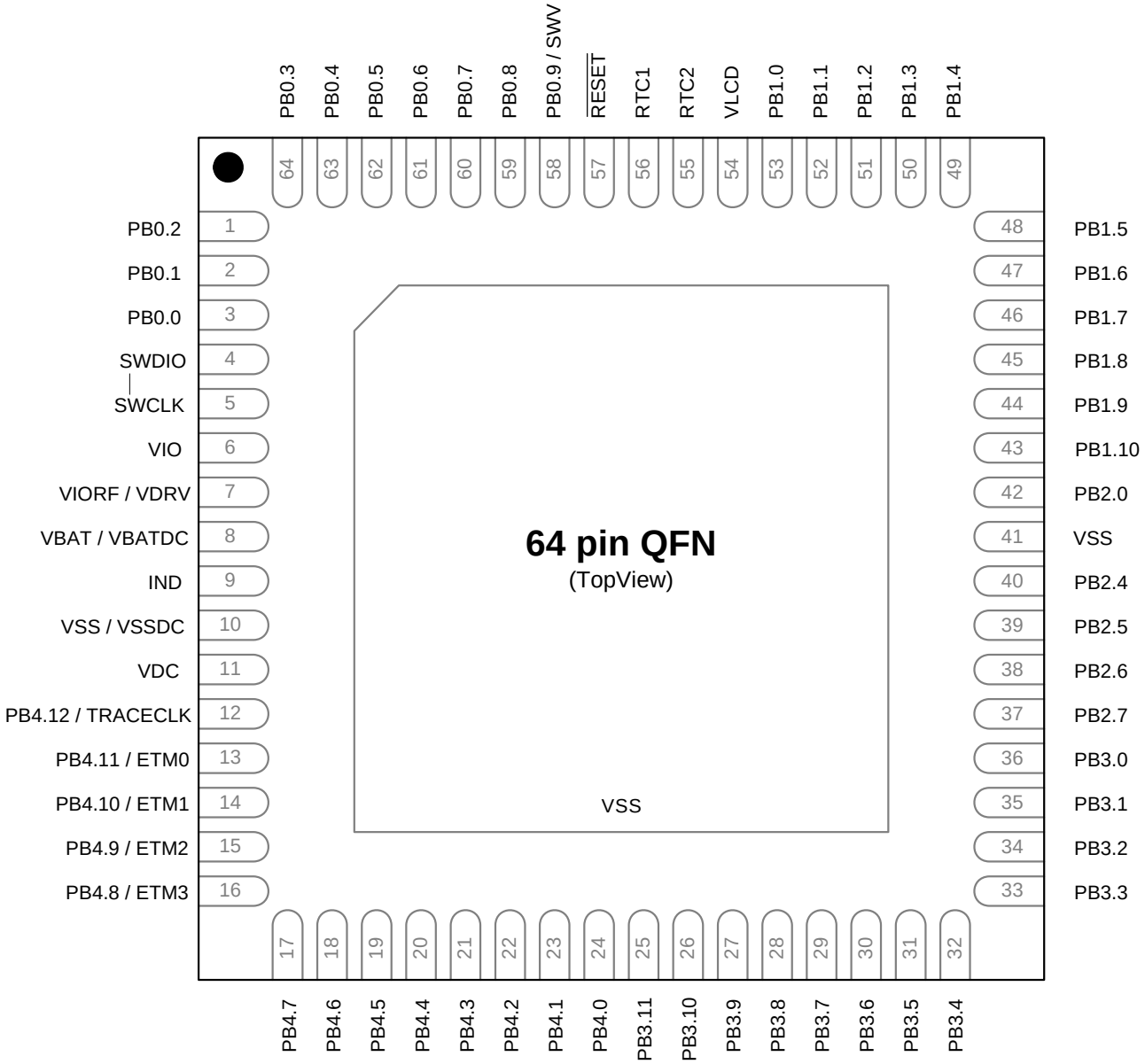


Figure 6.3. SiM3L1x6-GM Pinout

Table 6.3. Pin Definitions and Alternate Functions for SiM3L1x4 (Continued)

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB3.6	Standard I/O	14	VIO	XBR0	✓		INT1.14	ADC0.13
PB3.7	Standard I/O	13	VIO	XBR0	✓		INT1.15	ADC0.14
PB3.8	Standard I/O	12	VIO		✓			ADC0.15
PB3.9	Standard I/O	11	VIO		✓			ADC0.16

Table 6.4. TQFP-80 Package Dimensions

Dimension	Min	Nominal	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.20	0.27
c	0.09	—	0.20
D	14.00 BSC		
D1	12.00 BSC		
e	0.50 BSC		
E	14.00 BSC		
E1	12.00 BSC		
L	0.45	0.60	0.75
L1	1.00 Ref		
Θ	0°	3.5°	7°
aaa	0.20		
bbb	0.20		
ccc	0.08		
ddd	0.08		
eee	0.05		

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant ADD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.5.1. QFN-64 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.5.2. QFN-64 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 3x3 array of 1.0 mm square openings on a 1.5 mm pitch should be used for the center ground pad.

6.5.3. QFN-64 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Table 6.8. TQFP-64 Package Dimensions

Dimension	Min	Nominal	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	—	0.20
D	12.00 BSC		
D1	10.00 BSC		
e	0.50 BSC		
E	12.00 BSC		
E1	10.00 BSC		
L	0.45	0.60	0.75
Θ	0°	3.5°	7°
aaa	—	—	0.20
bbb	—	—	0.20
ccc	—	—	0.08
ddd	—	—	0.08

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant ACD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

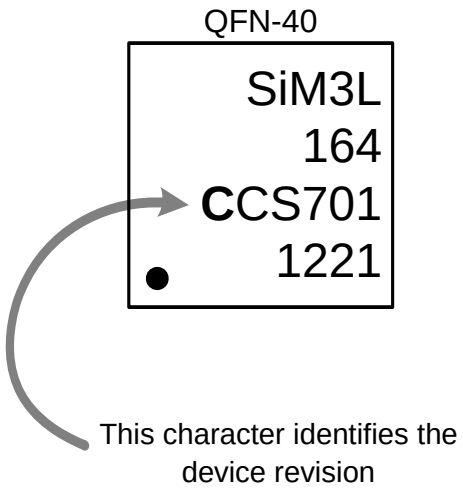
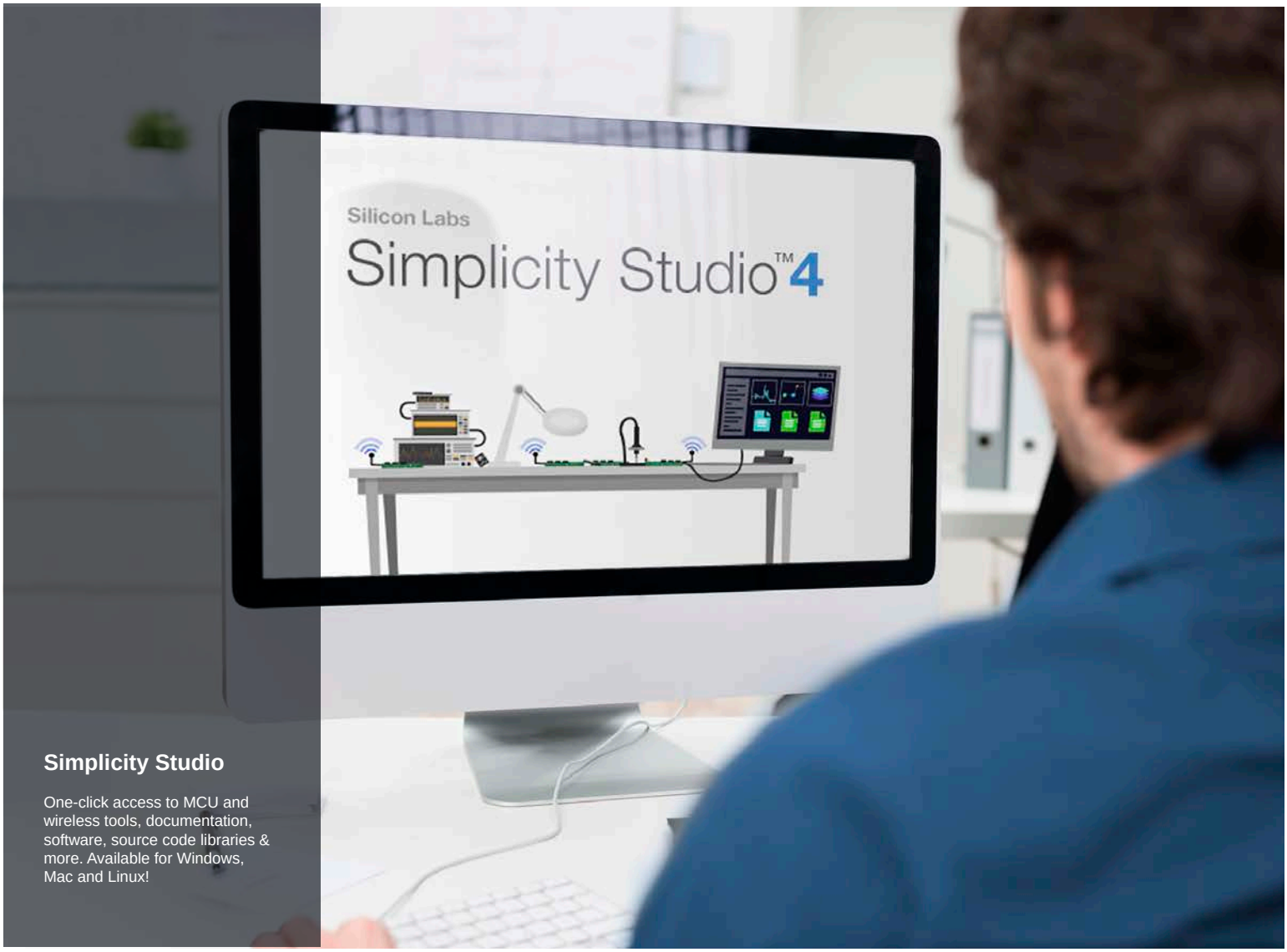


Figure 7.3. SiM3L1x4-GM Revision Information



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