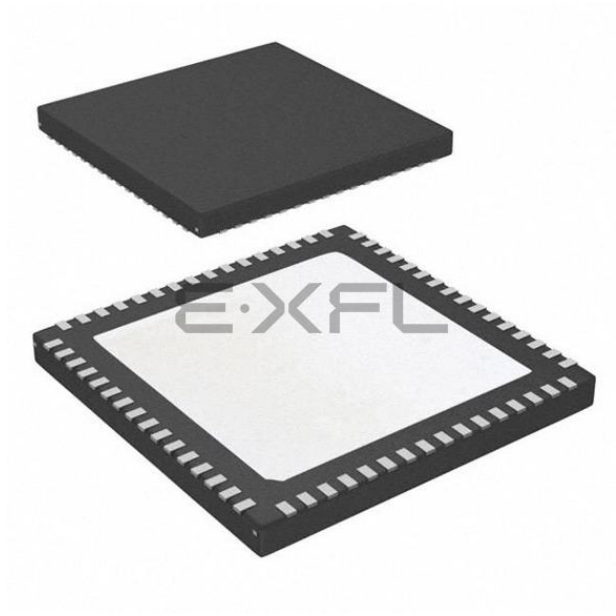

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 23x10/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/sim3l136-c-gmr

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 1[1,2,3,4]—Full speed with code executing from RAM, peripheral clocks ON	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	13.4	16.6	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	4.7	—	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	810	—	µA
Power Mode 1[1,2,3,4]—Full speed with code executing from RAM, peripheral clocks OFF	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	9.4	12.5	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	3.3	—	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	630	—	µA
Power Mode 1[1,2,3,4]—Full speed with code executing from RAM, LDOs powered by dc-dc at 1.9 V, peripheral clocks OFF	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz V_{BAT} = 3.3 V	—	7.05	—	mA
		F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz V_{BAT} = 3.8 V	—	6.3	—	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz V_{BAT} = 3.3 V	—	2.75	—	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz V_{BAT} = 3.8 V	—	2.6	—	mA
Power Mode 2[1,2,3,4,5]—Core halted with peripheral clocks ON	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	7.6	11.3	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	2.75	—	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	575	—	µA

Notes:

1. Currents are additive. For example, where I_{BAT} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded I_{VIO} is included in all I_{BAT} PM8 production test measurements.

Table 3.5. On-Chip Regulators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC-DC Buck Converter						
Input Voltage Range	V_{DCIN}		1.8	—	3.8	V
Input Supply to Output Voltage Differential (for regulation)	V_{DCREG}		0.45	—	—	V
Output Voltage Range	V_{DCOUT}		1.25	—	3.8	V
Output Voltage Accuracy	V_{DCACC}		—	±25	—	mV
Output Current	I_{DCOUT}		—	—	90	mA
Inductor Value[1]	L_{DC}		0.47	0.56	0.68	µH
Inductor Current Rating	I_{LDC}	I_{load} < 50 mA	450	—	—	mA
		I_{load} > 50 mA	550	—	—	mA
Output Capacitor Value	C_{DCOUT}		1	2.2	10	µF
Input Capacitor Value[2]	C_{DCIN}		—	4.7	—	µF
Load Regulation	R_{load}		—	0.03	—	mV/mA
Maximum DC Load Current During Startup	I_{DCMAX}		—	—	5	mA
Switching Clock Frequency	F_{DCCLK}		1.9	2.9	3.8	MHz
Local Oscillator Frequency	F_{DCOSC}		2.4	2.9	3.4	MHz
LDO Regulators						
Input Voltage Range[3]	V_{LDOIN}	Sourced from VBAT	1.8	—	3.8	V
		Sourced from VDC	1.9	—	3.8	V
Output Voltage Range[4]	V_{LDO}		0.8	—	1.9	V
LDO Output Voltage Accuracy	V_{LDOACC}		—	±25	—	mV
Output Settings in PM8 (All LDOs)	V_{LDO}	1.8 V ≤ V_{BAT} ≤ 2.9 V	1.5			V
		1.95 V ≤ V_{BAT} ≤ 3.5 V	1.8			V
		2.0 V ≤ V_{BAT} ≤ 3.8 V	1.9			V

Notes:

1. See reference manual for recommended inductors.
2. Recommended: X7R or X5R ceramic capacitors with low ESR. Example: Murata GRM21BR71C225K with ESR < 10 mΩ (@ frequency > 1 MHz).
3. Input voltage specification accounts for the internal LDO dropout voltage under the maximum load condition to ensure that the LDO output voltage will remain at a valid level as long as V_{LDOIN} is at or above the specified minimum.
4. The memory LDO output should always be set equal to or lower than the output of the analog LDO. When lowering both LDOs (for example to go into PM8 under low supply conditions), first adjust the memory LDO and then the analog LDO. When raising the output of both LDOs, adjust the analog LDO before adjusting the memory LDO.
5. Output range represents the programmable output range, and does not reflect the minimum voltage under all conditions. Dropout when the input supply is close to the output setting is normal, and accounted for.
6. Analog peripheral specifications assume a 1.8 V output on the analog LDO.

Table 3.7. Internal Oscillators (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RTC0 Oscillator (RTC0OSC)						
Missing Clock Detector Trigger Frequency	f_{RTCMCD}		—	8	15	kHz
RTC External Input CMOS Clock Frequency	$f_{RTCEXTCLK}$		0	—	40	kHz
RTC Robust Duty Cycle Range	DC_{RTC}		25	—	55	%

Table 3.8. External Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency	f_{CMOS}		0*	—	50	MHz
External Crystal Frequency	f_{XTAL}		0.01	—	25	MHz
External Input CMOS Clock High Time	t_{CMOSH}		9	—	—	ns
External Input CMOS Clock Low Time	t_{CMOSL}		9	—	—	ns
Low Power Mode Charge Pump Supply Range (input from V_{BAT})	V_{BAT}		2.4	—	3.8	V
***Note:** Minimum of 10 kHz when debugging.						

Table 3.10. IDAC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static Performance						
Resolution	N_{bits}			10		Bits
Integral Nonlinearity	INL		—	±0.5	±2	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL		—	±0.5	±1	LSB
Output Compliance Range	V_{OCR}		—	—	V_{BAT} – 1.0	V
Full Scale Output Current	I_{OUT}	2 mA Range, T_A = 25 °C	1.98	2.046	2.1	mA
		1 mA Range, T_A = 25 °C	0.99	1.023	1.05	mA
		0.5 mA Range, T_A = 25 °C	491	511.5	525	µA
Offset Error	E_{OFF}		—	250	—	nA
Full Scale Error Tempco	TC_{FS}	2 mA Range	—	100	—	ppm/°C
VBAT Power Supply Rejection Ratio		2 mA Range	—	–220	—	ppm/V
Test Load Impedance (to V_{SS})	R_{TEST}		—	1	—	kΩ
Dynamic Performance						
Output Settling Time to 1/2 LSB		min output to max output	—	1.2	—	µs
Startup Time			—	3	—	µs

Table 3.11. ACCTR (Advanced Capture Counter) (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LC Comparator Positive Hysteresis Mode 3 (CPMD = 00)	HYS_{CP+}	CMPHYP = 00	—	1.37	—	mV
		CMPHYP = 01	—	3.8	—	mV
		CMPHYP = 10	—	7.8	—	mV
		CMPHYP = 11	—	15.6	—	mV
LC Comparator Negative Hysteresis Mode 3 (CPMD = 00)	HYS_{CP-}	CMPHYN = 00	—	1.37	—	mV
		CMPHYN = 01	—	–3.9	—	mV
		CMPHYN = 10	—	–7.9	—	mV
		CMPHYN = 11	—	–16	—	mV
LC Comparator Input Range (ACCTR0_LCIN pin)	V_{IN}		–0.25	—	V_{BAT} + 0.25	V
LC Comparator Common-Mode Rejection Ratio	$CMRR_{CP}$		—	75	—	dB
LC Comparator Power Supply Rejection Ratio	$PSRR_{CP}$		—	72	—	dB
LC Comparator Input Offset Voltage	V_{OFF}	T_A = 25 °C	–10	0	10	mV
LC Comparator Input Offset Tempco	TC_{OFF}		—	3.5	—	µV/°C
Reference DAC Offset Error	DAC_{EOFF}		–1	—	1	LSB
Reference DAC Full Scale Output	DAC_{FS}	Low Range	—	V_{IO}/8	—	V
		High Range	—	V_{IO}	—	V
Reference DAC Step Size	DAC_{LSB}	Low Range (48 steps)	—	V_{IO}/384	—	V
		High Range (64 steps)	—	V_{IO}/64	—	V
LC Oscillator Period	T_{LCOSC}		—	25	—	ns
LC Bias Output Impedance	R_{LCBIAS}	10 µA Load	—	1	—	kΩ
LC Bias Drive Strength	I_{LCBIAS}		—	—	2	mA
Pull-Up Resistor Tolerance	R_{TOL}	PUVAL[4:2] = 0 to 6	-15	—	15	%
		PUVAL[4:2] = 7	-10	—	10	%

4. Precision32™ SiM3L1xx System Overview

The SiM3L1xx Precision32™ devices are fully integrated, mixed-signal system-on-a-chip MCUs. Highlighted features are listed below. Refer to Table 5.1 for specific product feature selection and part ordering numbers.

- **Core:**
  - 32-bit ARM Cortex-M3 CPU.
  - 50 MHz maximum operating frequency.
  - Branch target cache and prefetch buffers to minimize wait states.
- **Memory:** 32–256 kB flash; in-system programmable, 8–32 kB SRAM configurable to retention mode in 4 kB blocks. Blocks configured to retention mode preserve state in the low power PM8 mode.
- **Power:**
  - Three adjustable low drop-out (LDO) regulators.
  - DC-DC buck converter allows dynamic voltage scaling for maximum efficiency (250 mW output).
  - Power-on reset circuit and brownout detectors.
  - Power Management Unit (PMU).
  - Specialized charge pump reduces power consumption in low power modes.
  - Process/Voltage/Temperature (PVT) Monitor.
  - Register state retention in lowest power mode.
- **I/O:** Up to 62 contiguous 5 V tolerant I/O pins and one flexible peripheral crossbar.
- **Clock Sources:**
  - Internal oscillator with PLL: 23–50 MHz with ± 1.5% accuracy in free-running mode.
  - Low-power internal oscillator: 20 MHz.
  - Low-frequency internal oscillator: 16.4 kHz.
  - External RTC crystal oscillator: 32.768 kHz.
  - External oscillator: Crystal, RC, C, CMOS clock.
- **Integrated LCD Controller (4x40).**
- **Data Peripherals:**
  - 10-Channel DMA Controller.
  - 3 x Data Transfer Managers.
  - 128/192/256-bit Hardware AES Encryption.
  - CRC with programmable 16-bit polynomial, one 32-bit polynomial, and bus snooping capability.
  - Encoder / Decoder.
- **Timers/Counters:**
  - 3 x 32-bit Timers.
  - 1 x Enhanced Programmable Counter Array (EPCA).
  - Real Time Clock (RTC0).
  - Low Power Timer.
  - Watchdog Timer.
  - Low Power Mode Advanced Capture Counter (ACCTR).
- **Communications Peripherals:**
  - 1 x USART with IrDA and ISO7816 SmartCard support.
  - 1 x UART that operates in low power mode (PM8).
  - 2 x SPIs.
  - 1 x I2C.
- **Analog:**
  - 1 x 12-Bit Analog-to-Digital Converter (SARADC).
  - 1 x 10-Bit Digital-to-Analog Converter (IDAC).
  - 2 x Low-Current Comparators (CMP).
- **On-Chip Debugging**

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillators, the SiM3L1xx devices are truly stand-alone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing non-volatile data storage and allowing field upgrades of the firmware. User firmware has complete control of all

- Supports synchronizing the regulator switching with the system clock.
- Automatically limits the peak inductor current if the load current rises beyond a safe limit.
- Automatically goes into bypass mode if the battery voltage cannot provide sufficient headroom.
- Sources current, but cannot sink current.

4.1.2. Three Low Dropout LDO Regulators (LDO0)

The SiM3L1xx devices include one LDO0 module with three low dropout regulators. Each of these regulators have independent switches to select the battery voltage or the output of the dc-dc converter as the input to each LDO, and an adjustable output voltage.

The LDOs consume little power and provide flexibility in choosing a power supply for the system. Each regulator can be independently adjusted between 0.8 and 1.9 V output.

4.1.3. Voltage Supply Monitor (VMON0)

The SiM3L1xx devices include a voltage supply monitor that can monitor the main supply voltage. This module includes the following features:

- Main supply “VBAT Low” (VBAT below the early warning threshold) notification.
- Holds the device in reset if the main VBAT supply drops below the VBAT Reset threshold.

The voltage supply monitor allows devices to function in known, safe operating conditions without the need for external hardware.

4.1.4. Power Management Unit (PMU)

The Power Management Unit on the SiM3L1xx manages the power systems of the device. It manages the power-up sequence during power on and the wake up sources for PM8. On power-up, the PMU ensures the core voltages are a proper value before core instruction execution begins.

The VDRV pin powers external circuitry from either the VBAT battery input voltage or the output of the dc-dc converter on VDC. The PMU includes an internal switch to select one of these sources for the VDRV pin.

The PMU has a specialized VBAT-divided-by-2 charge pump that can power some internal modules while in PM8 to save power.

The PMU module includes the following features:

- Provides the enable or disable for the analog power system, including the three LDO regulators.
- Up to 14 pin wake inputs can wake the device from Power Mode 8.
- The Low Power Timer, RTC0 (alarms and oscillator failure), Comparator 0, Advanced Capture Counter, LCD0 VBAT monitor, UART0, low power mode charge pump failure, and the RESET pin can also serve as wake sources for Power Mode 8.
- Controls which 4 kB RAM blocks are retained while in Power Mode 8.
- Provides a PMU_Asleep signal to a pin as an indicator that the device is in PM8.
- Specialized charge pump to reduce power consumption in PM8.

Provides control for the internal switch between VBAT and VDC to power the VDRV pin for external circuitry.

4.1.5. Device Power Modes

The SiM3L1xx devices feature seven low power modes in addition to normal operating mode. Several peripherals provide wake up sources for these low power modes, including the Low Power Timer (LPTIMER0), RTC0 (alarms and oscillator failure notification), Comparator 0 (CMP0), Advanced Capture Counter (ACCTR0), LCD VBAT monitor (LCD0), UART0, low power mode charge pump failure, and PMU Pin Wake.

In addition, all peripherals can have their clocks disabled to reduce power consumption whenever a peripheral is not being used using the clock control (CLKCTRL) registers.

4.1.5.1. Normal Mode (Power Mode 0) and Power Mode 4

Normal Mode and Power Mode 4 are fully operational modes with code executing from flash memory. PM4 is the same as Normal Mode, but with the clocks operating at a lower speed. This enables power to be conserved by reducing the LDO regulator outputs.

4.1.5.2. Power Mode 1 and Power Mode 5

Power Mode 1 and Power Mode 5 are fully operational modes with code executing from RAM. PM5 is the same as PM1, but with the clocks operating at a lower speed. This enables power to be conserved by reducing the LDO regulator outputs. Compared with the corresponding flash operational mode (Normal or PM4), the active power consumption of the device in these modes is reduced. Additionally, at higher speeds in PM1, the core throughput can also be increased because RAMdoesnot require additional wait states that reduce the instruction fetch speed.

4.1.5.3. Power Mode 2 and Power Mode 6

In Power Mode 2 and Power Mode 6, the core halts and the peripherals continue to run at the selected clock speed. PM6 is the same as PM2, but with the clocks operating at a lower speed. This enables power to be conserved by reducing the LDO regulator outputs. To place the device in PM2 or PM6, the core should execute a wait-for-interrupt (WFI) or wait-for-event (WFE) instruction. If the WFI instruction is called from an interrupt service routine, the interrupt that wakes the device from PM2 or PM6 must be of a sufficient priority to be recognized by the core. It is recommended to perform both a DSB (Data Synchronization Barrier) and an ISB (Instruction Syncronization Barrier) operation prior to the WFI to ensure all bus accesses complete. When operating from the LFOSC0, PM6 can achieve similar power consumption to PM3, but with faster wake times and the ability to wake on any interrupt.

4.1.5.4. Power Mode 3

In Power Mode 3 the core and peripheral clocks are halted. The available sources to wake from PM3 are controlled by the Power Management Unit (PMU). A special Fast Wake option allows the core to wake faster by keeping the LFOSC0 or RTC0 clock active. Because the current consumption of these blocks is minimal, it is recommended to use the fast wake option.

Before entering PM3, the DMA controller should be disabled, and the desired wake source(s) should be configured in the PMU. The SLEEPDEEP bit in the ARM System Control Register should be set, and the PMSEL bit in the CLKCTRL0_CONFIG register should be cleared to indicate that PM3 is the desired power mode. For fast wake, the core clocks (AHB and APB) should be configured to run from the LPOSC, and the PM3 Fast wake option and clock source should be selected in the PM3CN register.

The device will enter PM3 on a WFI or WFE instruction. If the WFI instruction is called from an interrupt service routine, the interrupt that wakes the device from PM3 must be of a sufficient priority to be recognized by the core. It is recommended to perform both a DSB (Data Synchronization Barrier) and an ISB (Instruction Synchronization Barrier) operation prior to the WFI to ensure all bus access is complete.

4.1.5.5. Power Mode 8

In Power Mode 8, the core and most peripherals are completely powered down, but all registers and selected RAM blocks retain their state. The LDO regulators are disabled, so all active circuitry operates directly from VBAT. Alternatively, the PMU has a specialized VBAT-divided-by-2 charge pump that can power some internal modules while in PM8 to save power. The fully operational functions in this mode are: LPTIMER0 , RTC0, UART0 running from RTC0TCLK, PMU Pin Wake, the advanced capture counter, and the LCD controller.

This mode provides the lowest power consumption for the device, but requires an appropriate wake up source or reset to exit. The available wake up or reset sources to wake from PM8 are controlled by the Power Management Unit (PMU). The available wake up sources are: Low Power Timer (LPTIMER0), RTC0 (alarms and oscillator failure notification), Comparator 0 (CMP0), advanced capture counter (ACCTR0), LCD VBAT monitor (LCD0), UART0, low power mode charge pump failure, and PMU Pin Wake. The available reset sources are: RESET pin, VBAT supply monitor, Comparator 0, Comparator 1, low power mode charge pump failure, RTC0 oscillator failure, or a PMU wake event.

Before entering PM8, the desired wake source(s) should be configured in the PMU. The SLEEPDEEP bit in the ARM System Control Register should be set, and the PMSEL bit in the CLKCTRL0_CONFIG register should be set to indicate that PM8 is the desired power mode.

The device will enter PM8 on a WFI or WFE instruction, and remain in PM8 until a reset configured by the PMU occurs. It is recommended to perform both a DSB (Data Synchronization Barrier) and an ISB (Instruction Synchronization Barrier) operation prior to the WFI to ensure all bus access is complete.

4.5. Data Peripherals

4.5.1. 10-Channel DMA Controller

The DMA facilitates autonomous peripheral operation, allowing the core to finish tasks more quickly without spending time polling or waiting for peripherals to interrupt. This helps reduce the overall power consumption of the system, as the device can spend more time in low-power modes.

The DMA controller has the following features:

- Utilizes ARM PrimeCell uDMA architecture.
- Implements 10 channels.
- DMA crossbar supports DTM0, DTM1, DTM2, SARADC0, IDAC0, I2C0, SPI0, SPI1, USART0, AES0, ENCDEC0, EPCA0, external pin triggers, and timers.
- Supports primary, alternate, and scatter-gather data structures to implement various types of transfers.
- Access allowed to all AHB and APB memory space.

4.5.2. Data Transfer Managers (DTM0, DTM1, DTM2)

The Data Transfer Manager is a module that collects DMA request signals from various peripherals and generates a series of master DMA requests based on a state-driven configuration. This master request drives a set of DMA channels to perform functions such as assembling and transferring communication packets to external devices. This capability saves power by allowing the core to remain in a low power mode during complex transfer operations. A combination of simple and peripheral scatter-gather DMA configurations can be used to perform complex operations while reducing memory requirements.

The DTM acts as a side channel for the peripheral's DMA control signals. When active, it manages the DMA control signals for the peripherals. When the DTMn module is inactive, the peripherals communicate directly to the DMA module.

The DTMn module has the following features:

- State descriptions stored in RAM with up to 15 states supported per module.
- Supports up to 15 source peripherals and up to 15 destination peripherals per module, in addition to memory or peripherals that do not require a data request.
- Includes error detection and an optional transfer timeout.
- Includes notifications for state transitions.

4.5.3. 128/192/256-bit Hardware AES Encryption (AES0)

The basic AES block cipher is implemented in hardware. The integrated hardware support for Cipher Block Chaining (CBC) and Counter (CTR) algorithms results in identical performance, memory bandwidth, and memory footprint between the most basic Electronic Codebook (ECB) algorithm and these more complex algorithms. This hardware accelerator translates to more core bandwidth available for other functions or a power savings for low-power applications.

The AES module includes the following features:

- Operates on 4-word (16-byte) blocks.
- Supports key sizes of 128, 192, and 256 bits for both encryption and decryption.
- Generates the round key for decryption operations.
- All cipher operations can be performed without any firmware intervention for multiple 4-word blocks (up to 32 kB).
- Support for various chained and stream-ciphering configurations with XOR paths on both the input and output.
- Internal 4-word FIFOs to facilitate DMA operations.
- Integrated key storage.
- Hardware acceleration for Electronic Codebook (ECB), Cipher-Block Chaining (CBC), and Counter (CTR) algorithms utilizing integrated counterblock generation and previous-block caching.

- Multiple loop-back modes supported.
- Multi-processor communications support.
- Operates at 9600, 4800, 2400, or 1200 baud in Power Mode 8.

4.7.3. SPI (SPI0, SPI1)

SPI is a 3- or 4-wire communication interface that includes a clock, input data, output data, and an optional select signal.

The SPI0 and SPI1 modules include the following features:

- Supports 3- or 4-wire master or slave modes.
- Supports up to 10 MHz clock in master mode and 5 MHz clock in slave mode.
- Support for all clock phase and slave select (NSS) polarity modes.
- 16-bit programmable clock rate.
- Programmable MSB-first or LSB-first shifting.
- 8-byte FIFO buffers for both transmit and receive data paths to support high speed transfers.
- Support for multiple masters on the same data lines.

In addition, the SPI modules include several features to support autonomous DMA transfers:

- Hardware NSS control.
- Programmable FIFO threshold levels.
- Configurable FIFO data widths.
- Master or slave hardware flow control for the MISO and MOSI signals.

SPI1 is on fixed pins and supports additional flow control options using a fixed input (SPI1CTS). Neither SPI1 nor the flow control input are on the crossbar.

4.7.4. I2C (I2C0)

The I2C interface is a two-wire, bi-directional serial bus. The clock and data signals operate in open-drain mode with external pull-ups to support automatic bus arbitration.

Reads and writes to the interface are byte oriented with the I2C interface autonomously controlling the serial transfer of the data. Data can be transferred at up to 1/8th of the APB clock as a master or slave, which can be faster than allowed by the I2C specification, depending on the clock source used. A method of extending the clock-low duration is available to accommodate devices with different speed capabilities on the same bus.

The I2C interface may operate as a master and/or slave, and may function on a bus with multiple masters. The I2C provides control of SDA (serial data), SCL (serial clock) generation and synchronization, arbitration logic, and start/stop control and generation.

The I2C0 module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds.
- Can operate down to APB clock divided by 32768 or up to APB clock divided by 8.
- Support for master, slave, and multi-master modes.
- Hardware synchronization and arbitration for multi-master mode.
- Clock low extending (clock stretching) to interface with faster masters.
- Hardware support for 7-bit slave and general call address recognition.
- Firmware support for 10-bit slave address decoding.
- Ability to disable all slave states.
- Programmable clock high and low period.
- Programmable data setup/hold times.
- Spike suppression up to 2 times the APB period.

5. Ordering Information

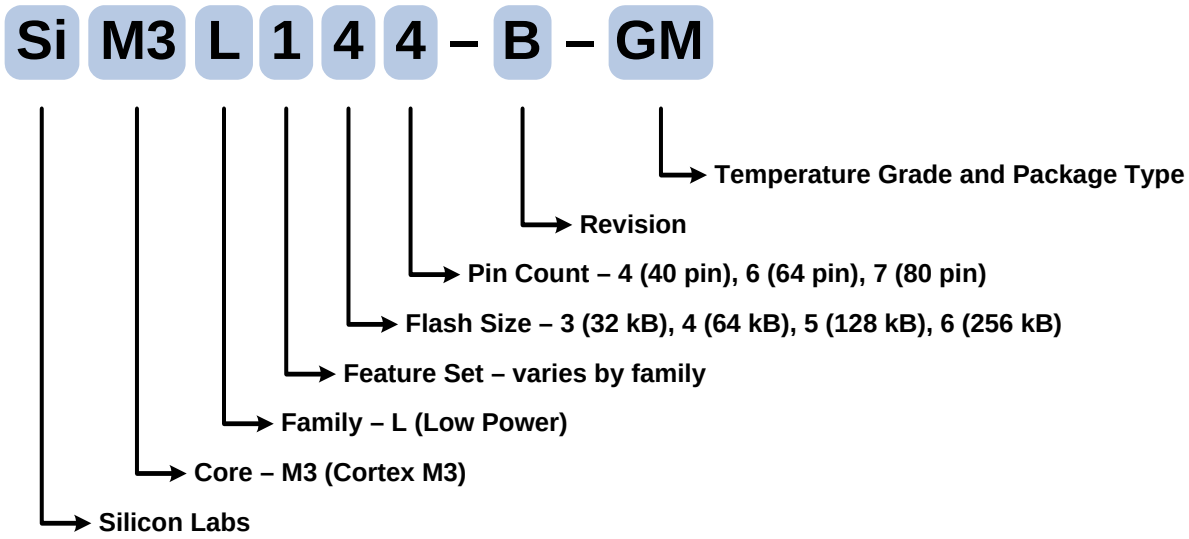

Figure 5.1. SiM3L1xx Part Numbering

All devices in the SiM3L1xx family have the following features:

- **Core:** ARM Cortex-M3 with maximum operating frequency of 50 MHz.
- **PLL.**
- **10-Channel DMA Controller.**
- **128/192/256-bit AES.**
- **16/32-bit CRC.**
- **Encoder/Decoder.**
- **DC-DC Buck Converter.**
- **Timers:** 3 x 32-bit (6 x 16-bit).
- **Real-Time Clock.**
- **Low-Power Timer.**
- **PCA:** 1 x 6 channels (Enhanced)
- **ADC:** 12-bit 250 ksps (10-bit 1 Msps) SAR.
- **DAC:** 10-bit IDAC.
- **Temperature Sensor.**
- **Internal VREF.**
- **Comparator:** 2 x low current.
- **Serial Buses:** 2 x USART, 2 x SPI, 1 x I2C

Additionally, all devices in the SiM3L1xx family include the low power mode advanced capture counter (ACCTR0), though the smaller packages (SiM3L1x4) only support some of the external inputs and outputs.

6. Pin Definitions

6.1. SiM3L1x7 Pin Definitions

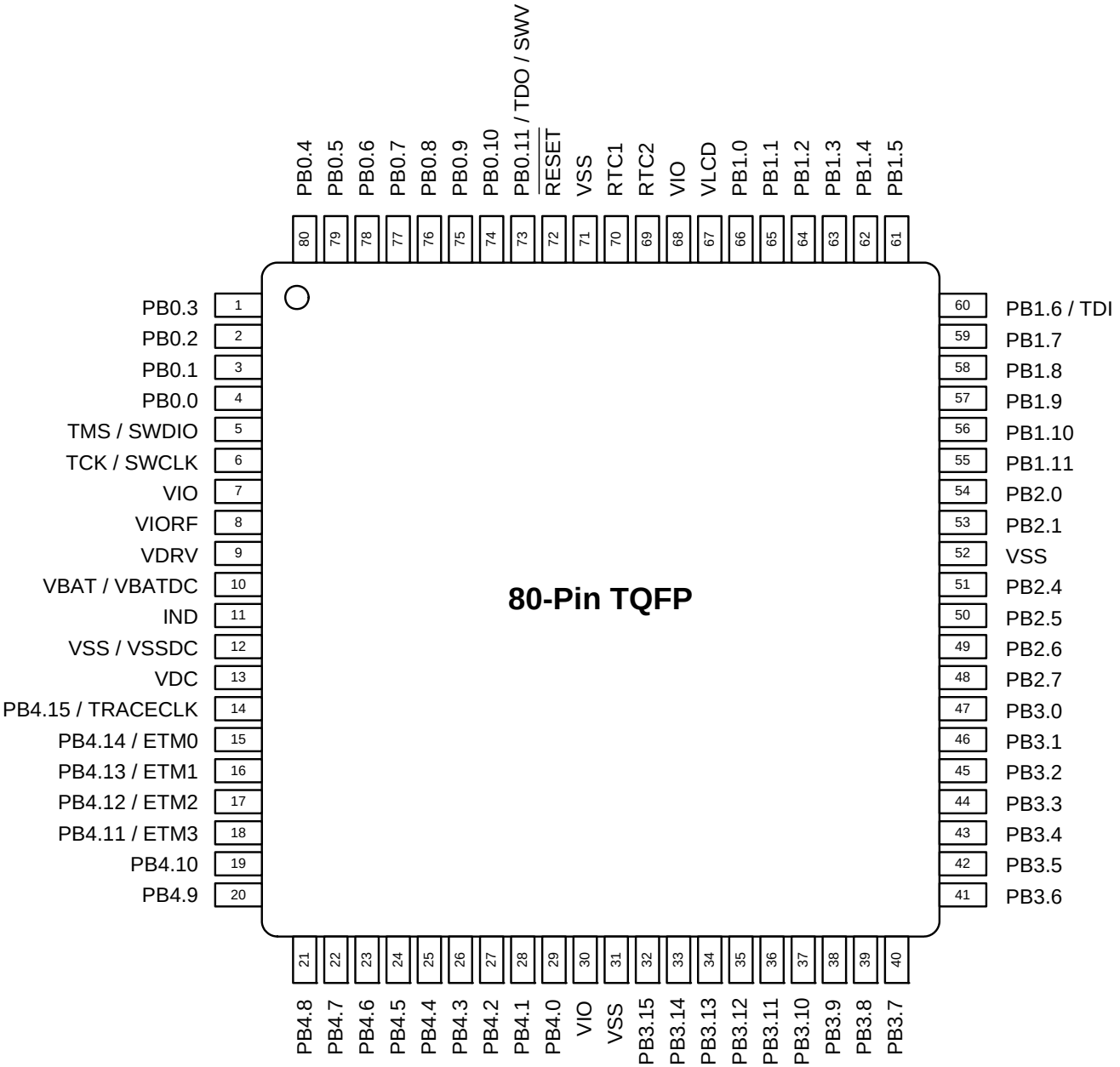

Figure 6.1. SiM3L1x7-GQ Pinout

Table 6.2. Pin Definitions and Alternate Functions for SiM3L1x6 (Continued)

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB4.0	Standard I/O	24	VIO		✓	COM0.1			
PB4.1	Standard I/O	23	VIO		✓	COM0.0			
PB4.2	Standard I/O	22	VIO		✓	LCD0.10			ADC0.19
PB4.3	Standard I/O	21	VIO		✓	LCD0.9			
PB4.4	Standard I/O	20	VIO		✓	LCD0.8			
PB4.5	Standard I/O	19	VIO		✓	LCD0.7			
PB4.6	Standard I/O	18	VIO		✓	LCD0.6		PMU_Asleep	
PB4.7	Standard I/O	17	VIO		✓	LCD0.5			
PB4.8/ETM3	Standard I/O / ETM	16	VIO		✓	LCD0.4			
PB4.9/ETM2	Standard I/O / ETM	15	VIO		✓	LCD0.3			
PB4.10/ ETM1	Standard I/O / ETM	14	VIO		✓	LCD0.2			
PB4.11/ ETM0	Standard I/O / ETM	13	VIO		✓	LCD0.1			
PB4.12/ TRACECLK	Standard I/O / ETM	12	VIO		✓	LCD0.0			

Table 6.3. Pin Definitions and Alternate Functions for SiM3L1x4 (Continued)

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB2.1	Standard I/O	28	VIORF	XBR0	✓		LPT0T9 INT1.1 WAKE.13 VIORFCLK	ADC0.3 CMP0N.4
PB2.2	Standard I/O	27	VIORF	XBR0	✓		LPT0T10 INT1.2 WAKE.14	ADC0.4 CMP1P.4
PB2.3	Standard I/O	26	VIORF	XBR0	✓		LPT0T11 INT1.3 WAKE.15	ADC0.5 CMP1N.4
PB2.4	Standard I/O	24	VIORF	XBR0	✓		LPT0T12 INT1.4 SPI1_SCLK	ADC0.6 CMP0P.5
PB2.5	Standard I/O	23	VIORF	XBR0	✓		LPT0T13 INT1.5 SPI1_MISO	ADC0.7 CMP0N.5
PB2.6	Standard I/O	22	VIORF	XBR0	✓		LPT0T14 INT1.6 SPI1_MOSI	ADC0.8 CMP1P.5
PB2.7	Standard I/O	21	VIORF	XBR0	✓		INT1.7 SPI1_NSS	ADC0.9 CMP1N.5
PB3.0	Standard I/O	20	VIO	XBR0	✓		INT1.8	CMP0N.7
PB3.1	Standard I/O	19	VIO	XBR0	✓		INT1.9	CMP1P.7
PB3.2	Standard I/O	18	VIO	XBR0	✓		INT1.10	CMP1N.7
PB3.3	Standard I/O	17	VIO	XBR0	✓		INT1.11	ADC0.10
PB3.4	Standard I/O	16	VIO	XBR0	✓		INT1.12	ADC0.11
PB3.5	Standard I/O	15	VIO	XBR0	✓		INT1.13	ADC0.12

6.4. TQFP-80 Package Specifications

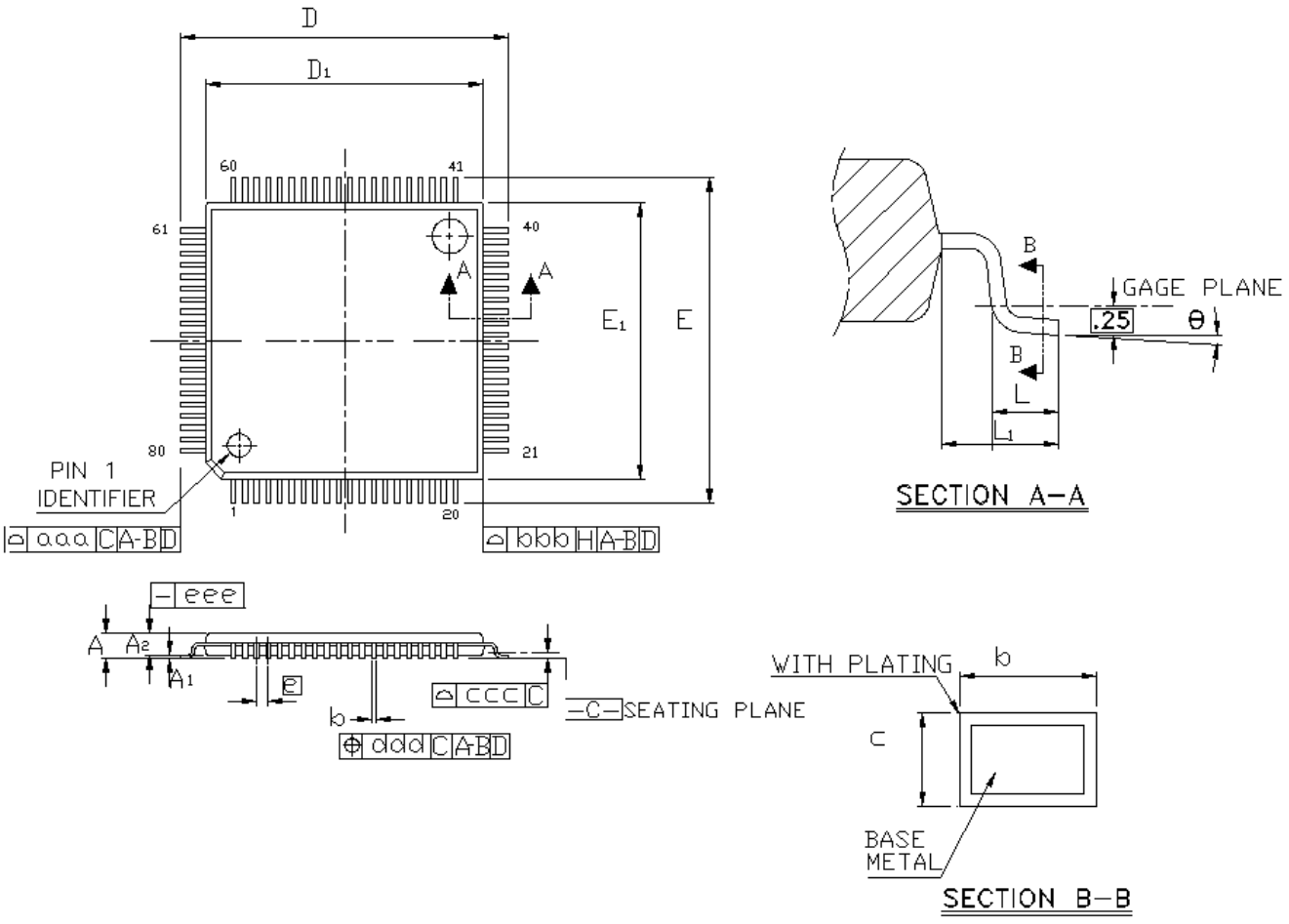

Figure 6.5. TQFP-80 Package Drawing

6.5. QFN-64 Package Specifications

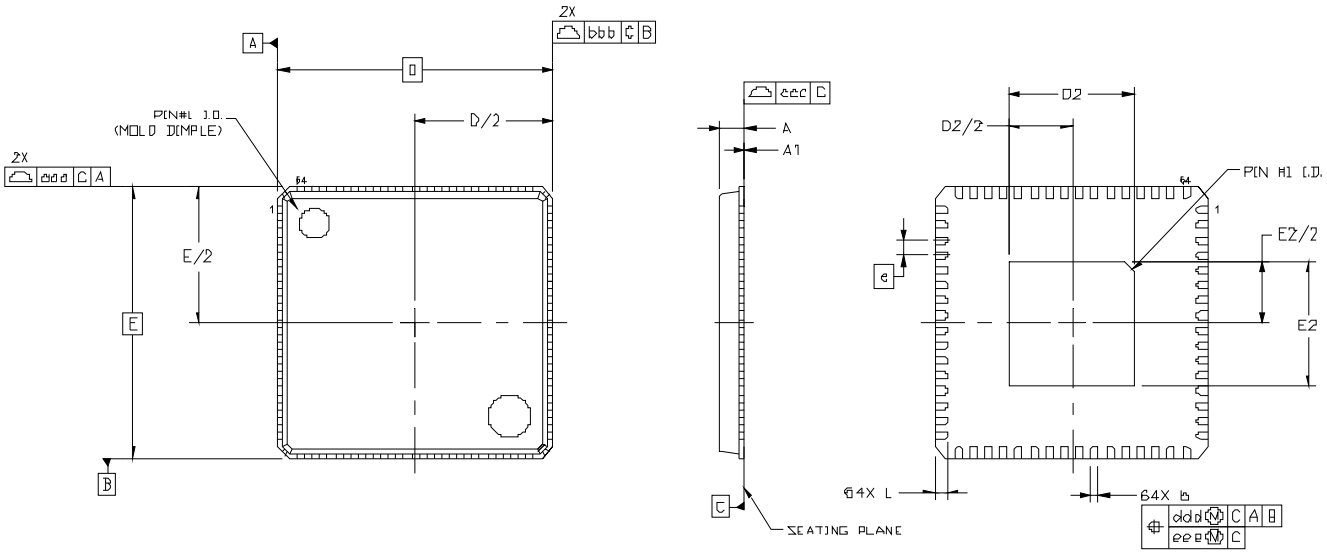

Figure 6.7. QFN-64 Package Drawing

Table 6.6. QFN-64 Package Dimensions

Dimension	Min	Nominal	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		9.00 BSC	
D2	3.95	4.10	4.25
e		0.50 BSC	
E		9.00 BSC	
E2	3.95	4.10	4.25
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

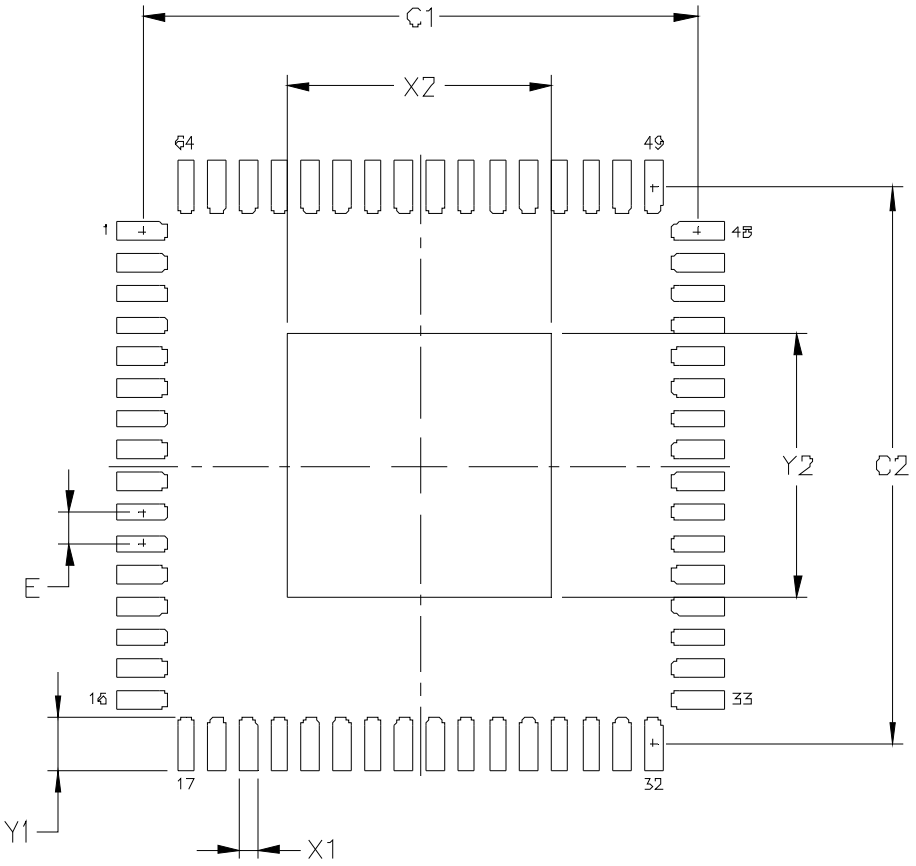

Figure 6.8. QFN-64 Landing Diagram

Table 6.7. QFN-64 Landing Diagram Dimensions

Dimension	mm
C1	8.90
C2	8.90
E	0.50
X1	0.30
Y1	0.85
X2	4.25
Y2	4.25

Notes:
1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

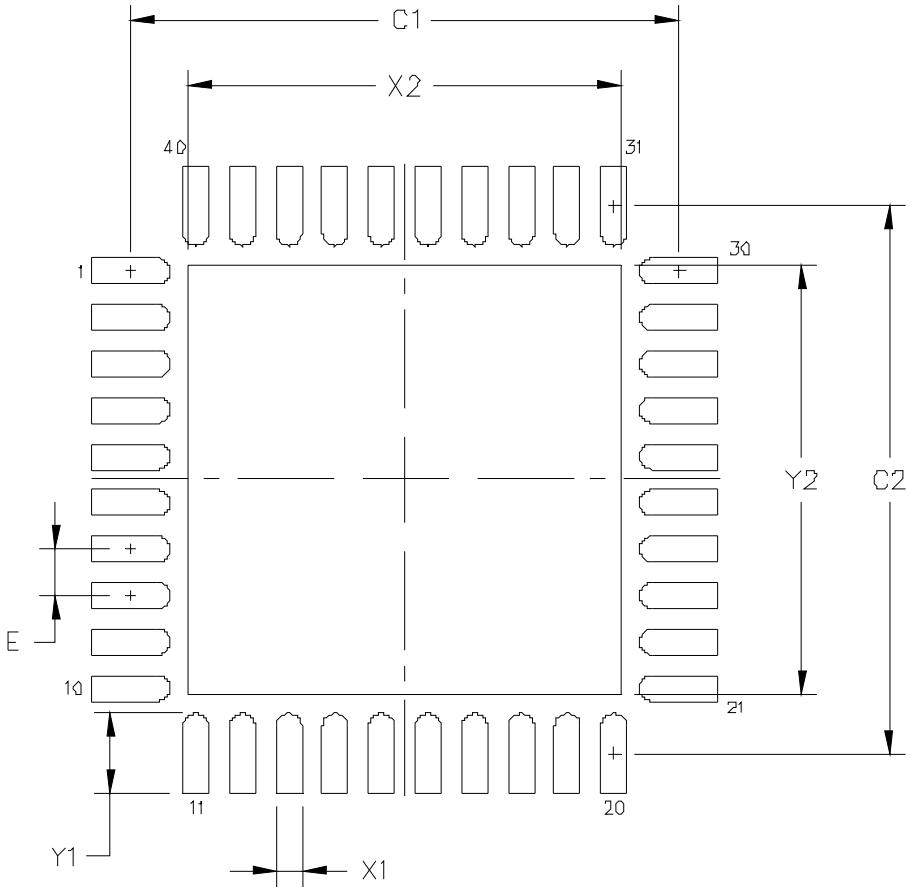

Figure 6.12. QFN-40 Landing Diagram

Table 6.11. QFN-40 Landing Diagram Dimensions

Dimension	mm
C1	5.90
C2	5.90
E	0.50
X1	0.30
Y1	0.85
X2	4.65
Y2	4.65

Notes:
1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

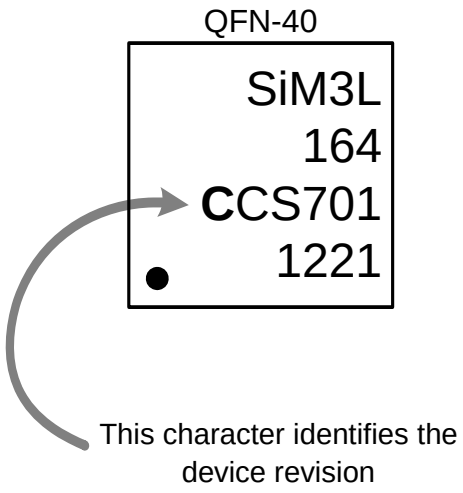

Figure 7.3. SiM3L1x4-GM Revision Information

Document Change List

Revision 0.5 to Revision 1.0

- Updated Electrical Specifications Tables with latest characterization data and production test limits.
- Added missing signal ACCTR0_LCPUL1 to Table 6.2, “Pin Definitions and Alternate Functions for SiM3L1x6,” on page 64.
- Removed ACCTR0_LCIN1 and ACCTR0_STOP0/1 signals from Table 6.3, “Pin Definitions and Alternate Functions for SiM3L1x4,” on page 70.
- Updated Figure 6.8, “TFBGA-80 Package Drawing,” on page 79.

Revision 1.0 to Revision 1.1

- Removed all references to BGA-80 and the parts SiM3L167-C-GL and SiM3L157-C-GL.