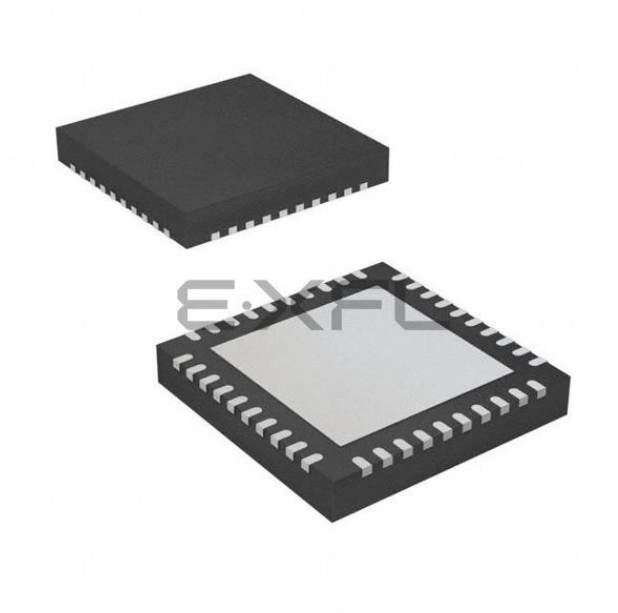

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	28
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 20x10/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/sim3l144-c-gm

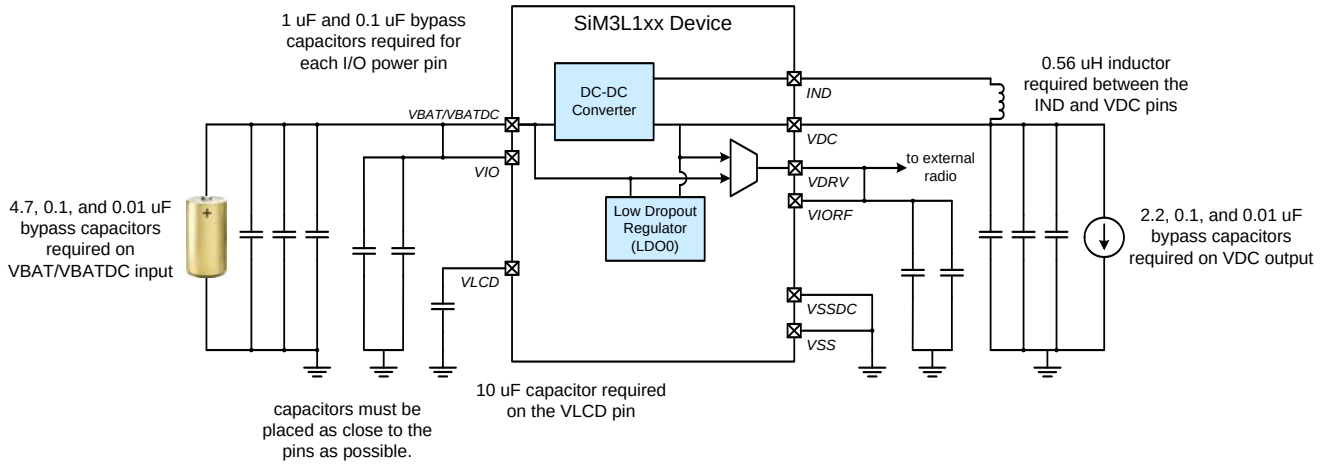

Figure 2.3. Connection Diagram with External Radio Device

Figure 2.4 shows a typical connection diagram for the power pins of the SiM3L1xx devices when the dc-dc buck converter is used and the I/O are powered separately.

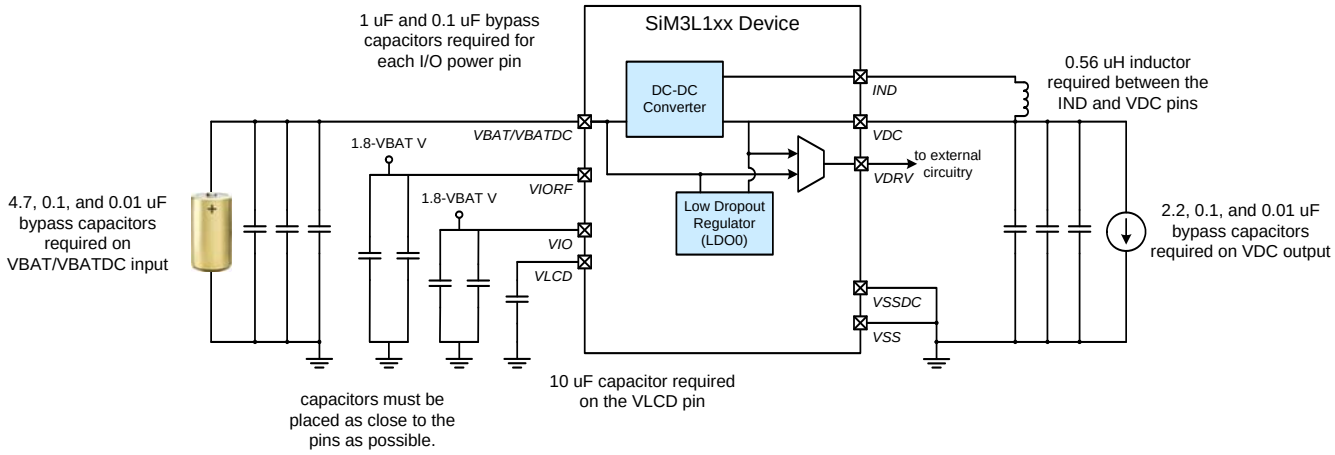

Figure 2.4. Connection Diagram with DC-DC Converter Used and I/O Powered Separately

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 1[1,2,3,4]—Full speed with code executing from RAM, peripheral clocks ON	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	13.4	16.6	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	4.7	—	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	810	—	µA
Power Mode 1[1,2,3,4]—Full speed with code executing from RAM, peripheral clocks OFF	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	9.4	12.5	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	3.3	—	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	630	—	µA
Power Mode 1[1,2,3,4]—Full speed with code executing from RAM, LDOs powered by dc-dc at 1.9 V, peripheral clocks OFF	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz V_{BAT} = 3.3 V	—	7.05	—	mA
		F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz V_{BAT} = 3.8 V	—	6.3	—	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz V_{BAT} = 3.3 V	—	2.75	—	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz V_{BAT} = 3.8 V	—	2.6	—	mA
Power Mode 2[1,2,3,4,5]—Core halted with peripheral clocks ON	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	7.6	11.3	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	2.75	—	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	575	—	µA

Notes:

1. Currents are additive. For example, where I_{BAT} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded I_{VIO} is included in all I_{BAT} PM8 production test measurements.

Table 3.5. On-Chip Regulators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC-DC Buck Converter						
Input Voltage Range	V_{DCIN}		1.8	—	3.8	V
Input Supply to Output Voltage Differential (for regulation)	V_{DCREG}		0.45	—	—	V
Output Voltage Range	V_{DCOUT}		1.25	—	3.8	V
Output Voltage Accuracy	V_{DCACC}		—	±25	—	mV
Output Current	I_{DCOUT}		—	—	90	mA
Inductor Value[1]	L_{DC}		0.47	0.56	0.68	µH
Inductor Current Rating	I_{LDC}	I_{load} < 50 mA	450	—	—	mA
		I_{load} > 50 mA	550	—	—	mA
Output Capacitor Value	C_{DCOUT}		1	2.2	10	µF
Input Capacitor Value[2]	C_{DCIN}		—	4.7	—	µF
Load Regulation	R_{load}		—	0.03	—	mV/mA
Maximum DC Load Current During Startup	I_{DCMAX}		—	—	5	mA
Switching Clock Frequency	F_{DCCLK}		1.9	2.9	3.8	MHz
Local Oscillator Frequency	F_{DCOSC}		2.4	2.9	3.4	MHz
LDO Regulators						
Input Voltage Range[3]	V_{LDOIN}	Sourced from VBAT	1.8	—	3.8	V
		Sourced from VDC	1.9	—	3.8	V
Output Voltage Range[4]	V_{LDO}		0.8	—	1.9	V
LDO Output Voltage Accuracy	V_{LDOACC}		—	±25	—	mV
Output Settings in PM8 (All LDOs)	V_{LDO}	1.8 V ≤ V_{BAT} ≤ 2.9 V	1.5			V
		1.95 V ≤ V_{BAT} ≤ 3.5 V	1.8			V
		2.0 V ≤ V_{BAT} ≤ 3.8 V	1.9			V

Notes:

1. See reference manual for recommended inductors.
2. Recommended: X7R or X5R ceramic capacitors with low ESR. Example: Murata GRM21BR71C225K with ESR < 10 mΩ (@ frequency > 1 MHz).
3. Input voltage specification accounts for the internal LDO dropout voltage under the maximum load condition to ensure that the LDO output voltage will remain at a valid level as long as V_{LDOIN} is at or above the specified minimum.
4. The memory LDO output should always be set equal to or lower than the output of the analog LDO. When lowering both LDOs (for example to go into PM8 under low supply conditions), first adjust the memory LDO and then the analog LDO. When raising the output of both LDOs, adjust the analog LDO before adjusting the memory LDO.
5. Output range represents the programmable output range, and does not reflect the minimum voltage under all conditions. Dropout when the input supply is close to the output setting is normal, and accounted for.
6. Analog peripheral specifications assume a 1.8 V output on the analog LDO.

Table 3.7. Internal Oscillators (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RTC0 Oscillator (RTC0OSC)						
Missing Clock Detector Trigger Frequency	f_{RTCMCD}		—	8	15	kHz
RTC External Input CMOS Clock Frequency	$f_{RTCEXTCLK}$		0	—	40	kHz
RTC Robust Duty Cycle Range	DC_{RTC}		25	—	55	%

Table 3.8. External Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency	f_{CMOS}		0*	—	50	MHz
External Crystal Frequency	f_{XTAL}		0.01	—	25	MHz
External Input CMOS Clock High Time	t_{CMOSH}		9	—	—	ns
External Input CMOS Clock Low Time	t_{CMOSL}		9	—	—	ns
Low Power Mode Charge Pump Supply Range (input from V_{BAT})	V_{BAT}		2.4	—	3.8	V
***Note:** Minimum of 10 kHz when debugging.						

Table 3.10. IDAC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static Performance						
Resolution	N_{bits}			10		Bits
Integral Nonlinearity	INL		—	±0.5	±2	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL		—	±0.5	±1	LSB
Output Compliance Range	V_{OCR}		—	—	V_{BAT} – 1.0	V
Full Scale Output Current	I_{OUT}	2 mA Range, T_A = 25 °C	1.98	2.046	2.1	mA
		1 mA Range, T_A = 25 °C	0.99	1.023	1.05	mA
		0.5 mA Range, T_A = 25 °C	491	511.5	525	µA
Offset Error	E_{OFF}		—	250	—	nA
Full Scale Error Tempco	TC_{FS}	2 mA Range	—	100	—	ppm/°C
VBAT Power Supply Rejection Ratio		2 mA Range	—	–220	—	ppm/V
Test Load Impedance (to V_{SS})	R_{TEST}		—	1	—	kΩ
Dynamic Performance						
Output Settling Time to 1/2 LSB		min output to max output	—	1.2	—	µs
Startup Time			—	3	—	µs

4. Precision32™ SiM3L1xx System Overview

The SiM3L1xx Precision32™ devices are fully integrated, mixed-signal system-on-a-chip MCUs. Highlighted features are listed below. Refer to Table 5.1 for specific product feature selection and part ordering numbers.

- **Core:**
  - 32-bit ARM Cortex-M3 CPU.
  - 50 MHz maximum operating frequency.
  - Branch target cache and prefetch buffers to minimize wait states.
- **Memory:** 32–256 kB flash; in-system programmable, 8–32 kB SRAM configurable to retention mode in 4 kB blocks. Blocks configured to retention mode preserve state in the low power PM8 mode.
- **Power:**
  - Three adjustable low drop-out (LDO) regulators.
  - DC-DC buck converter allows dynamic voltage scaling for maximum efficiency (250 mW output).
  - Power-on reset circuit and brownout detectors.
  - Power Management Unit (PMU).
  - Specialized charge pump reduces power consumption in low power modes.
  - Process/Voltage/Temperature (PVT) Monitor.
  - Register state retention in lowest power mode.
- **I/O:** Up to 62 contiguous 5 V tolerant I/O pins and one flexible peripheral crossbar.
- **Clock Sources:**
  - Internal oscillator with PLL: 23–50 MHz with ± 1.5% accuracy in free-running mode.
  - Low-power internal oscillator: 20 MHz.
  - Low-frequency internal oscillator: 16.4 kHz.
  - External RTC crystal oscillator: 32.768 kHz.
  - External oscillator: Crystal, RC, C, CMOS clock.
- **Integrated LCD Controller (4x40).**
- **Data Peripherals:**
  - 10-Channel DMA Controller.
  - 3 x Data Transfer Managers.
  - 128/192/256-bit Hardware AES Encryption.
  - CRC with programmable 16-bit polynomial, one 32-bit polynomial, and bus snooping capability.
  - Encoder / Decoder.
- **Timers/Counters:**
  - 3 x 32-bit Timers.
  - 1 x Enhanced Programmable Counter Array (EPCA).
  - Real Time Clock (RTC0).
  - Low Power Timer.
  - Watchdog Timer.
  - Low Power Mode Advanced Capture Counter (ACCTR).
- **Communications Peripherals:**
  - 1 x USART with IrDA and ISO7816 SmartCard support.
  - 1 x UART that operates in low power mode (PM8).
  - 2 x SPIs.
  - 1 x I2C.
- **Analog:**
  - 1 x 12-Bit Analog-to-Digital Converter (SARADC).
  - 1 x 10-Bit Digital-to-Analog Converter (IDAC).
  - 2 x Low-Current Comparators (CMP).
- **On-Chip Debugging**

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillators, the SiM3L1xx devices are truly stand-alone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing non-volatile data storage and allowing field upgrades of the firmware. User firmware has complete control of all

4.3. Clocking

The SiM3L1xx devices have two system clocks: AHB and APB. The AHB clock services memory peripherals and is derived from one of seven sources: the RTC timer clock (RTC0TCLK), the Low Frequency Oscillator, the Low Power Oscillator, the divided Low Power Oscillator, the External Oscillator, the PLL0 Oscillator, and the VIORFCLK pin input. In addition, a divider for the AHB clock provides flexible clock options for the device. The APB clock services data peripherals and is synchronized with the AHB clock. The APB clock can be equal to the AHB clock or set to the AHB clock divided by two.

The Clock Control module on SiM3L1xx devices allows the AHB and APB clocks to be turned off to unused peripherals to save system power. Any registers in a peripheral with disabled clocks will be unable to be accessed until the clocks are enabled. Most peripherals have clocks off by default after a power-on reset.

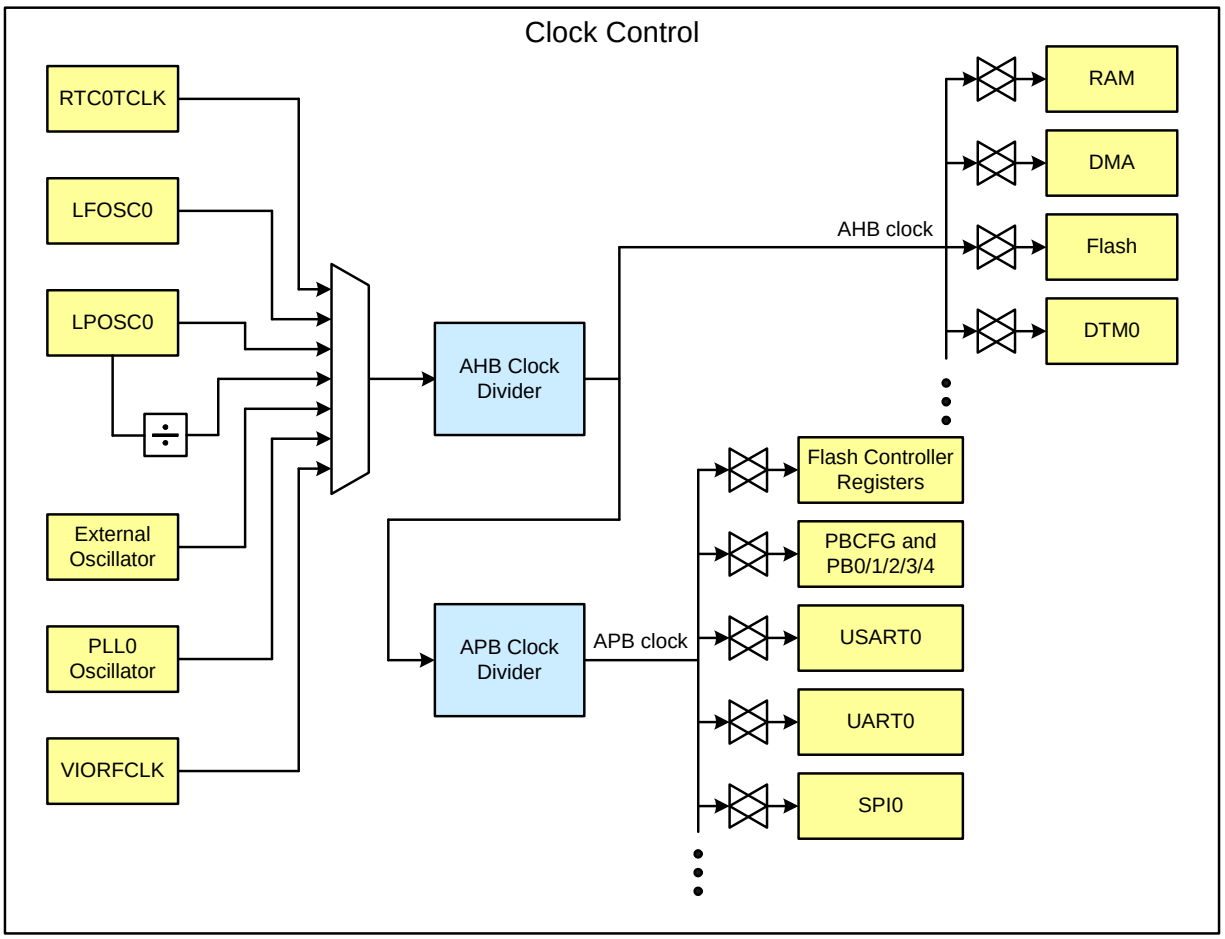

Figure 4.3. SiM3L1xx Clocking

4.4. Integrated LCD Controller (LCD0)

SiM3L1xx devices contain an LCD segment driver and on-chip bias generation that supports static, 2-mux, 3-mux and 4-mux LCDs with 1/2 or 1/3 bias. The on-chip charge pump with programmable output voltage allows software contrast control which is independent of the supply voltage. LCD timing is derived from the RTC timer clock (RTC0TCLK) to allow precise control over the refresh rate.

The SiM3L1xx devices use registers to store the enabled/disabled state of individual LCD segments. All LCD waveforms are generated on-chip based on the contents of these registers with flexible waveform control to reduce power consumption wherever possible. An LCD blinking function is also supported on a subset of LCD segments.

The LCD0 module has the following features:

- Up to 40 segment pins and 4 common pins.
- Supports LCDs with 1/2 or 1/3 bias.
- Includes an on-chip charge pump with programmable output that allows firmware to control the contrast independent of the supply voltage.
- The RTC timer clock (RTC0TCLK) determines the LCD timing and refresh rate.
- All LCD waveforms are generated on-chip based on the contents of the LCD0 registers with flexible waveform control.
- LCD segments can be placed in a discharge state for a configurable number of RTC clock cycles before switching to the next state to reduce power consumption due to display loading.
- Includes a VBAT monitor that can serve as a wakeup source for Power Mode 8.
- Supports four hardware auto-contrast modes: bypass, constant, minimum, and auto-bypass.
- Supports hardware blinking for up to 8 segments.

- Multiple loop-back modes supported.
- Multi-processor communications support.
- Operates at 9600, 4800, 2400, or 1200 baud in Power Mode 8.

4.7.3. SPI (SPI0, SPI1)

SPI is a 3- or 4-wire communication interface that includes a clock, input data, output data, and an optional select signal.

The SPI0 and SPI1 modules include the following features:

- Supports 3- or 4-wire master or slave modes.
- Supports up to 10 MHz clock in master mode and 5 MHz clock in slave mode.
- Support for all clock phase and slave select (NSS) polarity modes.
- 16-bit programmable clock rate.
- Programmable MSB-first or LSB-first shifting.
- 8-byte FIFO buffers for both transmit and receive data paths to support high speed transfers.
- Support for multiple masters on the same data lines.

In addition, the SPI modules include several features to support autonomous DMA transfers:

- Hardware NSS control.
- Programmable FIFO threshold levels.
- Configurable FIFO data widths.
- Master or slave hardware flow control for the MISO and MOSI signals.

SPI1 is on fixed pins and supports additional flow control options using a fixed input (SPI1CTS). Neither SPI1 nor the flow control input are on the crossbar.

4.7.4. I2C (I2C0)

The I2C interface is a two-wire, bi-directional serial bus. The clock and data signals operate in open-drain mode with external pull-ups to support automatic bus arbitration.

Reads and writes to the interface are byte oriented with the I2C interface autonomously controlling the serial transfer of the data. Data can be transferred at up to 1/8th of the APB clock as a master or slave, which can be faster than allowed by the I2C specification, depending on the clock source used. A method of extending the clock-low duration is available to accommodate devices with different speed capabilities on the same bus.

The I2C interface may operate as a master and/or slave, and may function on a bus with multiple masters. The I2C provides control of SDA (serial data), SCL (serial clock) generation and synchronization, arbitration logic, and start/stop control and generation.

The I2C0 module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds.
- Can operate down to APB clock divided by 32768 or up to APB clock divided by 8.
- Support for master, slave, and multi-master modes.
- Hardware synchronization and arbitration for multi-master mode.
- Clock low extending (clock stretching) to interface with faster masters.
- Hardware support for 7-bit slave and general call address recognition.
- Firmware support for 10-bit slave address decoding.
- Ability to disable all slave states.
- Programmable clock high and low period.
- Programmable data setup/hold times.
- Spike suppression up to 2 times the APB period.

4.8. Analog

4.8.1. 12-Bit Analog-to-Digital Converter (SARADC0)

The SARADC0 module on SiM3L1xx devices implements the Successive Approximation Register (SAR) ADC architecture. The key features of the module are as follows:

- Single-ended 12-bit and 10-bit modes.
- Supports an output update rate of 250 k samples per second in 12-bit mode or 1 M samples per second in 10-bit mode.
- Operation in low power modes at lower conversion speeds.
- Selectable asynchronous hardware conversion trigger with hardware channel select.
- DC offset cancellation.
- Automatic result notification with multiple programmable thresholds.
- Support for Burst Mode, which produces one set of accumulated data per conversion-start trigger with programmable power-on settling and tracking time.
- Non-burst mode operation can also automatically accumulate multiple conversions, but a conversion start is required for each conversion.
- Conversion complete, multiple conversion complete, and FIFO overflow and underflow flags and interrupts supported.
- Flexible output data formatting.
- Sequencer allows up to eight sources to be automatically scanned using one of four channel characteristic profiles without software intervention.
- Eight-word conversion data FIFO for DMA operations.
- Includes two internal references (1.65 V fast-settling, 1.2/2.4 V precision), support for an external reference, and support for an external signal ground.

4.8.2. 10-Bit Digital-to-Analog Converter (IDAC0)

The IDAC module takes a digital value as an input and outputs a proportional constant current on a pin. The IDAC module includes the following features:

- 10-bit current DAC with support for four timer, up to seven external I/O and on demand output update triggers.
- Ability to update on rising, falling, or both edges for any of the external I/O trigger sources.
- Supports an output update rate greater than 600 k samples per second.
- Support for three full-scale output modes: 0.5 mA, 1.0 mA and 2.0 mA.
- Four-word FIFO to aid with high-speed waveform generation or DMA interactions.
- Individual FIFO overrun, underrun, and went-empty interrupt status sources.
- Support for multiple data packing formats, including: single 10-bit sample per word, dual 10-bit samples per word, or four 8-bit samples per word.
- Support for left- and right-justified data.

4.8.3. Low Current Comparators (CMP0, CMP1)

The Comparators take two analog input voltages and output the relationship between these voltages (less than or greater than) as a digital signal. The low power comparator module includes the following features:

- Multiple sources for the positive and negative inputs, including VBAT, VREF, and 8 I/O pins.
- Two outputs available: a digital synchronous latched output and a digital asynchronous raw output.
- Programmable hysteresis and response time.
- Falling or rising edge interrupt options on the comparator output.
- 6-bit programmable reference divider.

5. Ordering Information

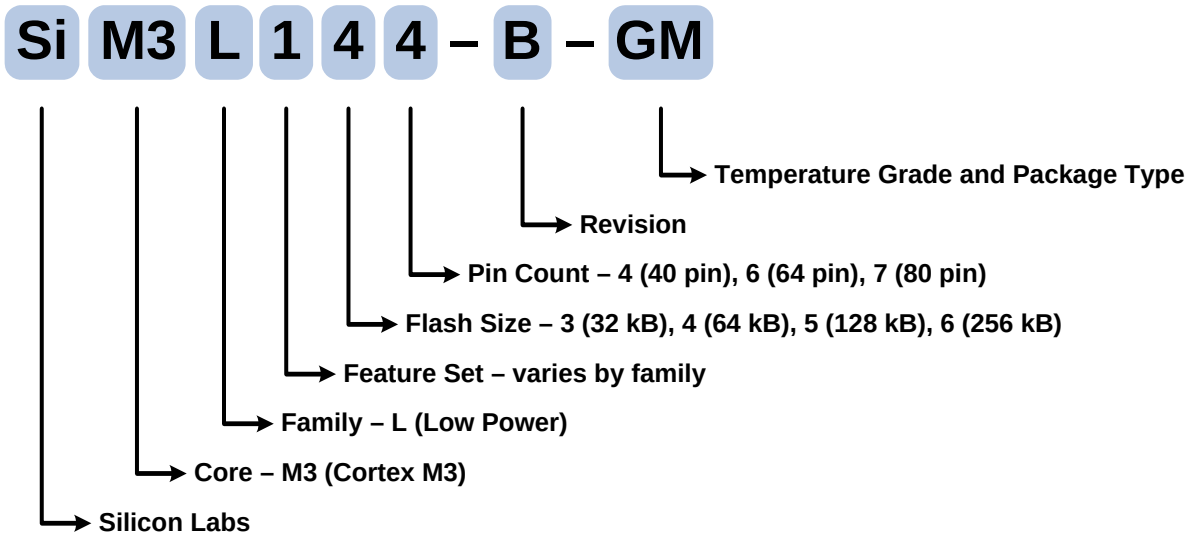

Figure 5.1. SiM3L1xx Part Numbering

All devices in the SiM3L1xx family have the following features:

- **Core:** ARM Cortex-M3 with maximum operating frequency of 50 MHz.
- **PLL.**
- **10-Channel DMA Controller.**
- **128/192/256-bit AES.**
- **16/32-bit CRC.**
- **Encoder/Decoder.**
- **DC-DC Buck Converter.**
- **Timers:** 3 x 32-bit (6 x 16-bit).
- **Real-Time Clock.**
- **Low-Power Timer.**
- **PCA:** 1 x 6 channels (Enhanced)
- **ADC:** 12-bit 250 ksps (10-bit 1 Msps) SAR.
- **DAC:** 10-bit IDAC.
- **Temperature Sensor.**
- **Internal VREF.**
- **Comparator:** 2 x low current.
- **Serial Buses:** 2 x USART, 2 x SPI, 1 x I2C

Additionally, all devices in the SiM3L1xx family include the low power mode advanced capture counter (ACCTR0), though the smaller packages (SiM3L1x4) only support some of the external inputs and outputs.

6. Pin Definitions

6.1. SiM3L1x7 Pin Definitions

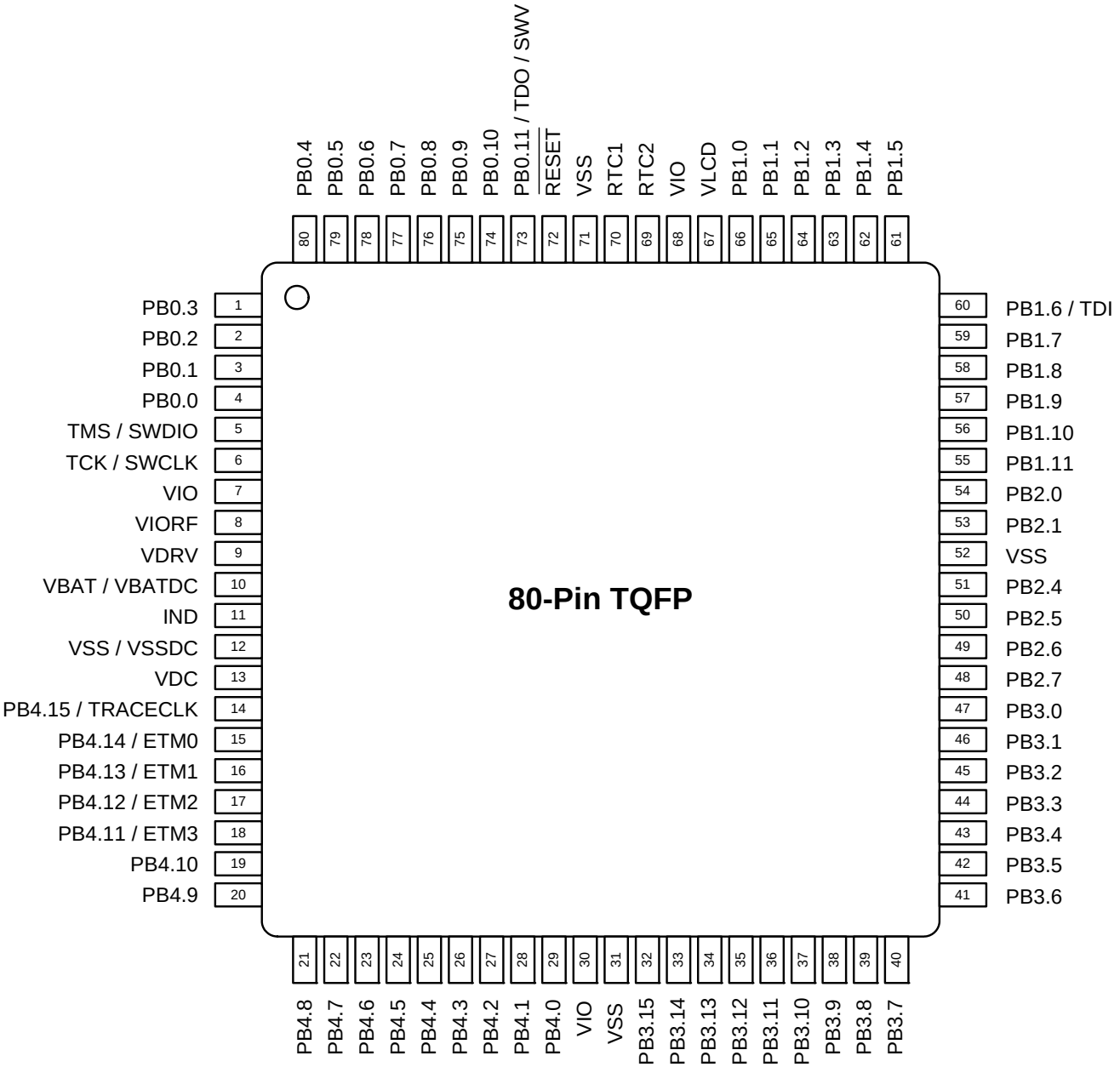

Figure 6.1. SiM3L1x7-GQ Pinout

Table 6.1. Pin Definitions and Alternate Functions for SiM3L1x7

Pin Name	Type	Pin Numbers (TQFP-80)	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
VSS	Ground	12 31 52 71							
VSSDC	Ground (DC-DC)	12							
VIO	Power (I/O)	7 30 68							
VIORF	Power (RF I/O)	8							
VBAT/ VBATDC		10							
VDRV		9							
VDC		13							
VLCD	Power (LCD Charge Pump)	67							
IND	DC-DC Inductor	11							
$\overline{\text{RESET}}$	Active-low Reset	72							
TCK/ SWCLK	JTAG / Serial Wire	6							
TMS/ SWDIO	JTAG / Serial Wire	5							
RTC1	RTC Oscillator Input	70							
RTC2	RTC Oscillator Output	69							

Table 6.2. Pin Definitions and Alternate Functions for SiM3L1x6 (Continued)

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB0.2	Standard I/O	1	VIO	XBR 0	✓		✓	INT0.2 WAKE.3	ADC0.23 CMP1N.0 XTAL1
PB0.3	Standard I/O	64	VIO	XBR 0	✓		✓	INT0.3 WAKE.4	ADC0.0 CMP0P.1 IDAC0
PB0.4	Standard I/O	63	VIO	XBR 0	✓		✓	INT0.4 WAKE.5 ACCTR0_STOP0	ACCTR0_IN0
PB0.5	Standard I/O	62	VIO	XBR 0	✓		✓	INT0.5 WAKE.6 ACCTR0_STOP1	ACCTR0_IN1
PB0.6	Standard I/O	61	VIO	XBR 0	✓		✓	INT0.6 WAKE.7	ACCTR0_LCIN0
PB0.7	Standard I/O	60	VIO	XBR 0	✓		✓	LPT0T0 LPT0OUT0 INT0.7 WAKE.8	ACCTR0_LCIN1
PB0.8	Standard I/O	59	VIO	XBR 0	✓		✓	LPT0T1 INT0.8 WAKE.9 ACCTR0_LCPUL0	ADC0.1 CMP0N.1
PB0.9/SWV	Standard I/O /Serial Wire Viewer	58	VIO	XBR 0	✓		✓	LPT0T2 INT0.9 WAKE.10 LPT0OUT1 ACCTR0_LCPUL1	ADC0.2 CMP1P.1
PB1.0	Standard I/O	53	VIO	XBR 0	✓	LCD0.31		LPT0T4 INT0.12 ACCTR0_LCBIAS0	CMP0P.2

Table 6.4. TQFP-80 Package Dimensions

Dimension	Min	Nominal	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.20	0.27
c	0.09	—	0.20
D	14.00 BSC		
D1	12.00 BSC		
e	0.50 BSC		
E	14.00 BSC		
E1	12.00 BSC		
L	0.45	0.60	0.75
L1	1.00 Ref		
Θ	0°	3.5°	7°
aaa	0.20		
bbb	0.20		
ccc	0.08		
ddd	0.08		
eee	0.05		

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant ADD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

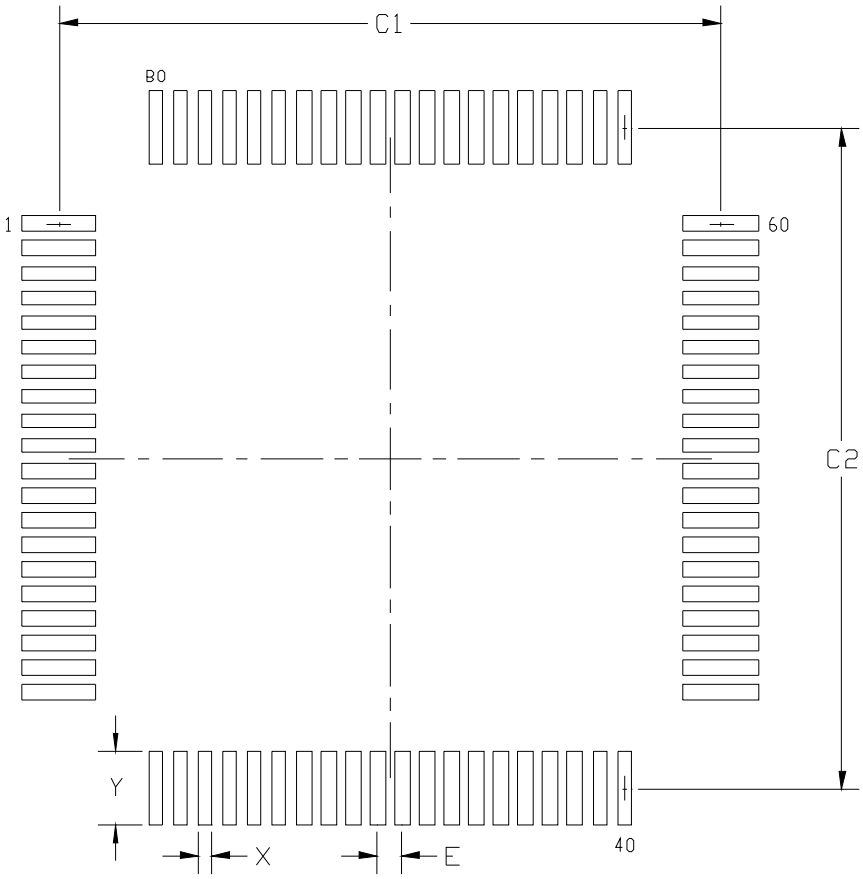

Figure 6.6. TQFP-80 Landing Diagram

Table 6.5. TQFP-80 Landing Diagram Dimensions

Dimension	Min	Max
C1	13.30	13.40
C2	13.30	13.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

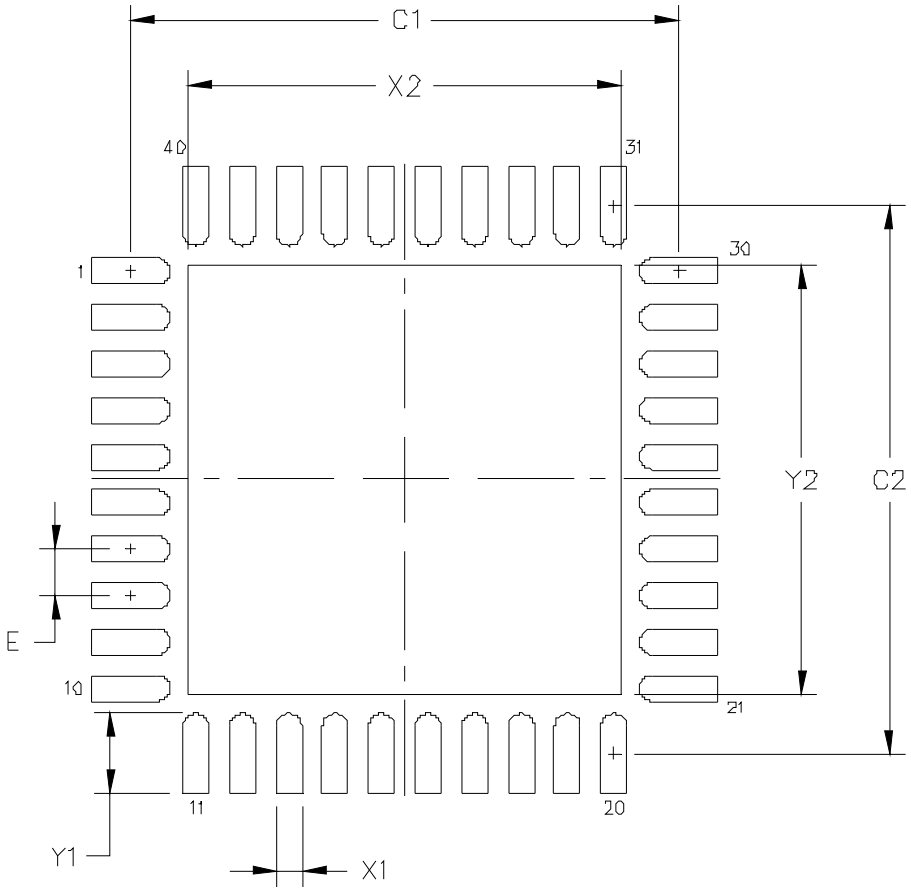

Figure 6.12. QFN-40 Landing Diagram

Table 6.11. QFN-40 Landing Diagram Dimensions

Dimension	mm
C1	5.90
C2	5.90
E	0.50
X1	0.30
Y1	0.85
X2	4.65
Y2	4.65

Notes:
1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

6.7.1. QFN-40 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.7.2. QFN-40 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 3x3 array of 1.1 mm square openings on a 1.6 mm pitch should be used for the center ground pad.

6.7.3. QFN-40 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. Revision Specific Behavior

This chapter describes any differences between released revisions of the device.

7.1. Revision Identification

The Lot ID Code on the top side of the device package can be used for decoding device revision information. Figures 7.1, 7.2, and 7.3 show how to find the Lot ID Code on the top side of the device package.

In addition, firmware can determine the revision of the device by checking the DEVICEID registers.

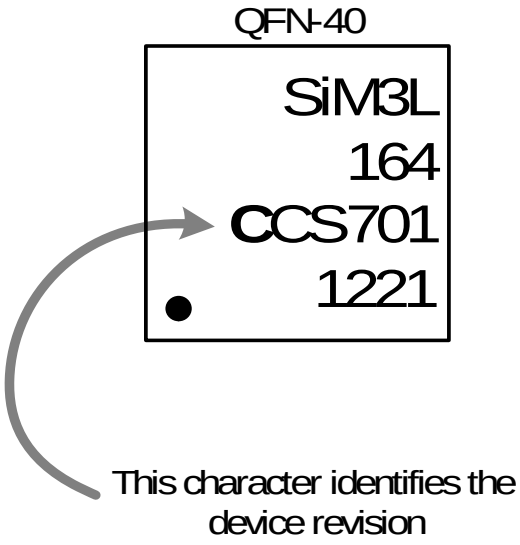

Figure 7.1. SiM3L1x7-GQ Revision Information

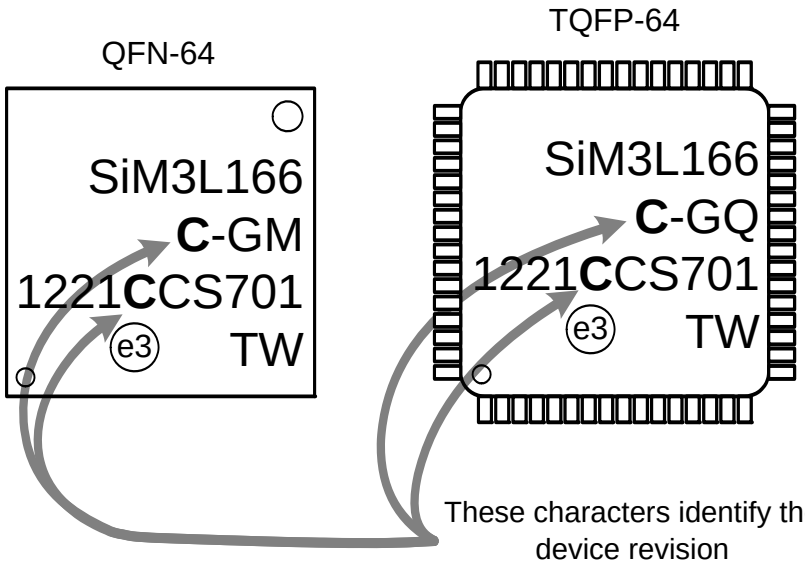

Figure 7.2. SiM3L1x6-GM and SiM3L1x6-GQ Revision Information