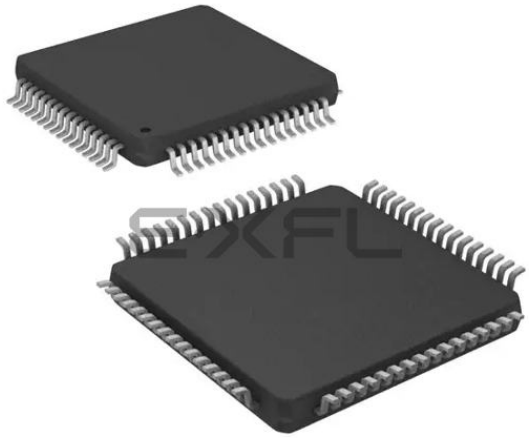

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | I²C, IrDA, SmartCard, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT |
| Number of I/O | 51 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.8V |
| Data Converters | A/D 23x10/12b; D/A 1x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-TQFP |
| Supplier Device Package | 64-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/sim3l146-c-gq |

# Table of Contents

**Table 3.2. Power Consumption (Continued)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SARADC0 | $I_{SARADC}$ | Sampling at 1 Msps, Internal VREF used | — | 1.2 | 1.6 | mA |
| | | Sampling at 250 ksps, lowest power mode settings. | — | 390 | 540 | µA |
| Temperature Sensor | $I_{TSENSE}$ | | — | 75 | 110 | µA |
| Internal SAR Reference | $I_{REFFS}$ | Normal Power Mode | — | 680 | — | µA |
| | | Normal Power Mode | — | 160 | — | µA |
| VREF0 | $I_{REFP}$ | | — | 80 | — | µA |
| Comparator 0 (CMP0), Comparator 1 (CMP1) | $I_{CMP}$ | CMPMD = 11 | — | 0.5 | 2 | µA |
| | | CMPMD = 10 | — | 3 | 8 | µA |
| | | CMPMD = 01 | — | 10 | 16 | µA |
| | | CMPMD = 00 | — | 25 | 42 | µA |
| IDAC0[8] | $I_{IDAC}$ | | — | 70 | 100 | µA |
| Voltage Supply Monitor (VMON0) | $I_{VMON}$ | | — | 10 | 22 | µA |
| **Flash Current on VBAT** | | | | | | |
| Write Operation | $I_{FLASH-W}$ | | — | — | 8 | mA |
| Erase Operation | $I_{FLASH-E}$ | | — | — | 15 | mA |

**Notes:**

1. Currents are additive. For example, where $I_{BAT}$ is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded $I_{VIO}$ is included in all $I_{BAT}$ PM8 production test measurements.

### Table 3.7. Internal Oscillators

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Phase-Locked Loop (PLL0OSC)** | | | | | | |
| Calibrated Output Frequency (Free-running output mode, RANGE = 2) | $f_{PLL0OSC}$ | Full Temperature and Supply Range | 48.3 | 49 | 49.7 | MHz |
| Power Supply Sensitivity (Free-running output mode, RANGE = 2) | $PSS_{PLL0OSC}$ | $T_A$ = 25 °C, Fout = 49 MHz | — | 300 | — | ppm/V |
| Temperature Sensitivity (Free-running output mode, RANGE = 2) | $TS_{PLL0OSC}$ | $V_{BAT}$ = 3.3 V, Fout = 49 MHz | — | 50 | — | ppm/°C |
| Adjustable Output Frequency Range | $f_{PLL0OSC}$ | | 23 | — | 50 | MHz |
| Lock Time | $t_{PLL0LOCK}$ | $f_{REF}$ = 20 MHz, $f_{PLL0OSC}$ = 50 MHz M=39, N=99, LOCKTH = 0 | — | 2.75 | — | µs |
| | | $f_{REF}$ = 2.5 MHz, $f_{PLL0OSC}$ = 50 MHz M=19, N=399, LOCKTH = 0 | — | 9.45 | — | µs |
| | | $f_{REF}$ = 32.768 kHz, $f_{PLL0OSC}$ = 50 MHz M=0, N=1524, LOCKTH = 0 | — | 92 | — | µs |
| **Low Power Oscillator (LPOSC0)** | | | | | | |
| Oscillator Frequency | $f_{LPOSC}$ | Full Temperature and Supply Range | 19 | 20 | 21 | MHz |
| Divided Oscillator Frequency | $f_{LPOSCD}$ | Full Temperature and Supply Range | 2.375 | 2.5 | 2.625 | MHz |
| Power Supply Sensitivity | $PSS_{LPOSC}$ | $T_A$ = 25 °C | — | 0.5 | — | %/V |
| Temperature Sensitivity | $TS_{LPOSC}$ | $V_{BAT}$ = 3.3 V | — | 55 | — | ppm/°C |
| **Low Frequency Oscillator (LFOSC0)** | | | | | | |
| Oscillator Frequency | $f_{LFOSC}$ | Full Temperature and Supply Range | 13.4 | 16.4 | 19.7 | kHz |
| | | $T_A$ = 25 °C, $V_{BAT}$ = 3.3 V | 15.8 | 16.4 | 17.3 | kHz |
| Power Supply Sensitivity | $PSS_{LFOSC}$ | $T_A$ = 25 °C | — | 2.4 | — | %/V |
| Temperature Sensitivity | $TS_{LFOSC}$ | $V_{BAT}$ = 3.3 V | — | 0.2 | — | %/°C |

**Table 3.11. ACCTR (Advanced Capture Counter) (Continued)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| LC Comparator Positive Hysteresis Mode 3 (CPMD = 00) | $HYS_{CP+}$ | CMPHYP = 00 | — | 1.37 | — | mV |
| | | CMPHYP = 01 | — | 3.8 | — | mV |
| | | CMPHYP = 10 | — | 7.8 | — | mV |
| | | CMPHYP = 11 | — | 15.6 | — | mV |
| LC Comparator Negative Hysteresis Mode 3 (CPMD = 00) | $HYS_{CP-}$ | CMPHYN = 00 | — | 1.37 | — | mV |
| | | CMPHYN = 01 | — | –3.9 | — | mV |
| | | CMPHYN = 10 | — | –7.9 | — | mV |
| | | CMPHYN = 11 | — | –16 | — | mV |
| LC Comparator Input Range (ACCTR0_LCIN pin) | $V_{IN}$ | | –0.25 | — | $V_{BAT}$ + 0.25 | V |
| LC Comparator Common-Mode Rejection Ratio | $CMRR_{CP}$ | | — | 75 | — | dB |
| LC Comparator Power Supply Rejection Ratio | $PSRR_{CP}$ | | — | 72 | — | dB |
| LC Comparator Input Offset Voltage | $V_{OFF}$ | $T_A$ = 25 °C | –10 | 0 | 10 | mV |
| LC Comparator Input Offset Tempco | $TC_{OFF}$ | | — | 3.5 | — | µV/°C |
| Reference DAC Offset Error | $DAC_{EOFF}$ | | –1 | — | 1 | LSB |
| Reference DAC Full Scale Output | $DAC_{FS}$ | Low Range | — | $V_{IO}$/8 | — | V |
| | | High Range | — | $V_{IO}$ | — | V |
| Reference DAC Step Size | $DAC_{LSB}$ | Low Range (48 steps) | — | $V_{IO}$/384 | — | V |
| | | High Range (64 steps) | — | $V_{IO}$/64 | — | V |
| LC Oscillator Period | $T_{LCOSC}$ | | — | 25 | — | ns |
| LC Bias Output Impedance | $R_{LCBIAS}$ | 10 µA Load | — | 1 | — | kΩ |
| LC Bias Drive Strength | $I_{LCBIAS}$ | | — | — | 2 | mA |
| Pull-Up Resistor Tolerance | $R_{TOL}$ | PUVAL[4:2] = 0 to 6 | -15 | — | 15 | % |
| | | PUVAL[4:2] = 7 | -10 | — | 10 | % |

**Table 3.16. Port I/O**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output High Voltage (PB0, PB1, PB3, or PB4) | $V_{OH}$ | Low Drive, $I_{OH}$ = –1 mA | $V_{IO}$ – 0.7 | — | — | V |
| | | Low Drive, $I_{OH}$ = –10 µA | $V_{IO}$ – 0.1 | — | — | V |
| | | High Drive, $I_{OH}$ = –3 mA | $V_{IO}$ – 0.7 | — | — | V |
| | | High Drive, $I_{OH}$ = –10 µA | $V_{IO}$ – 0.1 | — | — | V |
| Output High Voltage (PB2) | $V_{OH}$ | Low Drive, $I_{OH}$ = –1 mA | $V_{IORF}$ – 0.7 | — | — | V |
| | | Low Drive, $I_{OH}$ = –10 µA | $V_{IORF}$ – 0.1 | — | — | V |
| | | High Drive, $I_{OH}$ = –3 mA | $V_{IORF}$ – 0.7 | — | — | V |
| | | High Drive, $I_{OH}$ = –10 µA | $V_{IORF}$ – 0.1 | — | — | V |
| Output Low Voltage (any Port I/O pin or $\overline{\text{RESET}}$[1]) | $V_{OL}$ | Low Drive, $I_{OL}$ = 1.4 mA | — | — | 0.6 | V |
| | | Low Drive, $I_{OL}$ = 10 µA | — | — | 0.1 | V |
| | | High Drive, $I_{OL}$ = 8.5 mA | — | — | 0.6 | V |
| | | High Drive, $I_{OL}$ = 10 µA | — | — | 0.1 | V |
| Input High Voltage (PB0, PB1, PB3, PB4 or $\overline{\text{RESET}}$) | $V_{IH}$ | | $V_{IO}$ – 0.6 | — | — | V |
| Input High Voltage (PB2) | $V_{IH}$ | | $V_{IORF}$ – 0.6 | — | — | V |
| Input Low Voltage any Port I/O pin or $\overline{\text{RESET}}$) | $V_{IL}$ | | — | — | 0.6 | V |
| Weak Pull-Up Current[2] (per pin) | $I_{PU}$ | $V_{IO}$ or $V_{IORF}$ = 1.8 | -6 | -3.5 | -2 | µA |
| | | $V_{IO}$ or $V_{IORF}$ = 3.8 | -32 | -20 | -10 | µA |
| Input Leakage (Pullups off or Analog) | $I_{LK}$ | $0 \le V_{IN} \le V_{IO}$ or $V_{IORF}$ | -1 | — | 1 | µA |

**Notes:**

1. Specifications for $\overline{\text{RESET}}$ $V_{OL}$ adhere to the low drive setting.
2. On the SiM3L1x6 and SiM3L1x4 devices, the SWV pin will have double the weak pull-up current specified whenever the device is held in reset.

## 4.1. Power

The SiM3L1xx devices include a dc-dc buck converter that can take an input from 1.8–3.8 V and create an output from 1.25–3.8 V. In addition, SiM3L1xx devices include three low dropout regulators as part of the LDO0 module: one LDO powers the analog subsystems, one LDO powers the flash and SRAM memory at 1.8 V, and one LDO powers the digital and core circuitry. Each of these regulators can be independently powered from the dc-dc converter or directly from the battery voltage, and their outputs are adjustable to conserve system power. SiM3L1xx devices also include a low power charge pump in the PMU module for use in low power modes (PM8) to further reduce the power consumption of the device.

Figure 4.2 shows the power system configuration of these devices.

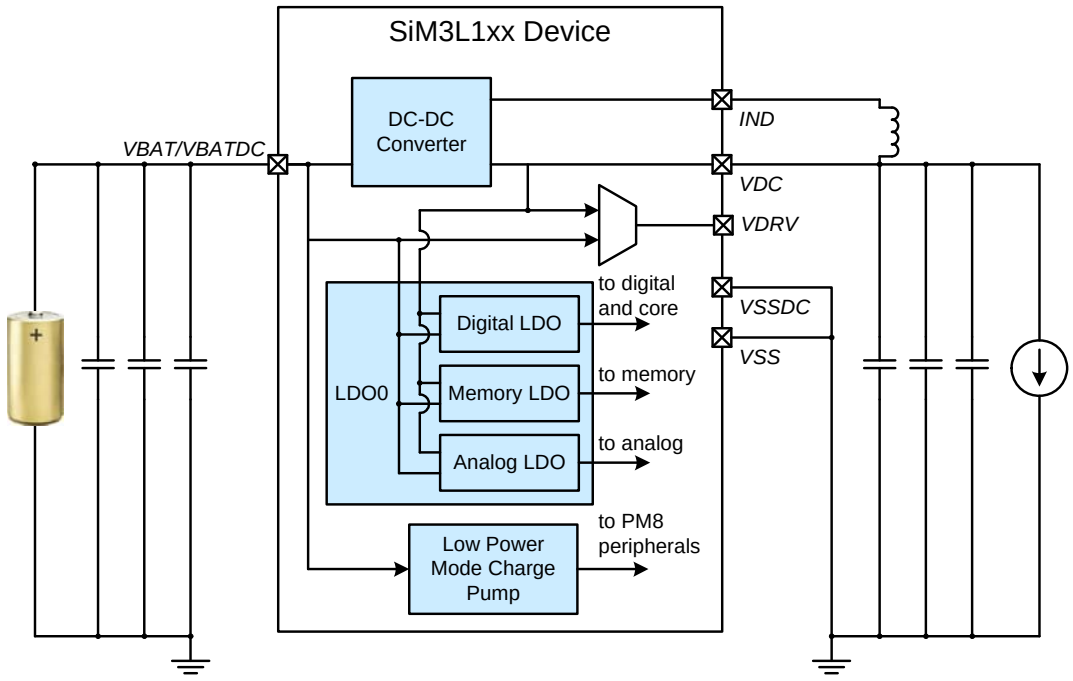



**Figure 4.2. SiM3L1xx Power**

### 4.1.1. DC-DC Buck Converter (DCDC0)

SiM3L1xx devices include an on-chip step-down dc-dc converter to efficiently utilize the energy stored in the battery, thus extending the operational life time. The dc-dc converter is a switching buck converter with a programmable output voltage that should be at least 0.45 V lower than the input battery voltage; if this criteria is not met and the converter can no longer operate, the output of the dc-dc converter automatically connects to the battery. The dc-dc converter can supply up to 100 mA and can be used to power the MCU and/or external devices in the system.

The dc-dc converter has a built in voltage reference and oscillator and will automatically limit or turn off the switching activity in case the peak inductor current rises beyond a safe limit or the output voltage rises above the programmed target value. This allows the dc-dc converter output to be safely overdriven by a secondary power source (when available) in order to preserve battery life. When enabled, the dc-dc converter can source current into the output capacitor, but cannot sink current.

The dc-dc converter includes the following features:

- Efficiently utilizes the energy stored in a battery, extending its operational lifetime.
- Input range: 1.8 to 3.8 V.
- Output range: 1.25 to 3.8 V in 50 mV (1.25–1.8 V) or 100 mV (1.8–3.8 V) steps.
- Supplies up to 100 mA.
- Includes a voltage reference and an oscillator.

### 4.6.3. Real-Time Clock (RTC0)

The RTC module includes a 32-bit timer that allows up to 36 hours of independent time-keeping when used with a 32.768 kHz watch crystal. The RTC provides three alarm events in addition to a missing clock event, which can also function as interrupt, reset, or wakeup sources on SiM3L1xx devices.

The RTC module includes internal loading capacitors that are programmable to 16 discrete levels, allowing compatibility with a wide range of crystals.

The RTC timer clock can be buffered and routed to a port bank pin to provide an accurate, low frequency clock to other devices while the core is in its lowest power down mode. The module also includes a low power internal low frequency oscillator that reduces low power mode current and is available for other modules to use as a clock source.

The RTC module includes the following features:

- 32-bit timer (supports up to 36 hours) with three separate alarms.
- Option for one alarm to automatically reset the RTC timer.
- Missing clock detector.
- Can be used with the internal Low Frequency Oscillator or with an external 32.768 kHz crystal (no additional resistors or capacitors necessary).
- Programmable internal loading capacitors support a wide range of external 32.768 kHz crystals.
- The RTC timer clock (RTC0CLK) can be buffered and routed to an I/O pin to provide an accurate, low frequency clock to other devices while the core is in its lowest power down mode.
- The RTC module can be powered from the low power mode charge pump for lowest possible power consumption while in PM8.

### 4.6.4. Low Power Timer (LPTIMER0)

The Low Power Timer (LPTIMER) module runs from the RTC timer clock (RTC0CLK), allowing the LPTIMER to operate even if the AHB and APB clocks are disabled. The LPTIMER counter can increment using one of two clock sources: the clock selected by the RTC0 module, or rising or falling edges of an external signal.

The Low Power Timer includes the following features:

- Runs on low-frequency RTC timer clock (RTC0TCLK).
- The LPTIMER counter can increment using one of two clock sources: the RTC0TCLK or rising or falling edges of an external signal.
- Overflow and threshold-match detection.
- Timer reset on threshold-match allows square-wave generation at a variable output frequency.
- Supports PWM with configurable period and duty cycle.
- The LPTIMER module can be powered from the low power mode charge pump for lowest possible power consumption while in PM8.

### 4.6.5. Watchdog Timer (WDTIMER0)

The WDTIMER module includes a 16-bit timer, a programmable early warning interrupt, and a programmable reset period. The timer registers are protected from inadvertent access by an independent lock and key interface.

The watchdog timer runs from the low frequency oscillator (LFOSC0).

The Watchdog Timer has the following features:

- Programmable timeout interval.
- Optional interrupt to warn when the Watchdog Timer is nearing the reset trip value.
- Lock-out feature to prevent any modification until a system reset.

## 4.7. Communications Peripherals

### 4.7.1. USART (USART0)

The USART uses two signals (TX and RX) to communicate serially with an external device. In addition to these signals, the USART module can optionally use a clock (UCLK) or hardware handshaking (RTS and CTS).

The USART module provides the following features:

- Independent transmitter and receiver configurations with separate 16-bit baud rate generators.
- Synchronous or asynchronous transmissions and receptions.
- Clock master or slave operation with programmable polarity and edge controls.
- Up to 5 Mbaud (synchronous or asynchronous, TX or RX, and master or slave) or 1 Mbaud Smartcard (TX or RX).
- Individual enables for generated clocks during start, stop, and idle states.
- Internal transmit and receive FIFOs with flush capability and support for byte, half-word, and word reads and writes.
- Data bit lengths from 5 to 9 bits.
- Programmable inter-packet transmit delays.
- Auto-baud detection with support for the LIN SYNC byte.
- Automatic parity generation (with enable).
- Automatic start and stop generation (with separate enables).
- Transmit and receive hardware flow-control.
- Independent inversion correction for TX, RX, RTS, and CTS signals.
- IrDA modulation and demodulation with programmable pulse widths.
- Smartcard ACK/NACK support.
- Parity error, frame error, overrun, and underrun detection.
- Multi-master and half-duplex support.
- Multiple loop-back modes supported.
- Multi-processor communications support.

### 4.7.2. UART (UART0)

The low-power UART uses two signals (TX and RX) to communicate serially with an external device.

The UART0 module can operate in PM8 mode by taking the clock directly from the RTC0 time clock (RTC0TCLK) and running from the low power mode charge pump. This will allow the system to conserve power while transmitting or receiving UART traffic. The UART supports standard baud-rates of 9600, 4800, 2400 and 1200 in this low power mode.

The UART0 module provides the following features:

- Independent transmitter and receiver configurations with separate 16-bit baud rate generators.
- Asynchronous transmissions and receptions.
- Up to 5 Mbaud (TX or RX).
- Internal transmit and receive FIFOs with flush capability and support for byte, half-word, and word reads and writes.
- Data bit lengths from 5 to 9 bits.
- Programmable inter-packet transmit delays.
- Auto-baud detection with support for the LIN SYNC byte.
- Automatic parity generation (with enable).
- Automatic start and stop generation (with separate enables).
- Independent inversion correction for TX and RX signals.
- Parity error, frame error, overrun, and underrun detection.
- Half-duplex support.

- Multiple loop-back modes supported.
- Multi-processor communications support.
- Operates at 9600, 4800, 2400, or 1200 baud in Power Mode 8.

### 4.7.3. SPI (SPI0, SPI1)

SPI is a 3- or 4-wire communication interface that includes a clock, input data, output data, and an optional select signal.

The SPI0 and SPI1 modules include the following features:

- Supports 3- or 4-wire master or slave modes.
- Supports up to 10 MHz clock in master mode and 5 MHz clock in slave mode.
- Support for all clock phase and slave select (NSS) polarity modes.
- 16-bit programmable clock rate.
- Programmable MSB-first or LSB-first shifting.
- 8-byte FIFO buffers for both transmit and receive data paths to support high speed transfers.
- Support for multiple masters on the same data lines.

In addition, the SPI modules include several features to support autonomous DMA transfers:

- Hardware NSS control.
- Programmable FIFO threshold levels.
- Configurable FIFO data widths.
- Master or slave hardware flow control for the MISO and MOSI signals.

SPI1 is on fixed pins and supports additional flow control options using a fixed input (SPI1CTS). Neither SPI1 nor the flow control input are on the crossbar.

### 4.7.4. I2C (I2C0)

The I2C interface is a two-wire, bi-directional serial bus. The clock and data signals operate in open-drain mode with external pull-ups to support automatic bus arbitration.

Reads and writes to the interface are byte oriented with the I2C interface autonomously controlling the serial transfer of the data. Data can be transferred at up to 1/8th of the APB clock as a master or slave, which can be faster than allowed by the I2C specification, depending on the clock source used. A method of extending the clock-low duration is available to accommodate devices with different speed capabilities on the same bus.

The I2C interface may operate as a master and/or slave, and may function on a bus with multiple masters. The I2C provides control of SDA (serial data), SCL (serial clock) generation and synchronization, arbitration logic, and start/stop control and generation.

The I2C0 module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds.
- Can operate down to APB clock divided by 32768 or up to APB clock divided by 8.
- Support for master, slave, and multi-master modes.
- Hardware synchronization and arbitration for multi-master mode.
- Clock low extending (clock stretching) to interface with faster masters.
- Hardware support for 7-bit slave and general call address recognition.
- Firmware support for 10-bit slave address decoding.
- Ability to disable all slave states.
- Programmable clock high and low period.
- Programmable data setup/hold times.
- Spike suppression up to 2 times the APB period.

## 4.8. Analog

### 4.8.1. 12-Bit Analog-to-Digital Converter (SARADC0)

The SARADC0 module on SiM3L1xx devices implements the Successive Approximation Register (SAR) ADC architecture. The key features of the module are as follows:

- Single-ended 12-bit and 10-bit modes.
- Supports an output update rate of 250 k samples per second in 12-bit mode or 1 M samples per second in 10-bit mode.
- Operation in low power modes at lower conversion speeds.
- Selectable asynchronous hardware conversion trigger with hardware channel select.
- DC offset cancellation.
- Automatic result notification with multiple programmable thresholds.
- Support for Burst Mode, which produces one set of accumulated data per conversion-start trigger with programmable power-on settling and tracking time.
- Non-burst mode operation can also automatically accumulate multiple conversions, but a conversion start is required for each conversion.
- Conversion complete, multiple conversion complete, and FIFO overflow and underflow flags and interrupts supported.
- Flexible output data formatting.
- Sequencer allows up to eight sources to be automatically scanned using one of four channel characteristic profiles without software intervention.
- Eight-word conversion data FIFO for DMA operations.
- Includes two internal references (1.65 V fast-settling, 1.2/2.4 V precision), support for an external reference, and support for an external signal ground.

### 4.8.2. 10-Bit Digital-to-Analog Converter (IDAC0)

The IDAC module takes a digital value as an input and outputs a proportional constant current on a pin. The IDAC module includes the following features:

- 10-bit current DAC with support for four timer, up to seven external I/O and on demand output update triggers.
- Ability to update on rising, falling, or both edges for any of the external I/O trigger sources.
- Supports an output update rate greater than 600 k samples per second.
- Support for three full-scale output modes: 0.5 mA, 1.0 mA and 2.0 mA.
- Four-word FIFO to aid with high-speed waveform generation or DMA interactions.
- Individual FIFO overrun, underrun, and went-empty interrupt status sources.
- Support for multiple data packing formats, including: single 10-bit sample per word, dual 10-bit samples per word, or four 8-bit samples per word.
- Support for left- and right-justified data.

### 4.8.3. Low Current Comparators (CMP0, CMP1)

The Comparators take two analog input voltages and output the relationship between these voltages (less than or greater than) as a digital signal. The low power comparator module includes the following features:

- Multiple sources for the positive and negative inputs, including VBAT, VREF, and 8 I/O pins.
- Two outputs available: a digital synchronous latched output and a digital asynchronous raw output.
- Programmable hysteresis and response time.
- Falling or rising edge interrupt options on the comparator output.
- 6-bit programmable reference divider.

# 5. Ordering Information

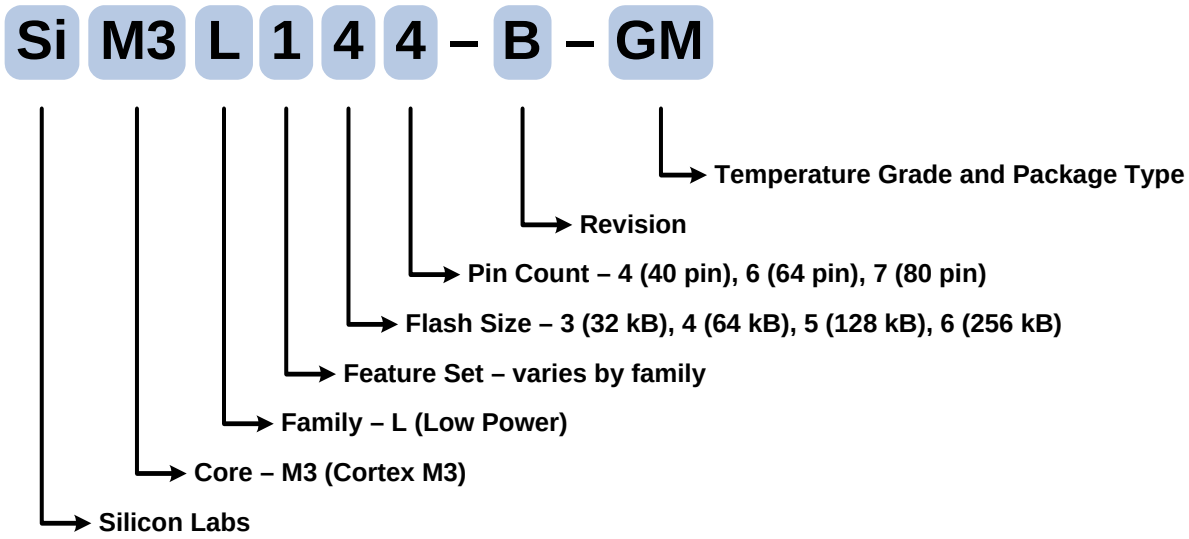



**Figure 5.1. SiM3L1xx Part Numbering**

All devices in the SiM3L1xx family have the following features:

- **Core:** ARM Cortex-M3 with maximum operating frequency of 50 MHz.
- **PLL.**
- **10-Channel DMA Controller.**
- **128/192/256-bit AES.**
- **16/32-bit CRC.**
- **Encoder/Decoder.**
- **DC-DC Buck Converter.**
- **Timers:** 3 x 32-bit (6 x 16-bit).
- **Real-Time Clock.**
- **Low-Power Timer.**
- **PCA:** 1 x 6 channels (Enhanced)
- **ADC:** 12-bit 250 ksps (10-bit 1 Msps) SAR.
- **DAC:** 10-bit IDAC.
- **Temperature Sensor.**
- **Internal VREF.**
- **Comparator:** 2 x low current.
- **Serial Buses:** 2 x USART, 2 x SPI, 1 x I2C

Additionally, all devices in the SiM3L1xx family include the low power mode advanced capture counter (ACCTR0), though the smaller packages (SiM3L1x4) only support some of the external inputs and outputs.

## 6.2. SiM3L1x6 Pin Definitions

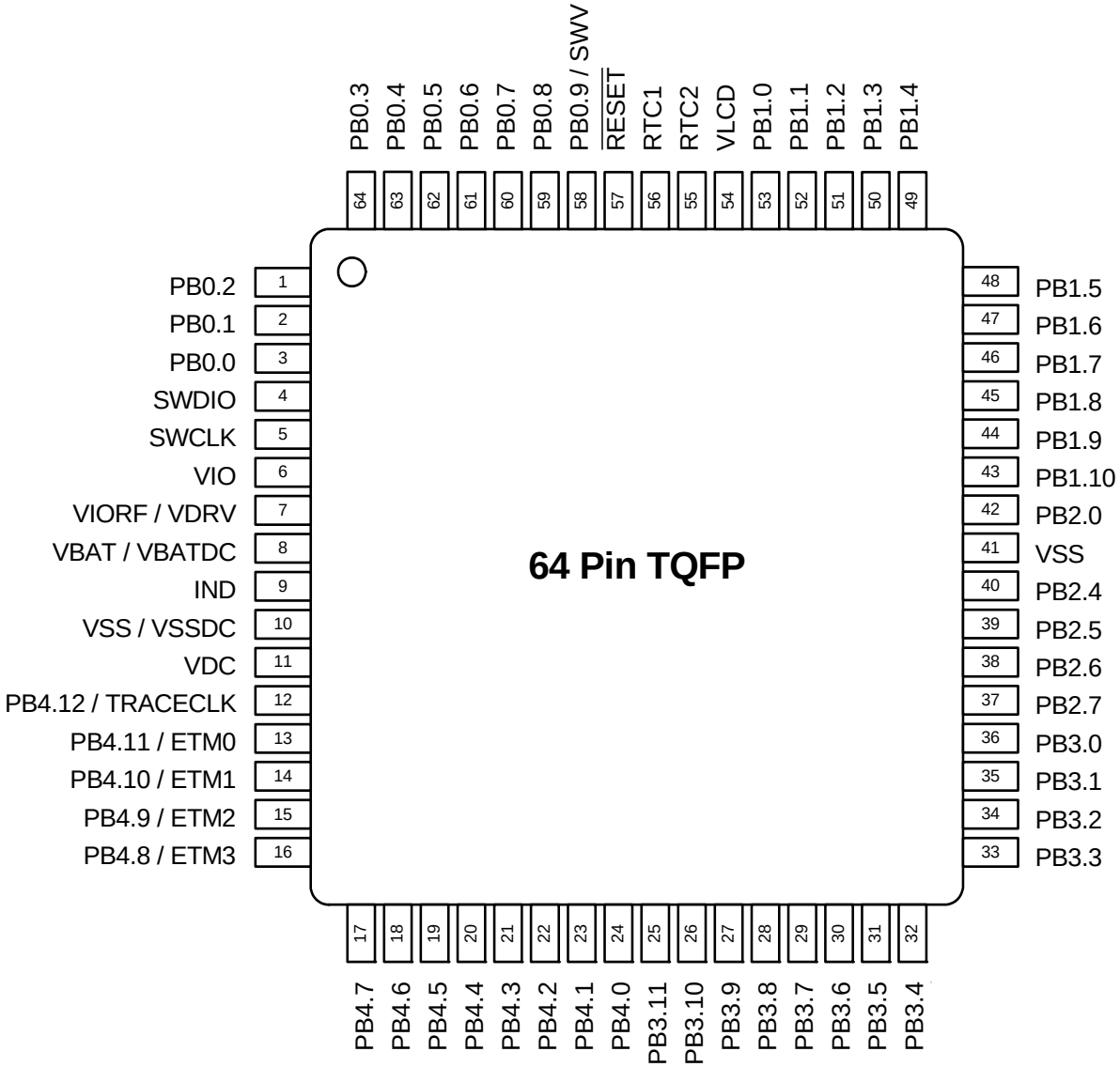



**Figure 6.2. SiM3L1x6-GQ Pinout**

**Table 6.2. Pin Definitions and Alternate Functions for SiM3L1x6 (Continued)**

| Pin Name | Type | Pin Numbers | I/O Voltage Domain | Crossbar Capability | Port Match | LCD Interface | Output Toggle Logic | External Trigger Inputs / Digital Functions | Analog Functions |
|---|---|---|---|---|---|---|---|---|---|
| PB0.2 | Standard I/O | 1 | VIO | XBR 0 | ✓ | | ✓ | INT0.2<br>WAKE.3 | ADC0.23<br>CMP1N.0<br>XTAL1 |
| PB0.3 | Standard I/O | 64 | VIO | XBR 0 | ✓ | | ✓ | INT0.3<br>WAKE.4 | ADC0.0<br>CMP0P.1<br>IDAC0 |
| PB0.4 | Standard I/O | 63 | VIO | XBR 0 | ✓ | | ✓ | INT0.4<br>WAKE.5<br>ACCTR0_STOP0 | ACCTR0_IN0 |
| PB0.5 | Standard I/O | 62 | VIO | XBR 0 | ✓ | | ✓ | INT0.5<br>WAKE.6<br>ACCTR0_STOP1 | ACCTR0_IN1 |
| PB0.6 | Standard I/O | 61 | VIO | XBR 0 | ✓ | | ✓ | INT0.6<br>WAKE.7 | ACCTR0_LCIN0 |
| PB0.7 | Standard I/O | 60 | VIO | XBR 0 | ✓ | | ✓ | LPT0T0<br>LPT0OUT0<br>INT0.7<br>WAKE.8 | ACCTR0_LCIN1 |
| PB0.8 | Standard I/O | 59 | VIO | XBR 0 | ✓ | | ✓ | LPT0T1<br>INT0.8<br>WAKE.9<br>ACCTR0_LCPUL0 | ADC0.1<br>CMP0N.1 |
| PB0.9/SWV | Standard I/O /Serial Wire Viewer | 58 | VIO | XBR 0 | ✓ | | ✓ | LPT0T2<br>INT0.9<br>WAKE.10<br>LPT0OUT1<br>ACCTR0_LCPUL1 | ADC0.2<br>CMP1P.1 |
| PB1.0 | Standard I/O | 53 | VIO | XBR 0 | ✓ | LCD0.31 | | LPT0T4<br>INT0.12<br>ACCTR0_LCBIAS0 | CMP0P.2 |

**Table 6.2. Pin Definitions and Alternate Functions for SiM3L1x6 (Continued)**

| Pin Name | Type | Pin Numbers | I/O Voltage Domain | Crossbar Capability | Port Match | LCD Interface | Output Toggle Logic | External Trigger Inputs / Digital Functions | Analog Functions |
|---|---|---|---|---|---|---|---|---|---|
| PB1.1 | Standard I/O | 52 | VIO | XBR0 | ✓ | LCD0.30 | | LPT0T5<br>INT0.13<br>ACCTR0_LCBIAS1 | CMP0N.2 |
| PB1.2 | Standard I/O | 51 | VIO | XBR0 | ✓ | LCD0.29 | | LPT0T6<br>INT0.14<br>UART0_TX | CMP1P.2 |
| PB1.3 | Standard I/O | 50 | VIO | XBR0 | ✓ | LCD0.28 | | LPT0T7<br>INT0.15<br>UART0_RX | CMP1N.2 |
| PB1.4 | Standard I/O | 49 | VIO | XBR0 | ✓ | LCD0.27 | | ACCTR0_DBG0 | ADC0.3 |
| PB1.5 | Standard I/O | 48 | VIO | XBR0 | ✓ | LCD0.26 | | ACCTR0_DBG1 | ADC0.4 |
| PB1.6 | Standard I/O | 47 | VIO | XBR0 | ✓ | LCD0.25 | | RTC0TCLK_OUT | ADC0.5 |
| PB1.7 | Standard I/O | 46 | VIO | XBR0 | ✓ | LCD0.24 | | | CMP0P.3 |
| PB1.8 | Standard I/O | 45 | VIO | XBR0 | ✓ | LCD0.23 | | | CMP0N.3 |
| PB1.9 | Standard I/O | 44 | VIO | XBR0 | ✓ | LCD0.22 | | | CMP1P.3 |
| PB1.10 | Standard I/O | 43 | VIO | XBR0 | ✓ | LCD0.21 | | | CMP1N.3 |
| PB2.0 | Standard I/O | 42 | VIORF | XBR0 | ✓ | | | LPT0T8<br>INT1.0<br>WAKE.12<br>SPI1_CTS | ADC0.6<br>CMP0P.4 |
| PB2.4 | Standard I/O | 40 | VIORF | XBR0 | ✓ | | | LPT0T12<br>INT1.4<br>SPI1_SCLK | ADC0.7<br>CMP0P.5 |

**Table 6.4. TQFP-80 Package Dimensions**

| Dimension | Min | Nominal | Max |
|---|---|---|---|
| A | — | — | 1.20 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| b | 0.17 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| D | 14.00 BSC | | |
| D1 | 12.00 BSC | | |
| e | 0.50 BSC | | |
| E | 14.00 BSC | | |
| E1 | 12.00 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 Ref | | |
| Θ | 0° | 3.5° | 7° |
| aaa | 0.20 | | |
| bbb | 0.20 | | |
| ccc | 0.08 | | |
| ddd | 0.08 | | |
| eee | 0.05 | | |

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant ADD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

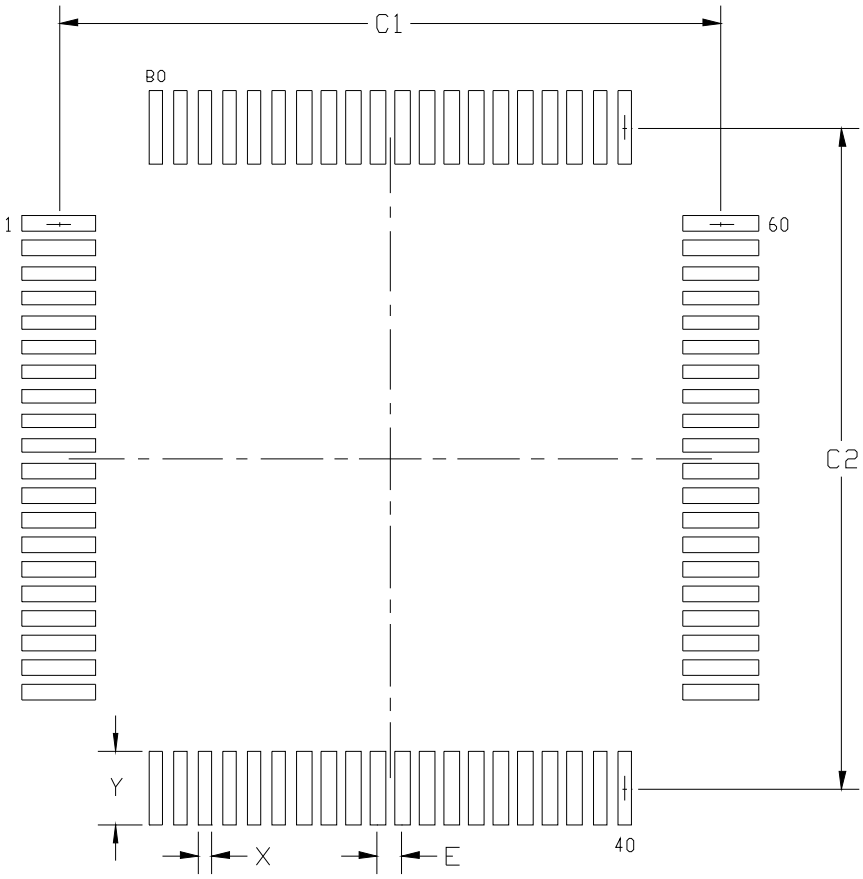



**Figure 6.6. TQFP-80 Landing Diagram**

**Table 6.5. TQFP-80 Landing Diagram Dimensions**

| Dimension | Min | Max |
|---|---|---|
| C1 | 13.30 | 13.40 |
| C2 | 13.30 | 13.40 |
| E | 0.50 BSC | |
| X | 0.20 | 0.30 |
| Y | 1.40 | 1.50 |

**Notes:**
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

**Table 6.8. TQFP-64 Package Dimensions**

| Dimension | Min | Nominal | Max |
|---|---|---|---|
| A | — | — | 1.20 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.09 | — | 0.20 |
| D | 12.00 BSC | | |
| D1 | 10.00 BSC | | |
| e | 0.50 BSC | | |
| E | 12.00 BSC | | |
| E1 | 10.00 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| Θ | 0° | 3.5° | 7° |
| aaa | — | — | 0.20 |
| bbb | — | — | 0.20 |
| ccc | — | — | 0.08 |
| ddd | — | — | 0.08 |

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant ACD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

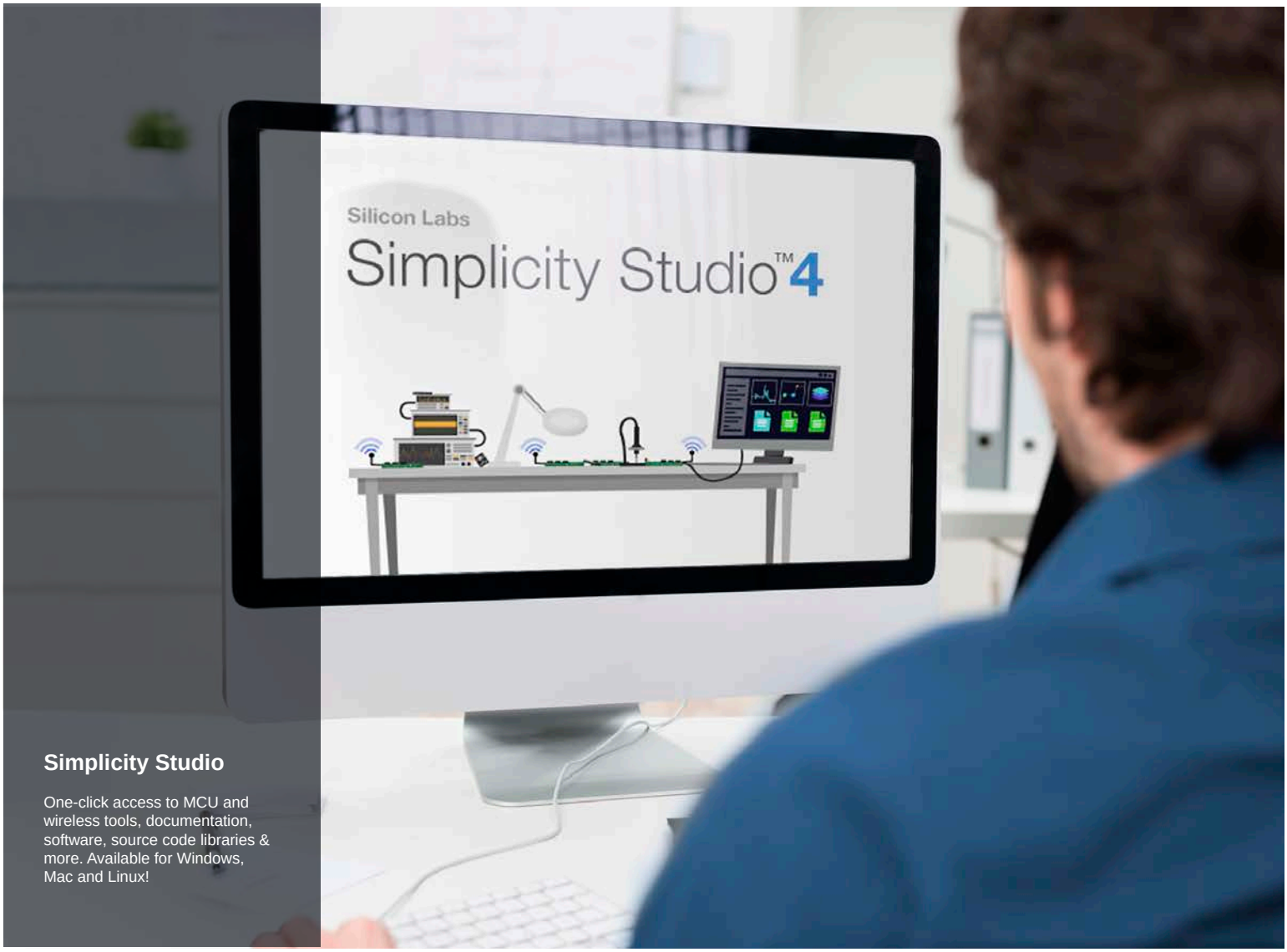
# Document Change List

## Revision 0.5 to Revision 1.0

- Updated Electrical Specifications Tables with latest characterization data and production test limits.
- Added missing signal ACCTR0_LCPUL1 to Table 6.2, “Pin Definitions and Alternate Functions for SiM3L1x6,” on page 64.
- Removed ACCTR0_LCIN1 and ACCTR0_STOP0/1 signals from Table 6.3, “Pin Definitions and Alternate Functions for SiM3L1x4,” on page 70.
- Updated Figure 6.8, “TFBGA-80 Package Drawing,” on page 79.

## Revision 1.0 to Revision 1.1

- Removed all references to BGA-80 and the parts SiM3L167-C-GL and SiM3L157-C-GL.

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