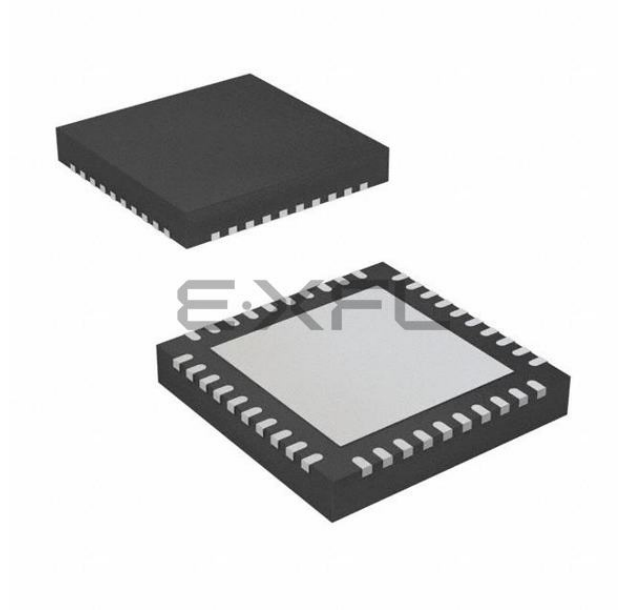

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | I²C, IrDA, SmartCard, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 28 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.8V |
| Data Converters | A/D 20x10/12b; D/A 1x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 40-VFQFN Exposed Pad |
| Supplier Device Package | 40-QFN (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/sim3l154-c-gmr |

# Table of Contents

### Table 3.2. Power Consumption

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Digital Core Supply Current** | | | | | | |
| Normal Mode[1,2,3,4]—Full speed with code executing from flash, peripheral clocks ON | $I_{BAT}$ | $F_{AHB}$ = 49 MHz, $F_{APB}$ = 24.5 MHz | — | 17.5 | 18.9 | mA |
| | | $F_{AHB}$ = 20 MHz, $F_{APB}$ = 10 MHz | — | 6.7 | 7.2 | mA |
| | | $F_{AHB}$ = 2.5 MHz, $F_{APB}$ = 1.25 MHz | — | 1.15 | 1.4 | mA |
| Normal Mode[1,2,3,4]—Full speed with code executing from flash, peripheral clocks OFF | $I_{BAT}$ | $F_{AHB}$ = 49 MHz, $F_{APB}$ = 24.5 MHz | — | 13.3 | 14.5 | mA |
| | | $F_{AHB}$ = 20 MHz, $F_{APB}$ = 10 MHz | — | 5.4 | 5.9 | mA |
| | | $F_{AHB}$ = 2.5 MHz, $F_{APB}$ = 1.25 MHz | — | 980 | 1.2 | µA |
| Normal Mode[1,2,3,4]—Full speed with code executing from flash, LDOs powered by dc-dc at 1.9 V, peripheral clocks OFF | $I_{BAT}$ | $F_{AHB}$ = 49 MHz, $F_{APB}$ = 24.5 MHz $V_{BAT}$ = 3.3 V | — | 9.7 | — | mA |
| | | $F_{AHB}$ = 49 MHz, $F_{APB}$ = 24.5 MHz $V_{BAT}$ = 3.8 V | — | 8.65 | — | mA |
| | | $F_{AHB}$ = 20 MHz, $F_{APB}$ = 10 MHz $V_{BAT}$ = 3.3 V | — | 4.15 | — | mA |
| | | $F_{AHB}$ = 20 MHz, $F_{APB}$ = 10 MHz $V_{BAT}$ = 3.8 V | — | 3.9 | — | mA |

**Notes:**

1. Currents are additive. For example, where $I_{BAT}$ is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded $I_{VIO}$ is included in all $I_{BAT}$ PM8 production test measurements.

### Table 3.12. Voltage Reference Electrical Characteristics

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Internal Fast Settling Reference** | | | | | | |
| Output Voltage | $V_{REFFS}$ | –40 to +85 °C, $V_{BAT}$ = 1.8–3.8 V | 1.6 | 1.65 | 1.7 | V |
| Temperature Coefficient | $TC_{REFFS}$ | | — | 50 | — | ppm/°C |
| Turn-on Time | $t_{REFFS}$ | | — | — | 1.5 | µs |
| Power Supply Rejection | $PSRR_{REFFS}$ | | — | 400 | — | ppm/V |
| **Internal Precision Reference** | | | | | | |
| Valid Supply Range | $V_{BAT}$ | VREF2X = 0 | 1.8 | — | 3.8 | V |
| | | VREF2X = 1 | 2.7 | — | 3.8 | V |
| Output Voltage | $V_{REFP}$ | 25 °C ambient, VREF2X = 0 | 1.17 | 1.2 | 1.23 | V |
| | | 25 °C ambient, VREF2X = 1 | 2.35 | 2.4 | 2.45 | V |
| Short-Circuit Current | $I_{SC}$ | | — | — | 10 | mA |
| Temperature Coefficient | $TC_{VREFP}$ | | — | 35 | — | ppm/°C |
| Load Regulation | $LR_{VREFP}$ | Load = 0 to 200 µA to VREFGND | — | 4.5 | — | ppm/µA |
| Load Capacitor | $C_{VREFP}$ | Load = 0 to 200 µA to VREFGND | 0.1 | — | — | µF |
| Turn-on Time | $t_{VREFPON}$ | 4.7 µF tantalum, 0.1 µF ceramic bypass | — | 3.8 | — | ms |
| | | 0.1 µF ceramic bypass | — | 200 | — | µs |
| Power Supply Rejection | $PSRR_{VREFP}$ | VREF2X = 0 | — | 320 | — | ppm/V |
| | | VREF2X = 1 | — | 560 | — | ppm/V |
| **External Reference** | | | | | | |
| Input Current | $I_{EXTREF}$ | Sample Rate = 250 ksps; VREF = 3.0 V | — | 5.25 | — | µA |

### Table 3.13. Temperature Sensor

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Offset | $V_{OFF}$ | $T_A$ = 0 °C | — | 760 | — | mV |
| Offset Error* | $E_{OFF}$ | $T_A$ = 0 °C | — | ±14 | — | mV |
| Slope | M | | — | 2.77 | — | mV/°C |
| Slope Error* | $E_M$ | | — | ±25 | — | µV/°C |
| Linearity | | | — | 1 | — | °C |
| Turn-on Time | | | — | 1.8 | — | µs |

***Note:** Absolute input pin voltage is limited by the lower of the supply at VBAT and VIO.

**Table 3.14. Comparator (Continued)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Positive Hysteresis Mode 3 (CPMD = 11) | $HYS_{CP+}$ | CMPHYP = 00 | — | 1.37 | — | mV |
| | | CMPHYP = 01 | — | 3.8 | — | mV |
| | | CMPHYP = 10 | — | 7.8 | — | mV |
| | | CMPHYP = 11 | — | 15.6 | — | mV |
| Negative Hysteresis Mode 3 (CPMD = 11) | $HYS_{CP-}$ | CMPHYN = 00 | — | 1.37 | — | mV |
| | | CMPHYN = 01 | — | –3.9 | — | mV |
| | | CMPHYN = 10 | — | –7.9 | — | mV |
| | | CMPHYN = 11 | — | –16 | — | mV |
| Input Range (CP+ or CP–) | $V_{IN}$ | | –0.25 | — | $V_{BAT}$ + 0.25 | V |
| Input Pin Capacitance | $C_{CP}$ | | — | 7.5 | — | pF |
| Common-Mode Rejection Ratio | $CMRR_{CP}$ | | — | 75 | — | dB |
| Power Supply Rejection Ratio | $PSRR_{CP}$ | | — | 72 | — | dB |
| Input Offset Voltage | $V_{OFF}$ | $T_A$ = 25 °C | –10 | 0 | 10 | mV |
| Input Offset Tempco | $TC_{OFF}$ | | — | 3.5 | — | µV/°C |
| Reference DAC Resolution | $N_{Bits}$ | | | 6 | | bits |

**Table 3.15. LCD0**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Charge Pump Output Voltage Error | $V_{CPERR}$ | | — | ±50 | — | mV |
| LCD Clock Frequency | $F_{LCD}$ | | 16 | — | 33 | kHz |

## 4.2. I/O

### 4.2.1. General Features

The SiM3L1xx ports have the following features:

- 5 V tolerant.
- Push-pull or open-drain output modes to the VIO or VIORF voltage level.
- Analog or digital modes.
- Option for high or low output drive strength.
- Port Match allows the device to recognize a change on a port pin value.
- Internal pull-up resistors are enabled or disabled on a port-by-port basis.
- Two external interrupts with up to 16 inputs each provide monitoring capability for external signals.
- Internal Pulse Generator Timer (PB0 only) to generate simple square waves and pulses.

### 4.2.2. Crossbar

The SiM3L1xx devices have one crossbar with the following features:

- Flexible peripheral assignment to port pins.
- Pins can be individually skipped to move peripherals as needed for design or layout considerations.

The crossbar has a fixed priority for each I/O function and assigns these functions to the port pins. When a digital resource is selected, the least-significant unassigned port pin is assigned to that resource. If a port pin is assigned, the crossbar skips that pin when assigning the next selected resource. Additionally, the crossbar will skip port pins whose associated bits in the PBSKIPEN registers are set. This provides flexibility when designing a system: pins involved with sensitive analog measurements can be moved away from digital I/O, and peripherals can be moved around the chip as needed to ease layout constraints.

### 4.3.1. PLL (PLL0)

The PLL module consists of a dedicated Digitally-Controlled Oscillator (DCO) that can be used in Free-Running mode without a reference frequency, Frequency-Locked to a reference frequency, or Phase-Locked to a reference frequency. The reference frequency for Frequency-Lock and Phase-Lock modes can use one of multiple sources (including the external oscillator) to provide maximum flexibility for different application needs. Because the PLL module generates its own clock, the DCO can be locked to a particular reference frequency and then moved to Free-Running mode to reduce system power and noise.

The PLL module includes the following features:

- Three output ranges with output frequencies ranging from 23 to 50 MHz.
- Multiple reference frequency inputs, including the RTC0 oscillator, Low Power Oscillator, and external oscillator.
- Three output modes: Free-Running Digitally-Controlled Oscillator, Frequency-Locked, and Phase-Locked.
- Able to sense the rising edge or falling edge of the reference source.
- DCO frequency LSB dithering to provide finer average output frequencies.
- Spectrum spreading to reduce generated system noise.
- Low jitter and fast lock times.\
- All output frequency updates (including dithering and spectrum spreading) can be temporarily suspended using the STALL bit during noise-sensitive measurements.

### 4.3.2. Low Power Oscillator (LPOSC0)

The Low Power Oscillator is the default AHB oscillator on SiM3L1xx devices and enables or disables automatically, as needed.

The default output frequency of this oscillator is factory calibrated to 20 MHz, and a divided 2.5 MHz version of this clock is also available as an AHB clock source.

The Low Power Oscillator has the following features:

- 20 MHz and divided 2.5 MHz frequencies available for the AHB clock.
- Automatically starts and stops as needed.

### 4.3.3. Low Frequency Oscillator (LFOSC0)

The low frequency oscillator (LFOSC) provides a low power internal clock source for the RTC0 timer and other peripherals on the device. No external components are required to use the low frequency oscillator, and the RTC1 and RTC2 pins do not need to be shorted together.

The Low Frequency Oscillator has the following features:

- 16.4 kHz output frequency.

### 4.3.4. External Oscillators (EXTOSC0)

The EXTOSC0 external oscillator circuit may drive an external crystal, ceramic resonator, capacitor, or RC network. A CMOS clock may also provide a clock input. The external oscillator output may be selected as the AHB clock or used to clock other modules independent of the AHB clock selection.

The External Oscillator control has the following features:

- Support for external crystal, resonator, RC, C, or CMOS oscillators.
- Support for external CMOS frequencies from 10 kHz to 50 MHz.
- Support for external crystal frequencies from 10 kHz to 25 MHz.
- Various drive strengths for flexible crystal oscillator support.
- Internal frequency divide-by-two option available.

## 4.5. Data Peripherals

### 4.5.1. 10-Channel DMA Controller

The DMA facilitates autonomous peripheral operation, allowing the core to finish tasks more quickly without spending time polling or waiting for peripherals to interrupt. This helps reduce the overall power consumption of the system, as the device can spend more time in low-power modes.

The DMA controller has the following features:

- Utilizes ARM PrimeCell uDMA architecture.
- Implements 10 channels.
- DMA crossbar supports DTM0, DTM1, DTM2, SARADC0, IDAC0, I2C0, SPI0, SPI1, USART0, AES0, ENCDEC0, EPCA0, external pin triggers, and timers.
- Supports primary, alternate, and scatter-gather data structures to implement various types of transfers.
- Access allowed to all AHB and APB memory space.

### 4.5.2. Data Transfer Managers (DTM0, DTM1, DTM2)

The Data Transfer Manager is a module that collects DMA request signals from various peripherals and generates a series of master DMA requests based on a state-driven configuration. This master request drives a set of DMA channels to perform functions such as assembling and transferring communication packets to external devices. This capability saves power by allowing the core to remain in a low power mode during complex transfer operations. A combination of simple and peripheral scatter-gather DMA configurations can be used to perform complex operations while reducing memory requirements.

The DTM acts as a side channel for the peripheral's DMA control signals. When active, it manages the DMA control signals for the peripherals. When the DTMn module is inactive, the peripherals communicate directly to the DMA module.

The DTMn module has the following features:

- State descriptions stored in RAM with up to 15 states supported per module.
- Supports up to 15 source peripherals and up to 15 destination peripherals per module, in addition to memory or peripherals that do not require a data request.
- Includes error detection and an optional transfer timeout.
- Includes notifications for state transitions.

### 4.5.3. 128/192/256-bit Hardware AES Encryption (AES0)

The basic AES block cipher is implemented in hardware. The integrated hardware support for Cipher Block Chaining (CBC) and Counter (CTR) algorithms results in identical performance, memory bandwidth, and memory footprint between the most basic Electronic Codebook (ECB) algorithm and these more complex algorithms. This hardware accelerator translates to more core bandwidth available for other functions or a power savings for low-power applications.

The AES module includes the following features:

- Operates on 4-word (16-byte) blocks.
- Supports key sizes of 128, 192, and 256 bits for both encryption and decryption.
- Generates the round key for decryption operations.
- All cipher operations can be performed without any firmware intervention for multiple 4-word blocks (up to 32 kB).
- Support for various chained and stream-ciphering configurations with XOR paths on both the input and output.
- Internal 4-word FIFOs to facilitate DMA operations.
- Integrated key storage.
- Hardware acceleration for Electronic Codebook (ECB), Cipher-Block Chaining (CBC), and Counter (CTR) algorithms utilizing integrated counterblock generation and previous-block caching.

### 4.5.4. 16/32-bit Enhanced CRC (ECRC0)

The ECRC module is designed to provide hardware calculations for flash memory verification and communications protocols. In addition to calculating a result from direct writes from firmware, the ECRC module can automatically snoop the APB bus and calculate a result from data written to or read from a particular peripheral. This allows for an automatic CRC result without directly feeding data through the ECRC module.

The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3). The 16-bit polynomial is fully programmable.

The ECRC module includes the following features:

- Support for a programmable 16-bit polynomial and one fixed 32-bit polynomial.
- Byte-level bit reversal for the CRC input.
- Byte-order reorientation of words for the CRC input.
- Word or half-word bit reversal of the CRC result.
- Ability to configure and seed an operation in a single register write.
- Support for single-cycle parallel (unrolled) CRC computation for 32-, 16-, or 8-bit blocks.
- Capability to CRC 32 bits of data per peripheral bus (APB) clock.
- Automatic APB bus snooping.
- Support for DMA writes using firmware request mode.

### 4.5.5. Encoder / Decoder (ENCDEC0)

The encoder / decoder module supports Manchester and Three-out-of-Six encoding and decoding from either firmware or DMA operations.

This module has the following features:

- Supports Manchester and Three-out-of-Six encoding and decoding.
- Automatic flag clearing when writing the input or reading the output data registers.
- Writing to the input data register automatically initiates an encode or decode operation.
- Optional output in one’s complement format.
- Hardware error detection for invalid input data during decode operations, which helps reduce power consumption and packet turn-around time.
- Flexible byte swapping on the input or output data.

## 4.6. Counters/Timers

### 4.6.1. 32-bit Timer (TIMER0, TIMER1, TIMER2)

Each timer module is independent, and includes the following features:

- Operation as a single 32-bit or two independent 16-bit timers.
- Clocking options include the APB clock, the APB clock scaled using an 8-bit prescaler, the external oscillator, or falling edges on an external input pin (synchronized to the APB clock).
- Auto-reload functionality in both 32-bit and 16-bit modes.

TIMER0 and TIMER1 have the following features:

- Up/Down count capability, controlled by an external input pin.
- Rising and falling edge capture modes.
- Low or high pulse capture modes.
- Period and duty cycle capture mode.
- Square wave output mode, which is capable of toggling an external pin at a given rate with 50% duty cycle.
- 32- or 16-bit pulse-width modulation mode.

TIMER2 does not support the standard input/output features of TIMER0 and TIMER1. The TIMER2 EX signal is internally connected to the outputs of the PVTOSC0 oscillators. TIMER2 can use any of the counting modes that use EX as an input, including up/down mode, edge capture mode, and pulse capture mode. The TIMER2 CT signal is disconnected.

### 4.6.2. Enhanced Programmable Counter Array (EPCA0)

The Enhanced Programmable Counter Array (EPCA) module is a timer/counter system allowing for complex timing or waveform generation. Multiple modules run from the same main counter, allowing for synchronous output waveforms.

This module includes the following features:

- Three sets of channel pairs (six channels total) capable of generating complementary waveforms.
- Center- and edge-aligned waveform generation.
- Programmable dead times that ensure channel pairs are never active at the same time.
- Programmable clock divisor and multiple options for clock source selection.
- Waveform update scheduling.
- Option to function while the core is inactive.
- Multiple synchronization triggers.
- Pulse-Width Modulation (PWM) waveform generation.

## 4.10. Security

The peripherals on the SiM3L1xx devices have a register lock and key mechanism that prevents undesired accesses of the peripherals from firmware. Each bit in the PERIPHLOCKx registers controls a set of peripherals. A key sequence must be written to the KEY register to modify bits in PERIPHLOCKx. Any subsequent write to KEY will then inhibit accesses of PERIPHLOCKx until it is unlocked again through KEY. Reading the KEY register indicates the current status of the PERIPHLOCKx lock state.

If a peripheral's registers are locked, all writes will be ignored. The registers can be read, regardless of the peripheral's lock state.

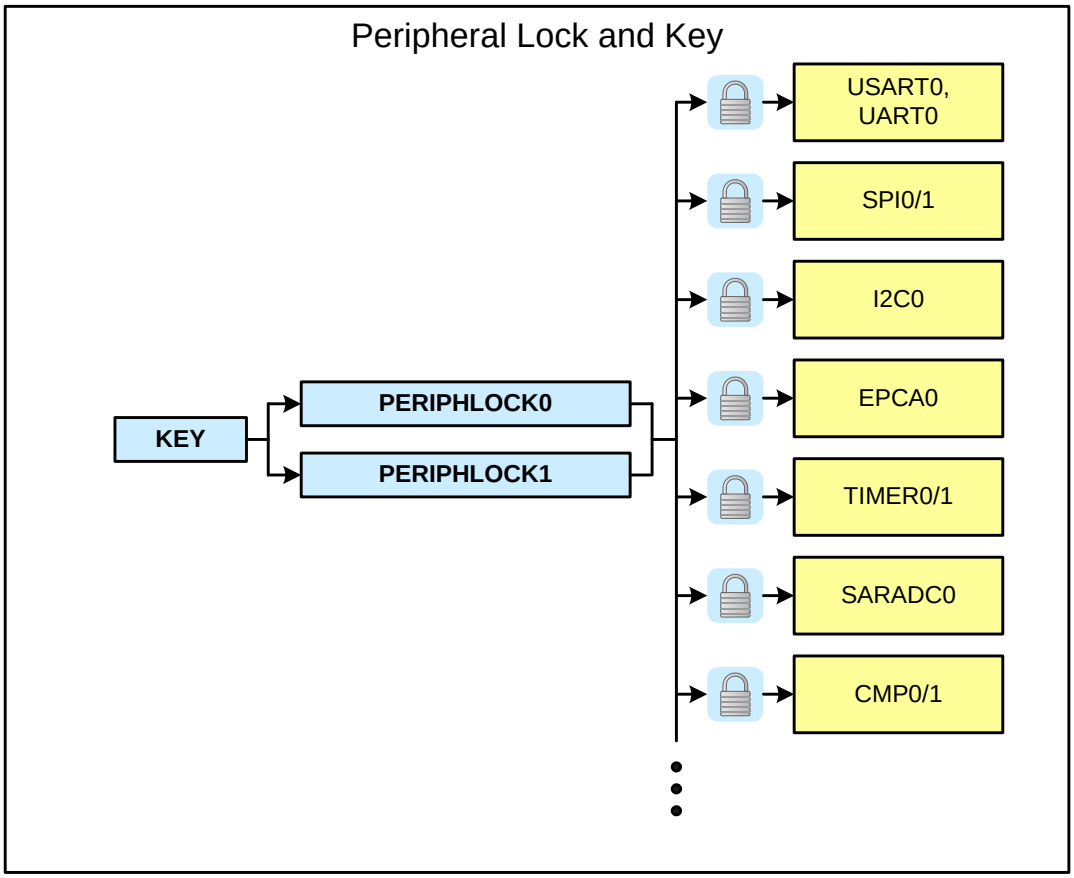


**Figure 4.5. SiM3L1xx Security Block Diagram**

## 4.11. On-Chip Debugging

The SiM3L1xx devices include JTAG and Serial Wire programming and debugging interfaces and ETM for instruction trace. The JTAG interface is supported on SiM3L1x7 devices only, and does not include boundary scan capabilites. The ETM interface is supported on SiM3L1x7, and SiM3L1x6 devices only. The JTAG and ETM interfaces can be optionally enabled to provide more visibility while debugging at the cost of using several Port I/O pins. Additionally, if the core is configured for Serial Wire (SW) mode and not JTAG, then the Serial Wire Viewer (SWV) is available to provide a single pin to send out TPIU messages. Serial Wire Viewer is supported on all SiM3Lxxx devices.

Most peripherals on SiM3L1xx devices have the option to halt or continue functioning when the core halts in debug mode.

**Table 6.1. Pin Definitions and Alternate Functions for SiM3L1x7 (Continued)**

| Pin Name | Type | Pin Numbers (TQFP-80) | I/O Voltage Domain | Crossbar Capability | Port Match | LCD Interface | Output Toggle Logic | External Trigger Inputs / Digital Functions | Analog Functions |
|---|---|---|---|---|---|---|---|---|---|
| PB0.9 | Standard I/O | 75 | VIO | ✓ | ✓ | | ✓ | LPT0T1<br>INT0.9<br>WAKE.9<br>ACCTR0_LCPUL0 | ADC0.1<br>CMP0N.1 |
| PB0.10 | Standard I/O | 74 | VIO | ✓ | ✓ | | ✓ | LPT0T2<br>INT0.10<br>WAKE.10<br>ACCTR0_LCPUL1 | ADC0.2<br>CMP1P.1 |
| PB0.11/ TDO/SWV | Standard I/O / JTAG / Serial Wire Viewer | 73 | VIO | ✓ | ✓ | | ✓ | LPT0T3<br>LPT0OUT1<br>INT0.11<br>WAKE.11 | ADC0.3<br>CMP1N.1 |
| PB1.0 | Standard I/O | 66 | VIO | ✓ | ✓ | LCD0.39 | | LPT0T4<br>INT0.12<br>ACCTR0_LCBIAS0 | CMP0P.2 |
| PB1.1 | Standard I/O | 65 | VIO | ✓ | ✓ | LCD0.38 | | LPT0T5<br>INT0.13<br>ACCTR0_LCBIAS1 | CMP0N.2 |
| PB1.2 | Standard I/O | 64 | VIO | ✓ | ✓ | LCD0.37 | | LPT0T6<br>INT0.14<br>UART0_TX | CMP1P.2 |
| PB1.3 | Standard I/O | 63 | VIO | ✓ | ✓ | LCD0.36 | | LPT0T7<br>INT0.15<br>UART0_RX | CMP1N.2 |
| PB1.4 | Standard I/O | 62 | VIO | ✓ | ✓ | LCD0.35 | | ACCTR0_DBG0 | ADC0.4 |
| PB1.5 | Standard I/O | 61 | VIO | ✓ | ✓ | LCD0.34 | | ACCTR0_DBG1 | ADC0.5 |
| PB1.6/TDI | Standard I/O / JTAG | 60 | VIO | ✓ | ✓ | LCD0.33 | | | ADC0.6 |
| PB1.7 | Standard I/O | 59 | VIO | ✓ | ✓ | LCD0.32 | | RTC0TCLK_OUT | ADC0.7 |

**Table 6.1. Pin Definitions and Alternate Functions for SiM3L1x7 (Continued)**

| Pin Name | Type | Pin Numbers (TQFP-80) | I/O Voltage Domain | Crossbar Capability | Port Match | LCD Interface | Output Toggle Logic | External Trigger Inputs / Digital Functions | Analog Functions |
|---|---|---|---|---|---|---|---|---|---|
| PB4.9 | Standard I/O | 20 | VIO | | ✓ | LCD0.6 | | | |
| PB4.10 | Standard I/O | 19 | VIO | | ✓ | LCD0.5 | | | |
| PB4.11/ ETM3 | Standard I/O / ETM | 18 | VIO | | ✓ | LCD0.4 | | | |
| PB4.12/ ETM2 | Standard I/O / ETM | 17 | VIO | | ✓ | LCD0.3 | | | |
| PB4.13/ ETM1 | Standard I/O / ETM | 16 | VIO | | ✓ | LCD0.2 | | | |
| PB4.14/ ETM0 | Standard I/O / ETM | 15 | VIO | | ✓ | LCD0.1 | | | |
| PB4.15/ TRACE-CLK | Standard I/O / ETM | 14 | VIO | | ✓ | LCD0.0 | | | |

## 6.2. SiM3L1x6 Pin Definitions

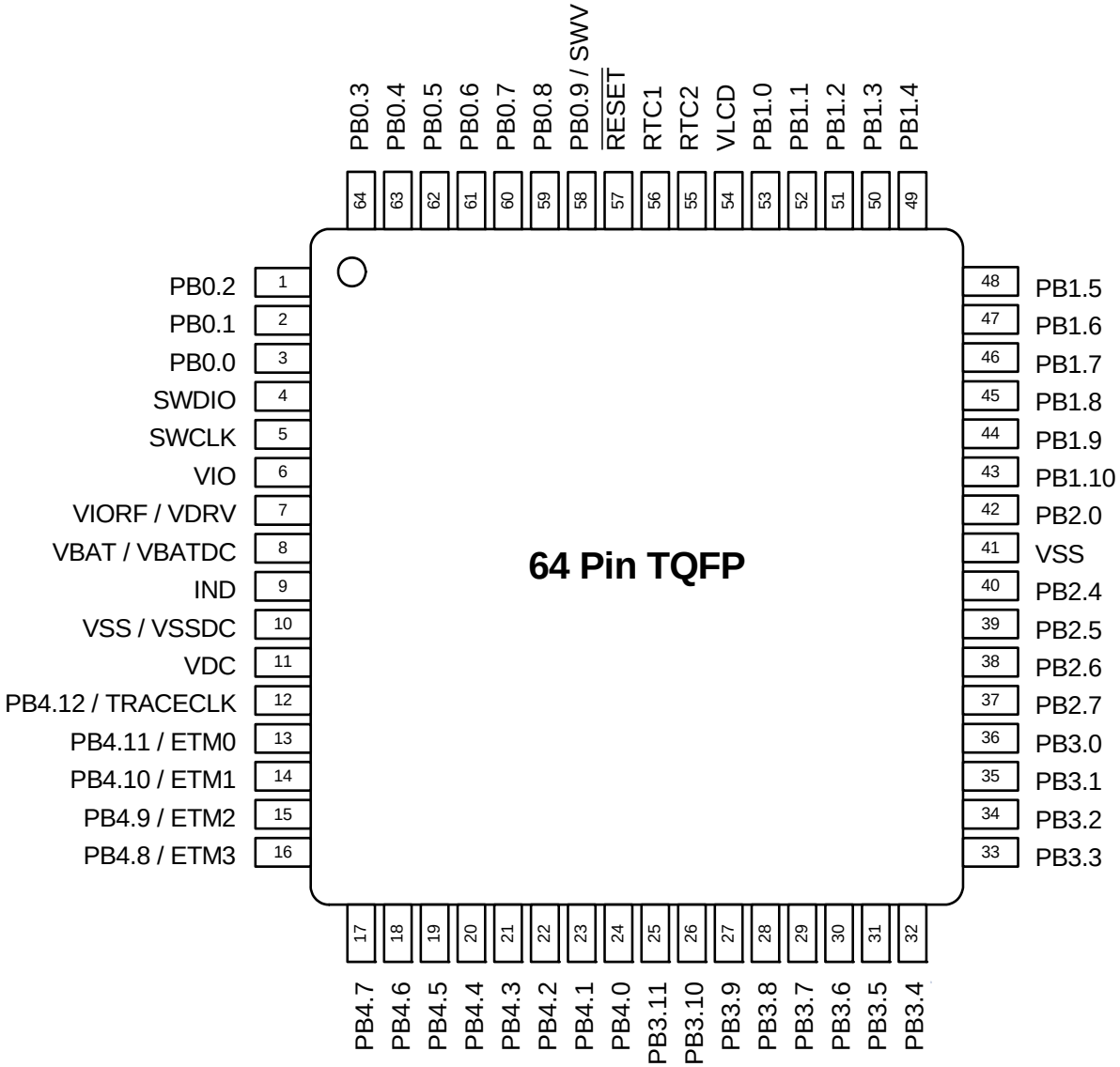


**Figure 6.2. SiM3L1x6-GQ Pinout**

**Table 6.2. Pin Definitions and Alternate Functions for SiM3L1x6**

| Pin Name | Type | Pin Numbers | I/O Voltage Domain | Crossbar Capability | Port Match | LCD Interface | Output Toggle Logic | External Trigger Inputs / Digital Functions | Analog Functions |
|---|---|---|---|---|---|---|---|---|---|
| VSS | Ground | 10<br>41 | | | | | | | |
| VSSDC | Ground (DC-DC) | 10 | | | | | | | |
| VIO | Power (I/O) | 6 | | | | | | | |
| VIORF / VDRV | Power (RF I/O) | 7 | | | | | | | |
| VBAT / VBATDC | | 8 | | | | | | | |
| VDC | | 11 | | | | | | | |
| VLCD | Power (LCD Charge Pump) | 54 | | | | | | | |
| IND | DC-DC Inductor | 9 | | | | | | | |
| $\overline{\text{RESET}}$ | Active-low Reset | 57 | | | | | | | |
| SWCLK | Serial Wire | 5 | | | | | | | |
| SWDIO | Serial Wire | 4 | | | | | | | |
| RTC1 | RTC Oscillator Input | 56 | | | | | | | |
| RTC2 | RTC Oscillator Output | 55 | | | | | | | |
| PB0.0 | Standard I/O | 3 | VIO | XBR 0 | ✓ | | ✓ | INT0.0<br>WAKE.0 | ADC0.20<br>VREF<br>CMP0P.0 |
| PB0.1 | Standard I/O | 2 | VIO | XBR 0 | ✓ | | ✓ | INT0.1<br>WAKE.2 | ADC0.22<br>CMP0N.0<br>CMP1P.0<br>XTAL2 |

**Table 6.2. Pin Definitions and Alternate Functions for SiM3L1x6 (Continued)**

| Pin Name | Type | Pin Numbers | I/O Voltage Domain | Crossbar Capability | Port Match | LCD Interface | Output Toggle Logic | External Trigger Inputs / Digital Functions | Analog Functions |
|---|---|---|---|---|---|---|---|---|---|
| PB0.2 | Standard I/O | 1 | VIO | XBR 0 | ✓ | | ✓ | INT0.2<br>WAKE.3 | ADC0.23<br>CMP1N.0<br>XTAL1 |
| PB0.3 | Standard I/O | 64 | VIO | XBR 0 | ✓ | | ✓ | INT0.3<br>WAKE.4 | ADC0.0<br>CMP0P.1<br>IDAC0 |
| PB0.4 | Standard I/O | 63 | VIO | XBR 0 | ✓ | | ✓ | INT0.4<br>WAKE.5<br>ACCTR0_STOP0 | ACCTR0_IN0 |
| PB0.5 | Standard I/O | 62 | VIO | XBR 0 | ✓ | | ✓ | INT0.5<br>WAKE.6<br>ACCTR0_STOP1 | ACCTR0_IN1 |
| PB0.6 | Standard I/O | 61 | VIO | XBR 0 | ✓ | | ✓ | INT0.6<br>WAKE.7 | ACCTR0_LCIN0 |
| PB0.7 | Standard I/O | 60 | VIO | XBR 0 | ✓ | | ✓ | LPT0T0<br>LPT0OUT0<br>INT0.7<br>WAKE.8 | ACCTR0_LCIN1 |
| PB0.8 | Standard I/O | 59 | VIO | XBR 0 | ✓ | | ✓ | LPT0T1<br>INT0.8<br>WAKE.9<br>ACCTR0_LCPUL0 | ADC0.1<br>CMP0N.1 |
| PB0.9/SWV | Standard I/O /Serial Wire Viewer | 58 | VIO | XBR 0 | ✓ | | ✓ | LPT0T2<br>INT0.9<br>WAKE.10<br>LPT0OUT1<br>ACCTR0_LCPUL1 | ADC0.2<br>CMP1P.1 |
| PB1.0 | Standard I/O | 53 | VIO | XBR 0 | ✓ | LCD0.31 | | LPT0T4<br>INT0.12<br>ACCTR0_LCBIAS0 | CMP0P.2 |

## 6.3. SiM3L1x4 Pin Definitions

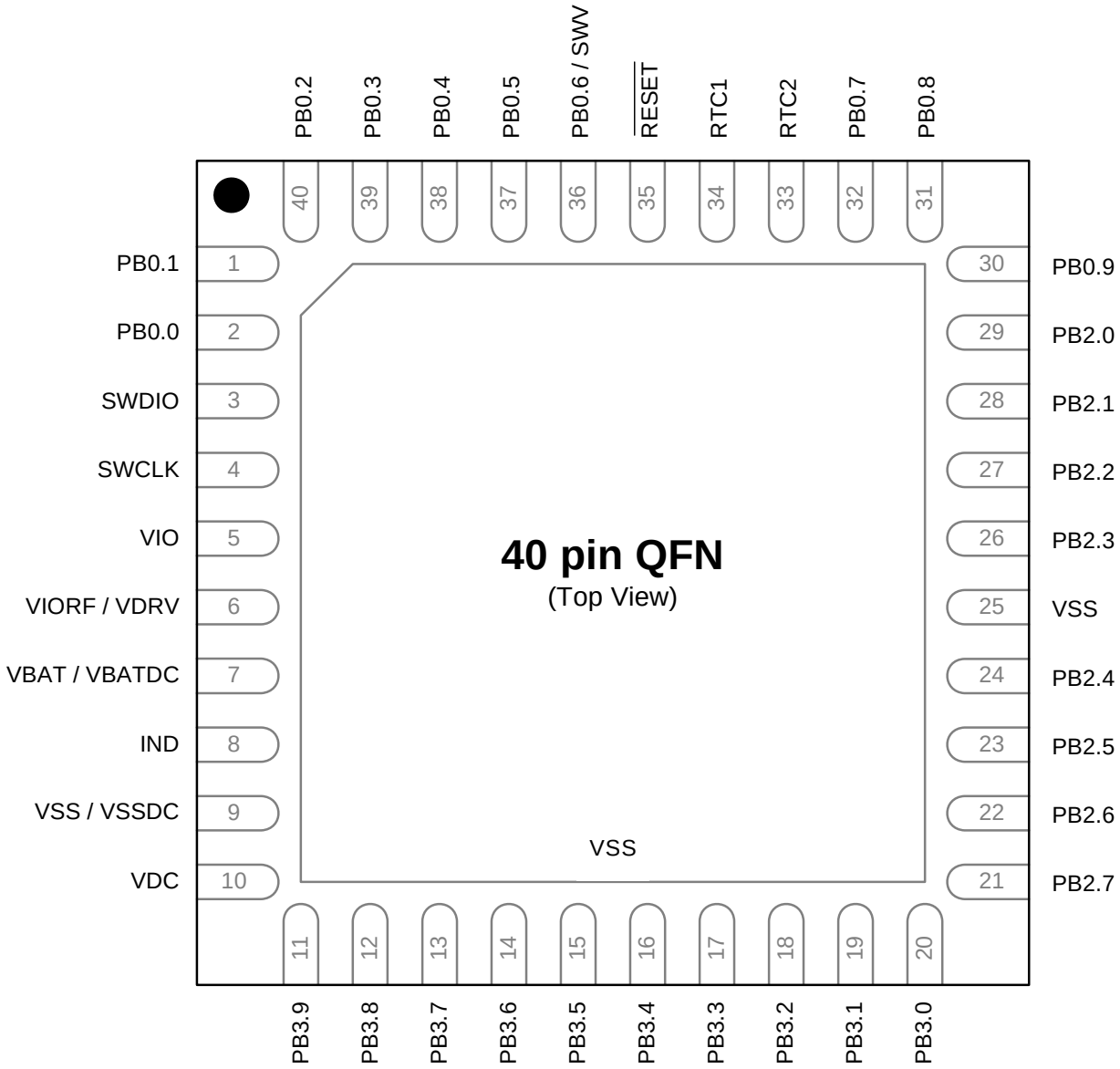


**Figure 6.4. SiM3L1x4-GM Pinout**

**Table 6.4. TQFP-80 Package Dimensions**

| Dimension | Min | Nominal | Max |
|---|---|---|---|
| A | — | — | 1.20 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| b | 0.17 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| D | 14.00 BSC | | |
| D1 | 12.00 BSC | | |
| e | 0.50 BSC | | |
| E | 14.00 BSC | | |
| E1 | 12.00 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 Ref | | |
| Θ | 0° | 3.5° | 7° |
| aaa | 0.20 | | |
| bbb | 0.20 | | |
| ccc | 0.08 | | |
| ddd | 0.08 | | |
| eee | 0.05 | | |

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant ADD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

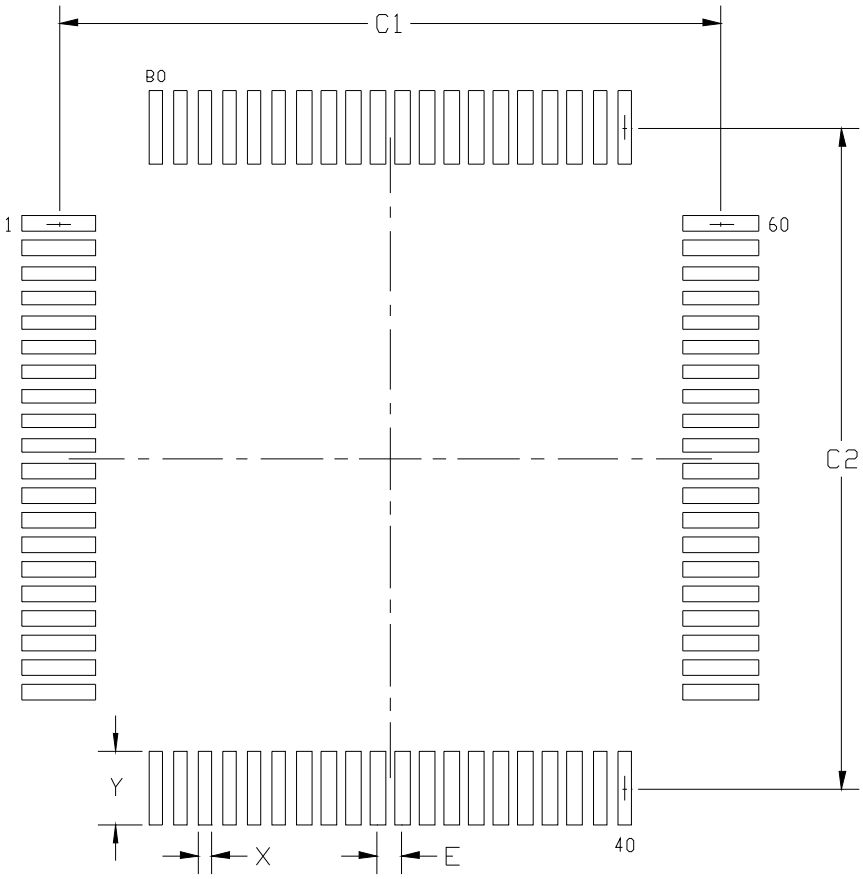


**Figure 6.6. TQFP-80 Landing Diagram**

**Table 6.5. TQFP-80 Landing Diagram Dimensions**

| Dimension | Min | Max |
|---|---|---|
| C1 | 13.30 | 13.40 |
| C2 | 13.30 | 13.40 |
| E | 0.50 BSC | |
| X | 0.20 | 0.30 |
| Y | 1.40 | 1.50 |

**Notes:**
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

### 6.4.1. TQFP-80 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

### 6.4.2. TQFP-80 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.

### 6.4.3. TQFP-80 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

**Table 6.8. TQFP-64 Package Dimensions**

| Dimension | Min | Nominal | Max |
|---|---|---|---|
| A | — | — | 1.20 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.09 | — | 0.20 |
| D | 12.00 BSC | | |
| D1 | 10.00 BSC | | |
| e | 0.50 BSC | | |
| E | 12.00 BSC | | |
| E1 | 10.00 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| Θ | 0° | 3.5° | 7° |
| aaa | — | — | 0.20 |
| bbb | — | — | 0.20 |
| ccc | — | — | 0.08 |
| ddd | — | — | 0.08 |

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant ACD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.