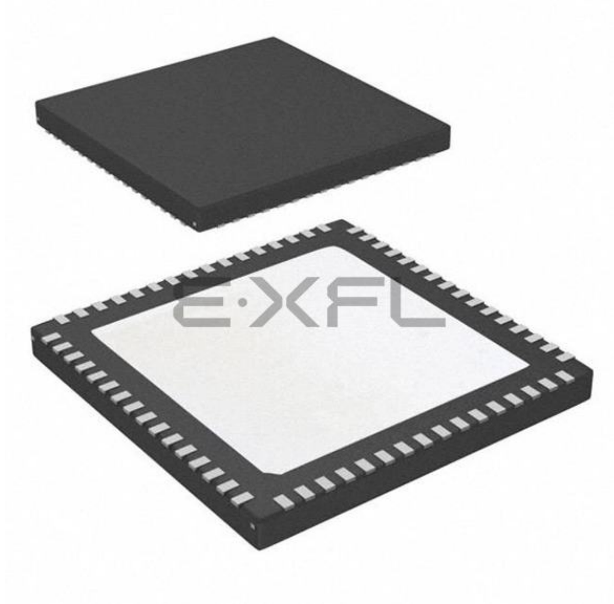

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 23x10/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/sim3l156-c-gm

Table 3.3. Power Mode Wake Up Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 2 or 6 Wake Time	t_{PM2}		4	—	5	clocks
Power Mode 3 Fast Wake Time (using LFO as clock source)	t_{PM3FW}		—	425	—	µs
Power Mode 8 Wake Time	t_{PM8}		—	3.8	—	µs

Notes:

1. Wake times are specified as the time from the wake source to the execution phase of the first instruction following WFI. This includes latency to recognize the wake event and fetch the first instruction (assuming wait states = 0).

Table 3.4. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{BAT} High Supply Monitor Threshold (VBATHITHEN = 1)	V_{VBATMH}	Early Warning	—	2.20	—	V
		Reset	1.95	2.05	2.1	V
V_{BAT} Low Supply Monitor Threshold (VBATHITHEN = 0)	V_{VBATML}	Early Warning	—	1.85	—	V
		Reset	1.70	1.75	1.77	V
Power-On Reset (POR) Threshold	V_{POR}	Rising Voltage on V_{BAT}	—	1.4	—	V
		Falling Voltage on V_{BAT}	0.8	1	1.3	V
V_{BAT} Ramp Time	t_{RMP}	Time to $V_{BAT} \geq 1.8$ V	10	—	3000	µs
Reset Delay from POR	t_{POR}	Relative to $V_{BAT} \geq V_{POR}$	3	—	100	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	10	—	µs
$\overline{\text{RESET}}$ Low Time to Generate Reset	t_{RSTL}		50	—	—	ns
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	F_{AHB} > 1 MHz	—	0.5	1.5	ms
Missing Clock Detector Trigger Frequency	F_{MCD}		—	2.5	10	kHz
V_{BAT} Supply Monitor Turn-On Time	t_{MON}		—	2	—	µs

Table 3.11. ACCTR (Advanced Capture Counter)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LC Comparator Response Time, CMPMD = 11 (Highest Speed)	t_{RESP0}	+100 mV Differential	—	100	—	ns
		–100 mV Differential	—	150	—	ns
LC Comparator Response Time, CMPMD = 00 (Lowest Power)	t_{RESP3}	+100 mV Differential	—	1.4	—	µs
		–100 mV Differential	—	3.5	—	µs
LC Comparator Positive Hysteresis Mode 0 (CPMD = 11)	HYS_{CP+}	CMPHYP = 00	—	0.37	—	mV
		CMPHYP = 01	—	7.9	—	mV
		CMPHYP = 10	—	16.7	—	mV
		CMPHYP = 11	—	32.8	—	mV
LC Comparator Negative Hysteresis Mode 0 (CPMD = 11)	HYS_{CP-}	CMPHYN = 00	—	0.37	—	mV
		CMPHYN = 01	—	–7.9	—	mV
		CMPHYN = 10	—	–16.1	—	mV
		CMPHYN = 11	—	–32.7	—	mV
LC Comparator Positive Hysteresis Mode 1 (CPMD = 10)	HYS_{CP+}	CMPHYP = 00	—	0.47	—	mV
		CMPHYP = 01	—	5.85	—	mV
		CMPHYP = 10	—	12	—	mV
		CMPHYP = 11	—	24.4	—	mV
LC Comparator Negative Hysteresis Mode 1 (CPMD = 10)	HYS_{CP-}	CMPHYN = 00	—	0.47	—	mV
		CMPHYN = 01	—	–6.0	—	mV
		CMPHYN = 10	—	–12.1	—	mV
		CMPHYN = 11	—	–24.6	—	mV
LC Comparator Positive Hysteresis Mode 2 (CPMD = 01)	HYS_{CP+}	CMPHYP = 00	—	0.66	—	mV
		CMPHYP = 01	—	4.55	—	mV
		CMPHYP = 10	—	9.3	—	mV
		CMPHYP = 11	—	19	—	mV
LC Comparator Negative Hysteresis Mode 2 (CPMD = 01)	HYS_{CP-}	CMPHYN = 00	—	0.6	—	mV
		CMPHYN = 01	—	–4.5	—	mV
		CMPHYN = 10	—	–9.5	—	mV
		CMPHYN = 11	—	–19	—	mV

Table 3.11. ACCTR (Advanced Capture Counter) (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LC Comparator Positive Hysteresis Mode 3 (CPMD = 00)	HYS_{CP+}	CMPHYP = 00	—	1.37	—	mV
		CMPHYP = 01	—	3.8	—	mV
		CMPHYP = 10	—	7.8	—	mV
		CMPHYP = 11	—	15.6	—	mV
LC Comparator Negative Hysteresis Mode 3 (CPMD = 00)	HYS_{CP-}	CMPHYN = 00	—	1.37	—	mV
		CMPHYN = 01	—	–3.9	—	mV
		CMPHYN = 10	—	–7.9	—	mV
		CMPHYN = 11	—	–16	—	mV
LC Comparator Input Range (ACCTR0_LCIN pin)	V_{IN}		–0.25	—	V_{BAT} + 0.25	V
LC Comparator Common-Mode Rejection Ratio	$CMRR_{CP}$		—	75	—	dB
LC Comparator Power Supply Rejection Ratio	$PSRR_{CP}$		—	72	—	dB
LC Comparator Input Offset Voltage	V_{OFF}	T_A = 25 °C	–10	0	10	mV
LC Comparator Input Offset Tempco	TC_{OFF}		—	3.5	—	µV/°C
Reference DAC Offset Error	DAC_{EOFF}		–1	—	1	LSB
Reference DAC Full Scale Output	DAC_{FS}	Low Range	—	V_{IO}/8	—	V
		High Range	—	V_{IO}	—	V
Reference DAC Step Size	DAC_{LSB}	Low Range (48 steps)	—	V_{IO}/384	—	V
		High Range (64 steps)	—	V_{IO}/64	—	V
LC Oscillator Period	T_{LCOSC}		—	25	—	ns
LC Bias Output Impedance	R_{LCBIAS}	10 µA Load	—	1	—	kΩ
LC Bias Drive Strength	I_{LCBIAS}		—	—	2	mA
Pull-Up Resistor Tolerance	R_{TOL}	PUVAL[4:2] = 0 to 6	-15	—	15	%
		PUVAL[4:2] = 7	-10	—	10	%

4. Precision32™ SiM3L1xx System Overview

The SiM3L1xx Precision32™ devices are fully integrated, mixed-signal system-on-a-chip MCUs. Highlighted features are listed below. Refer to Table 5.1 for specific product feature selection and part ordering numbers.

- **Core:**
  - 32-bit ARM Cortex-M3 CPU.
  - 50 MHz maximum operating frequency.
  - Branch target cache and prefetch buffers to minimize wait states.
- **Memory:** 32–256 kB flash; in-system programmable, 8–32 kB SRAM configurable to retention mode in 4 kB blocks. Blocks configured to retention mode preserve state in the low power PM8 mode.
- **Power:**
  - Three adjustable low drop-out (LDO) regulators.
  - DC-DC buck converter allows dynamic voltage scaling for maximum efficiency (250 mW output).
  - Power-on reset circuit and brownout detectors.
  - Power Management Unit (PMU).
  - Specialized charge pump reduces power consumption in low power modes.
  - Process/Voltage/Temperature (PVT) Monitor.
  - Register state retention in lowest power mode.
- **I/O:** Up to 62 contiguous 5 V tolerant I/O pins and one flexible peripheral crossbar.
- **Clock Sources:**
  - Internal oscillator with PLL: 23–50 MHz with ± 1.5% accuracy in free-running mode.
  - Low-power internal oscillator: 20 MHz.
  - Low-frequency internal oscillator: 16.4 kHz.
  - External RTC crystal oscillator: 32.768 kHz.
  - External oscillator: Crystal, RC, C, CMOS clock.
- **Integrated LCD Controller (4x40).**
- **Data Peripherals:**
  - 10-Channel DMA Controller.
  - 3 x Data Transfer Managers.
  - 128/192/256-bit Hardware AES Encryption.
  - CRC with programmable 16-bit polynomial, one 32-bit polynomial, and bus snooping capability.
  - Encoder / Decoder.
- **Timers/Counters:**
  - 3 x 32-bit Timers.
  - 1 x Enhanced Programmable Counter Array (EPCA).
  - Real Time Clock (RTC0).
  - Low Power Timer.
  - Watchdog Timer.
  - Low Power Mode Advanced Capture Counter (ACCTR).
- **Communications Peripherals:**
  - 1 x USART with IrDA and ISO7816 SmartCard support.
  - 1 x UART that operates in low power mode (PM8).
  - 2 x SPIs.
  - 1 x I2C.
- **Analog:**
  - 1 x 12-Bit Analog-to-Digital Converter (SARADC).
  - 1 x 10-Bit Digital-to-Analog Converter (IDAC).
  - 2 x Low-Current Comparators (CMP).
- **On-Chip Debugging**

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillators, the SiM3L1xx devices are truly stand-alone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing non-volatile data storage and allowing field upgrades of the firmware. User firmware has complete control of all peripherals and may individually shut down and gate the clocks of any or all peripherals for power savings.

The on-chip debugging interface (SWJ-DP) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging.

Each device is specified for 1.8 to 3.8 V operation over the industrial temperature range (–40 to +85 °C). The SiM3L1xx devices are available in 40-pin or 64-pin QFN and 64-pin or 80-pin TQFP packages. All package options are lead-free and RoHS compliant. See Table 5.1 for ordering information. A block diagram is included in Figure 4.1.

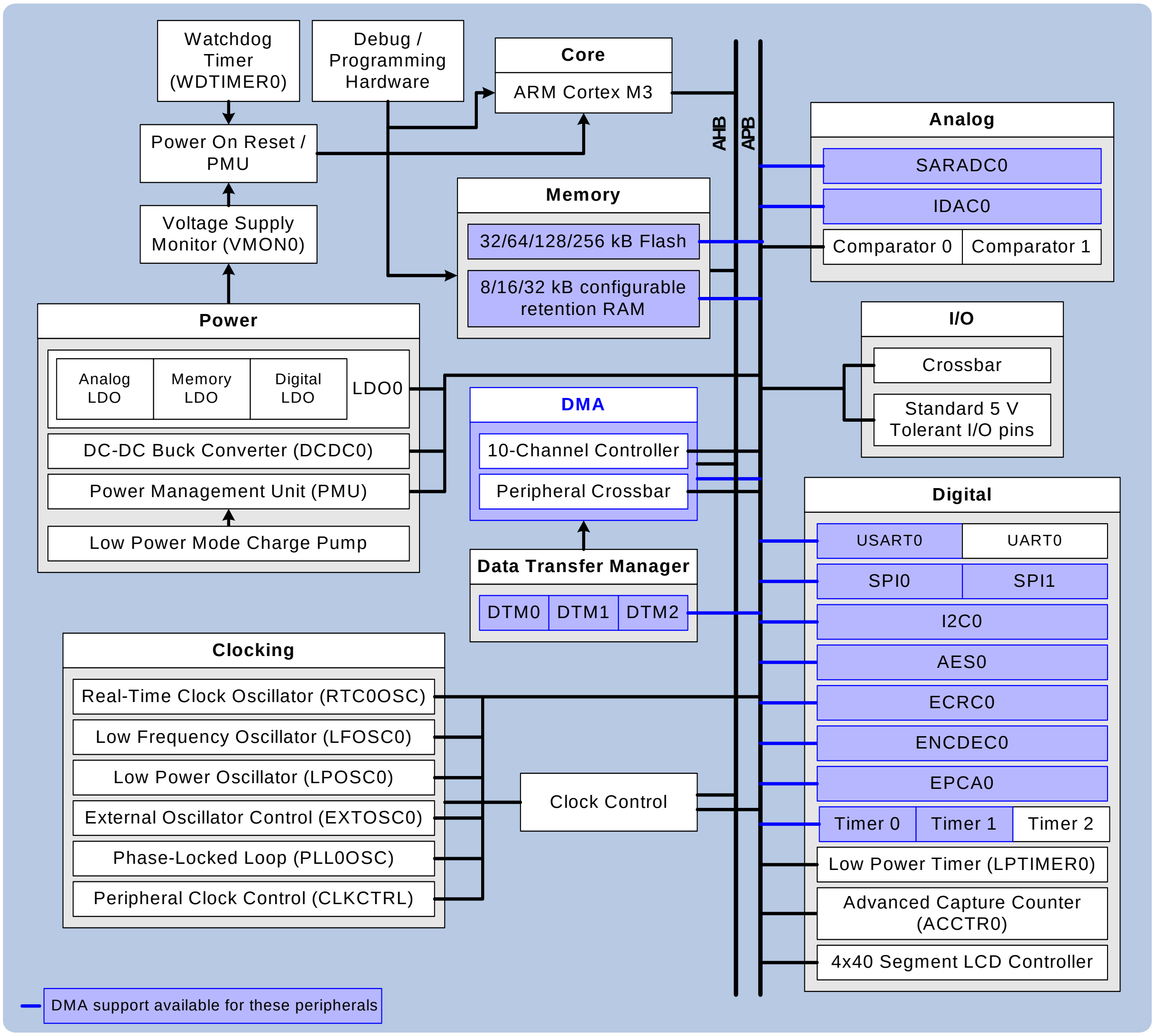

Figure 4.1. Precision32™ SiM3L1xx Family Block Diagram

4.1.5.6. Power Mode Summary

The power modes described above are summarized in Table 4.1. Table 3.2 and Table 3.3 provide more information on the power consumption and wake up times for each mode.

Table 4.1. SiM3L1xx Power Modes

Mode	Description	Notes
Normal	■ Core operating at full speed ■ Code executing from flash	■ Full device operation
Power Mode 1 (PM1)	■ Core operating at full speed ■ Code executing from RAM	■ Full device operation ■ Higher CPU bandwidth than PM0 (RAM can operate with zero wait states at any frequency)
Power Mode 2 (PM2)	■ Core halted ■ AHB, APB and all peripherals operational at full speed	■ Fast wakeup from any interrupt source
Power Mode 3 (PM3)	■ All clocks to core and peripherals stopped ■ Faster wake enabled by keeping LFOSC0 or RTC0TCLK active	■ Wake on any wake source or reset source defined in the PMU
Power Mode 4 (PM4)	■ Core operating at low speed ■ Code executing from flash	■ Same capabilities as PM0, operating at lower speed ■ Lower clock speed enables lower LDO output settings to save power
Power Mode 5 (PM5)	■ Core operating at low speed ■ Code executing from RAM	■ Same capabilities as PM1, operating at lower speed ■ Lower clock speed enables lower LDO output settings to save power
Power Mode 6 (PM6)	■ Core halted ■ AHB, APB and all peripherals operational at low speed	■ Same capabilities as PM2, operating at lower speed ■ Lower clock speed enables lower LDO output settings to save power ■ When running from LFOSC0, power is similar to PM3, but the device wakes much faster
Power Mode 8 (PM8)	■ Low power sleep ■ LDO regulators are disabled and all active circuitry operates directly from VBAT ■ The following functions are available: ACCTR0, RTC0, UART0 running from RTC0TCLK, LPTIMER0, port match, and the LCD controller ■ Register and RAM state retention	■ Lowest power consumption ■ Wake on any wake source or reset source defined in the PMU

4.2. I/O

4.2.1. General Features

The SiM3L1xx ports have the following features:

- 5 V tolerant.
- Push-pull or open-drain output modes to the VIO or VIORF voltage level.
- Analog or digital modes.
- Option for high or low output drive strength.
- Port Match allows the device to recognize a change on a port pin value.
- Internal pull-up resistors are enabled or disabled on a port-by-port basis.
- Two external interrupts with up to 16 inputs each provide monitoring capability for external signals.
- Internal Pulse Generator Timer (PB0 only) to generate simple square waves and pulses.

4.2.2. Crossbar

The SiM3L1xx devices have one crossbar with the following features:

- Flexible peripheral assignment to port pins.
- Pins can be individually skipped to move peripherals as needed for design or layout considerations.

The crossbar has a fixed priority for each I/O function and assigns these functions to the port pins. When a digital resource is selected, the least-significant unassigned port pin is assigned to that resource. If a port pin is assigned, the crossbar skips that pin when assigning the next selected resource. Additionally, the crossbar will skip port pins whose associated bits in the PBSKIPEN registers are set. This provides flexibility when designing a system: pins involved with sensitive analog measurements can be moved away from digital I/O, and peripherals can be moved around the chip as needed to ease layout constraints.

4.3. Clocking

The SiM3L1xx devices have two system clocks: AHB and APB. The AHB clock services memory peripherals and is derived from one of seven sources: the RTC timer clock (RTC0TCLK), the Low Frequency Oscillator, the Low Power Oscillator, the divided Low Power Oscillator, the External Oscillator, the PLL0 Oscillator, and the VIORFCLK pin input. In addition, a divider for the AHB clock provides flexible clock options for the device. The APB clock services data peripherals and is synchronized with the AHB clock. The APB clock can be equal to the AHB clock or set to the AHB clock divided by two.

The Clock Control module on SiM3L1xx devices allows the AHB and APB clocks to be turned off to unused peripherals to save system power. Any registers in a peripheral with disabled clocks will be unable to be accessed until the clocks are enabled. Most peripherals have clocks off by default after a power-on reset.

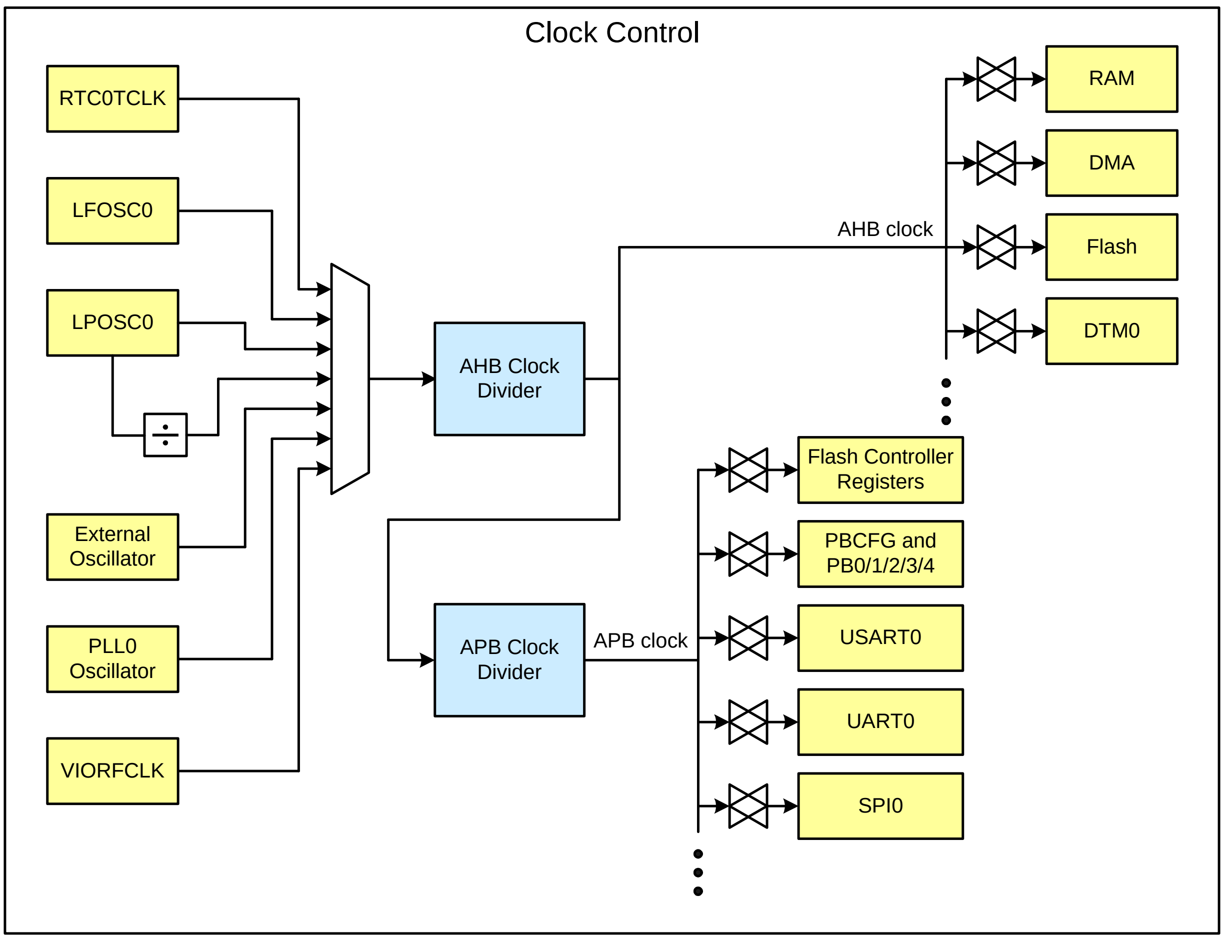

Figure 4.3. SiM3L1xx Clocking

4.4. Integrated LCD Controller (LCD0)

SiM3L1xx devices contain an LCD segment driver and on-chip bias generation that supports static, 2-mux, 3-mux and 4-mux LCDs with 1/2 or 1/3 bias. The on-chip charge pump with programmable output voltage allows software contrast control which is independent of the supply voltage. LCD timing is derived from the RTC timer clock (RTC0TCLK) to allow precise control over the refresh rate.

The SiM3L1xx devices use registers to store the enabled/disabled state of individual LCD segments. All LCD waveforms are generated on-chip based on the contents of these registers with flexible waveform control to reduce power consumption wherever possible. An LCD blinking function is also supported on a subset of LCD segments.

The LCD0 module has the following features:

- Up to 40 segment pins and 4 common pins.
- Supports LCDs with 1/2 or 1/3 bias.
- Includes an on-chip charge pump with programmable output that allows firmware to control the contrast independent of the supply voltage.
- The RTC timer clock (RTC0TCLK) determines the LCD timing and refresh rate.
- All LCD waveforms are generated on-chip based on the contents of the LCD0 registers with flexible waveform control.
- LCD segments can be placed in a discharge state for a configurable number of RTC clock cycles before switching to the next state to reduce power consumption due to display loading.
- Includes a VBAT monitor that can serve as a wakeup source for Power Mode 8.
- Supports four hardware auto-contrast modes: bypass, constant, minimum, and auto-bypass.
- Supports hardware blinking for up to 8 segments.

4.6.3. Real-Time Clock (RTC0)

The RTC module includes a 32-bit timer that allows up to 36 hours of independent time-keeping when used with a 32.768 kHz watch crystal. The RTC provides three alarm events in addition to a missing clock event, which can also function as interrupt, reset, or wakeup sources on SiM3L1xx devices.

The RTC module includes internal loading capacitors that are programmable to 16 discrete levels, allowing compatibility with a wide range of crystals.

The RTC timer clock can be buffered and routed to a port bank pin to provide an accurate, low frequency clock to other devices while the core is in its lowest power down mode. The module also includes a low power internal low frequency oscillator that reduces low power mode current and is available for other modules to use as a clock source.

The RTC module includes the following features:

- 32-bit timer (supports up to 36 hours) with three separate alarms.
- Option for one alarm to automatically reset the RTC timer.
- Missing clock detector.
- Can be used with the internal Low Frequency Oscillator or with an external 32.768 kHz crystal (no additional resistors or capacitors necessary).
- Programmable internal loading capacitors support a wide range of external 32.768 kHz crystals.
- The RTC timer clock (RTC0CLK) can be buffered and routed to an I/O pin to provide an accurate, low frequency clock to other devices while the core is in its lowest power down mode.
- The RTC module can be powered from the low power mode charge pump for lowest possible power consumption while in PM8.

4.6.4. Low Power Timer (LPTIMER0)

The Low Power Timer (LPTIMER) module runs from the RTC timer clock (RTC0CLK), allowing the LPTIMER to operate even if the AHB and APB clocks are disabled. The LPTIMER counter can increment using one of two clock sources: the clock selected by the RTC0 module, or rising or falling edges of an external signal.

The Low Power Timer includes the following features:

- Runs on low-frequency RTC timer clock (RTC0TCLK).
- The LPTIMER counter can increment using one of two clock sources: the RTC0TCLK or rising or falling edges of an external signal.
- Overflow and threshold-match detection.
- Timer reset on threshold-match allows square-wave generation at a variable output frequency.
- Supports PWM with configurable period and duty cycle.
- The LPTIMER module can be powered from the low power mode charge pump for lowest possible power consumption while in PM8.

4.6.5. Watchdog Timer (WDTIMER0)

The WDTIMER module includes a 16-bit timer, a programmable early warning interrupt, and a programmable reset period. The timer registers are protected from inadvertent access by an independent lock and key interface.

The watchdog timer runs from the low frequency oscillator (LFOSC0).

The Watchdog Timer has the following features:

- Programmable timeout interval.
- Optional interrupt to warn when the Watchdog Timer is nearing the reset trip value.
- Lock-out feature to prevent any modification until a system reset.

4.6.6. Low Power Mode Advanced Capture Counter (ACCTR0)

The SiM3L1xx devices contain a low-power Advanced Capture Counter module that runs from the RTC0 clock domain and can be used with digital inputs, switch topology circuits (reed switches), or with LC resonant circuits. For switch topology circuits, the module charges one or two external lines by pulsing internal pull-up resistors and detecting whether the reed switch is open or closed. For LC resonant circuits, the inputs are periodically energized to produce a dampened sine wave and configurable discriminator circuits detect the resulting decay time-constant.

The advanced capture counter has the following general features:

- Single or differential inputs supporting single, dual, and quadrature modes of operation.
- Variety of interrupt and PM8 wake up sources.
- Provides feedback of the direction history, current and previous states, and condition flags.

The advanced capture counter has the following features for switch circuit topologies:

- Ultra low power input comparators.
- Supports a wide range of pull-up resistor values with a self-calibration engine.
- Asymmetrical integrators for low-pass filtering and switch debounce.
- Two 24-bit counters and two 24-bit digital threshold comparators.
- Supports switch flutter detection.

For LC resonant circuit topologies, the advanced capture counter includes:

- Separate minimum and maximum count registers and polarity, pulse, and toggle controls.
- Zone-based programmable timing.
- Two input comparators with support for a positive side input bias at VIO divided by 2.
- Supports a configurable excitation pulse width based on a 40 MHz oscillator and timer or an external digital stop signal.
- Two 8-bit peak counters that saturate at full scale for detecting the number of LC resonant peaks.
- Two discriminators with programmable thresholds.
- Supports a sample and hold mode for Wheatstone bridges.

All devices in the SiM3L1xx family include the low power mode advanced capture counter (ACCTR0). Table 4.2 lists the supported inputs and outputs for each of the packages.

Table 4.2. SiM3L1xx Supported Advanced Capture Counter Inputs and Outputs

Input/Output	SiM3L1x7	SiM3L1x6	SiM3L1x4
ACCTR0_IN0	✓	✓	✓
ACCTR0_IN1	✓	✓	✓
ACCTR0_LCIN0	✓	✓	
ACCTR0_LCIN1	✓	✓	✓
ACCTR0_STOP0	✓	✓	✓
ACCTR0_STOP1	✓	✓	✓
ACCTR0_LCPUL0	✓	✓	
ACCTR0_LCPUL1	✓	✓	
ACCTR0_LCBIAS0	✓	✓	
ACCTR0_LCBIAS1	✓	✓	
ACCTR0_DBG0	✓	✓	
ACCTR0_DBG1	✓	✓	

4.7. Communications Peripherals

4.7.1. USART (USART0)

The USART uses two signals (TX and RX) to communicate serially with an external device. In addition to these signals, the USART module can optionally use a clock (UCLK) or hardware handshaking (RTS and CTS).

The USART module provides the following features:

- Independent transmitter and receiver configurations with separate 16-bit baud rate generators.
- Synchronous or asynchronous transmissions and receptions.
- Clock master or slave operation with programmable polarity and edge controls.
- Up to 5 Mbaud (synchronous or asynchronous, TX or RX, and master or slave) or 1 Mbaud Smartcard (TX or RX).
- Individual enables for generated clocks during start, stop, and idle states.
- Internal transmit and receive FIFOs with flush capability and support for byte, half-word, and word reads and writes.
- Data bit lengths from 5 to 9 bits.
- Programmable inter-packet transmit delays.
- Auto-baud detection with support for the LIN SYNC byte.
- Automatic parity generation (with enable).
- Automatic start and stop generation (with separate enables).
- Transmit and receive hardware flow-control.
- Independent inversion correction for TX, RX, RTS, and CTS signals.
- IrDA modulation and demodulation with programmable pulse widths.
- Smartcard ACK/NACK support.
- Parity error, frame error, overrun, and underrun detection.
- Multi-master and half-duplex support.
- Multiple loop-back modes supported.
- Multi-processor communications support.

4.7.2. UART (UART0)

The low-power UART uses two signals (TX and RX) to communicate serially with an external device.

The UART0 module can operate in PM8 mode by taking the clock directly from the RTC0 time clock (RTC0TCLK) and running from the low power mode charge pump. This will allow the system to conserve power while transmitting or receiving UART traffic. The UART supports standard baud-rates of 9600, 4800, 2400 and 1200 in this low power mode.

The UART0 module provides the following features:

- Independent transmitter and receiver configurations with separate 16-bit baud rate generators.
- Asynchronous transmissions and receptions.
- Up to 5 Mbaud (TX or RX).
- Internal transmit and receive FIFOs with flush capability and support for byte, half-word, and word reads and writes.
- Data bit lengths from 5 to 9 bits.
- Programmable inter-packet transmit delays.
- Auto-baud detection with support for the LIN SYNC byte.
- Automatic parity generation (with enable).
- Automatic start and stop generation (with separate enables).
- Independent inversion correction for TX and RX signals.
- Parity error, frame error, overrun, and underrun detection.
- Half-duplex support.

4.10. Security

The peripherals on the SiM3L1xx devices have a register lock and key mechanism that prevents undesired accesses of the peripherals from firmware. Each bit in the PERIPHLOCKx registers controls a set of peripherals. A key sequence must be written to the KEY register to modify bits in PERIPHLOCKx. Any subsequent write to KEY will then inhibit accesses of PERIPHLOCKx until it is unlocked again through KEY. Reading the KEY register indicates the current status of the PERIPHLOCKx lock state.

If a peripheral's registers are locked, all writes will be ignored. The registers can be read, regardless of the peripheral's lock state.

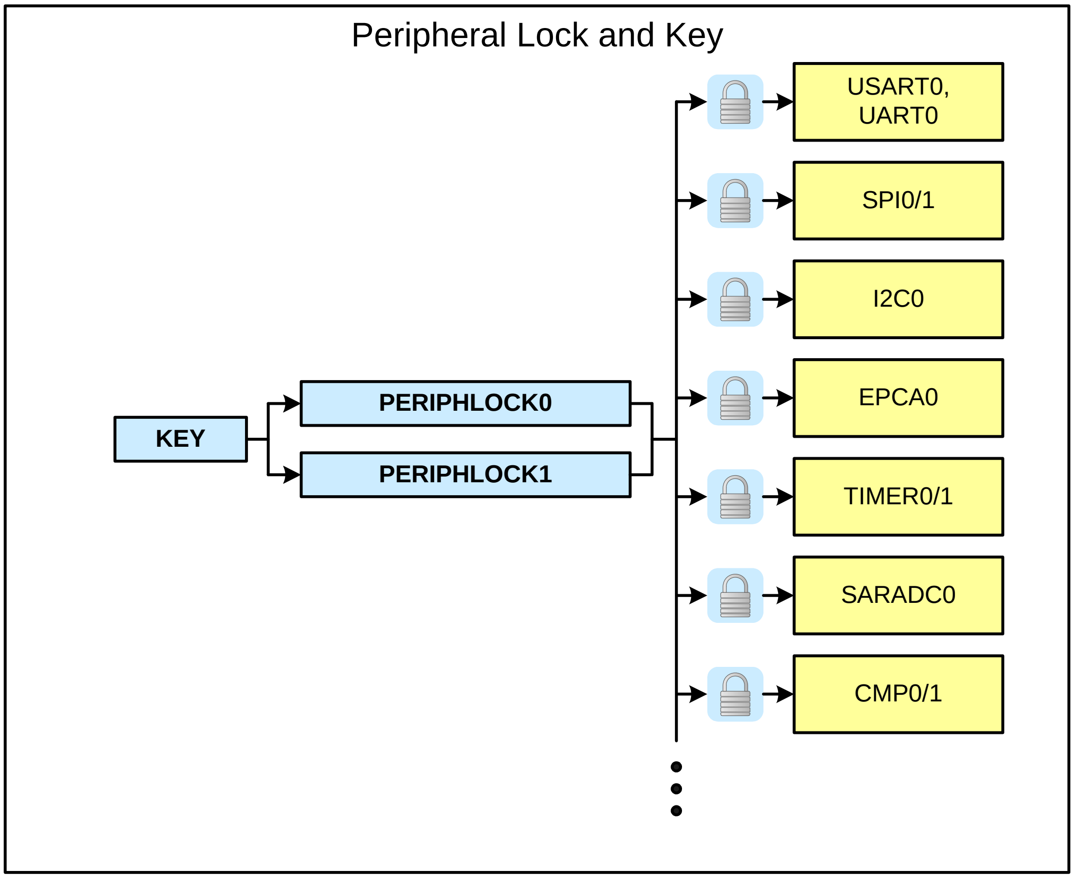

Figure 4.5. SiM3L1xx Security Block Diagram

4.11. On-Chip Debugging

The SiM3L1xx devices include JTAG and Serial Wire programming and debugging interfaces and ETM for instruction trace. The JTAG interface is supported on SiM3L1x7 devices only, and does not include boundary scan capabilites. The ETM interface is supported on SiM3L1x7, and SiM3L1x6 devices only. The JTAG and ETM interfaces can be optionally enabled to provide more visibility while debugging at the cost of using several Port I/O pins. Additionally, if the core is configured for Serial Wire (SW) mode and not JTAG, then the Serial Wire Viewer (SWV) is available to provide a single pin to send out TPIU messages. Serial Wire Viewer is supported on all SiM3Lxxx devices.

Most peripherals on SiM3L1xx devices have the option to halt or continue functioning when the core halts in debug mode.

5. Ordering Information

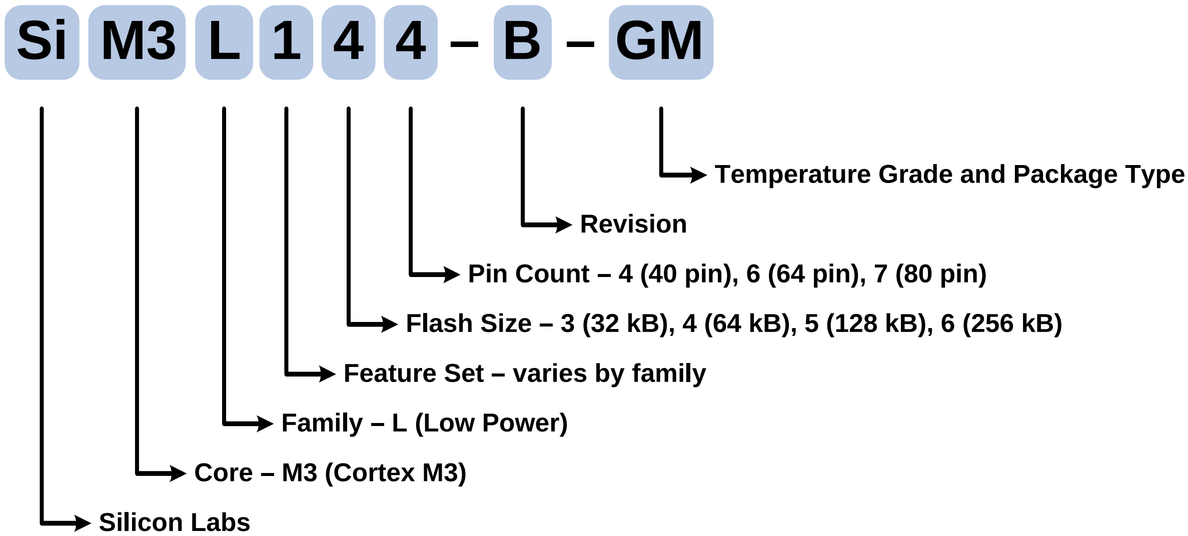

Figure 5.1. SiM3L1xx Part Numbering

All devices in the SiM3L1xx family have the following features:

- **Core:** ARM Cortex-M3 with maximum operating frequency of 50 MHz.
- **PLL.**
- **10-Channel DMA Controller.**
- **128/192/256-bit AES.**
- **16/32-bit CRC.**
- **Encoder/Decoder.**
- **DC-DC Buck Converter.**
- **Timers:** 3 x 32-bit (6 x 16-bit).
- **Real-Time Clock.**
- **Low-Power Timer.**
- **PCA:** 1 x 6 channels (Enhanced)
- **ADC:** 12-bit 250 ksps (10-bit 1 Msps) SAR.
- **DAC:** 10-bit IDAC.
- **Temperature Sensor.**
- **Internal VREF.**
- **Comparator:** 2 x low current.
- **Serial Buses:** 2 x USART, 2 x SPI, 1 x I2C

Additionally, all devices in the SiM3L1xx family include the low power mode advanced capture counter (ACCTR0), though the smaller packages (SiM3L1x4) only support some of the external inputs and outputs.

Table 5.1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	RAM (kB)	LCD Segments	Digital Port I/Os	Digital Port I/Os on the Crossbar	Number of SARADC0 Channels	Number of Comparator 0/1 Inputs (+/-)	Number of PMU Pin Wake Sources	Number of ACCTR0 Inputs and Outputs	JTAG Debugging Interface	ETM Debugging Interface	Serial Wire Debugging Interface	Lead-free (RoHS Compliant)	Package
SiM3L167-C-GQ	256	32	160 (4x40)	62	38	24	15/15	14	12	✓	✓	✓	✓	TQFP-80
SiM3L166-C-GM	256	32	128 (4x32)	51	34	23	14/12	11	12		✓	✓	✓	QFN-64
SiM3L166-C-GQ	256	32	128 (4x32)	51	34	23	14/12	11	12		✓	✓	✓	TQFP-64
SiM3L164-C-GM	256	32		28	26	20	9/10	11	5			✓	✓	QFN-40
SiM3L157-C-GQ	128	32	160 (4x40)	62	38	24	15/15	14	12	✓	✓	✓	✓	TQFP-80
SiM3L156-C-GM	128	32	128 (4x32)	51	34	23	14/12	11	12		✓	✓	✓	QFN-64
SiM3L156-C-GQ	128	32	128 (4x32)	51	34	23	14/12	11	12		✓	✓	✓	TQFP-64
SiM3L154-C-GM	128	32		28	26	20	9/10	11	5			✓	✓	QFN-40
SiM3L146-C-GM	64	16	128 (4x32)	51	34	23	14/12	11	12		✓	✓	✓	QFN-64
SiM3L146-C-GQ	64	16	128 (4x32)	51	34	23	14/12	11	12		✓	✓	✓	TQFP-64
SiM3L144-C-GM	64	16		28	26	20	9/10	11	5			✓	✓	QFN-40
SiM3L136-C-GM	32	8	128 (4x32)	51	34	23	14/12	11	12		✓	✓	✓	QFN-64
SiM3L136-C-GQ	32	8	128 (4x32)	51	34	23	14/12	11	12		✓	✓	✓	TQFP-64
SiM3L134-C-GM	32	8		28	26	20	9/10	11	5			✓	✓	QFN-40

Table 6.2. Pin Definitions and Alternate Functions for SiM3L1x6

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
VSS	Ground	10 41							
VSSDC	Ground (DC-DC)	10							
VIO	Power (I/O)	6							
VIORF / VDRV	Power (RF I/O)	7							
VBAT / VBATDC		8							
VDC		11							
VLCD	Power (LCD Charge Pump)	54							
IND	DC-DC Inductor	9							
$\overline{\text{RESET}}$	Active-low Reset	57							
SWCLK	Serial Wire	5							
SWDIO	Serial Wire	4							
RTC1	RTC Oscillator Input	56							
RTC2	RTC Oscillator Output	55							
PB0.0	Standard I/O	3	VIO	XBR0	✓		✓	INT0.0 WAKE.0	ADC0.20 VREF CMP0P.0
PB0.1	Standard I/O	2	VIO	XBR0	✓		✓	INT0.1 WAKE.2	ADC0.22 CMP0N.0 CMP1P.0 XTAL2

Table 6.2. Pin Definitions and Alternate Functions for SiM3L1x6 (Continued)

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB4.0	Standard I/O	24	VIO		✓	COM0.1			
PB4.1	Standard I/O	23	VIO		✓	COM0.0			
PB4.2	Standard I/O	22	VIO		✓	LCD0.10			ADC0.19
PB4.3	Standard I/O	21	VIO		✓	LCD0.9			
PB4.4	Standard I/O	20	VIO		✓	LCD0.8			
PB4.5	Standard I/O	19	VIO		✓	LCD0.7			
PB4.6	Standard I/O	18	VIO		✓	LCD0.6		PMU_Asleep	
PB4.7	Standard I/O	17	VIO		✓	LCD0.5			
PB4.8/ETM3	Standard I/O / ETM	16	VIO		✓	LCD0.4			
PB4.9/ETM2	Standard I/O / ETM	15	VIO		✓	LCD0.3			
PB4.10/ ETM1	Standard I/O / ETM	14	VIO		✓	LCD0.2			
PB4.11/ ETM0	Standard I/O / ETM	13	VIO		✓	LCD0.1			
PB4.12/ TRACECLK	Standard I/O / ETM	12	VIO		✓	LCD0.0			

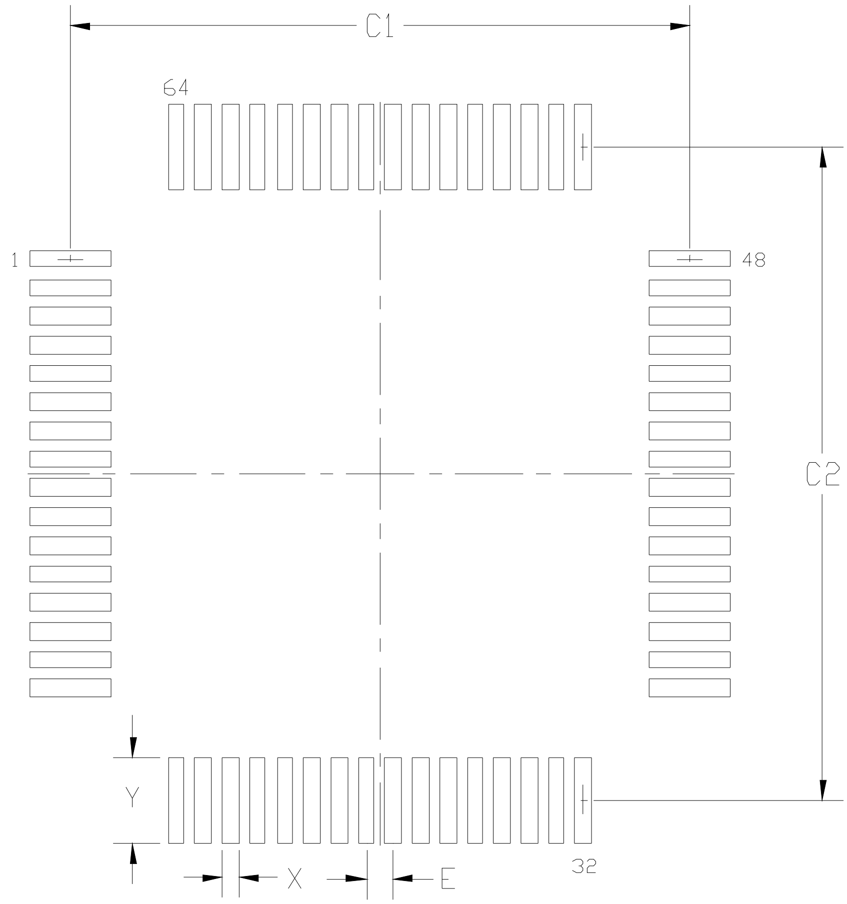

Figure 6.10. TQFP-64 Landing Diagram

Table 6.9. TQFP-64 Landing Diagram Dimensions

Dimension	Min	Max
C1	11.30	11.40
C2	11.30	11.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

7. Revision Specific Behavior

This chapter describes any differences between released revisions of the device.

7.1. Revision Identification

The Lot ID Code on the top side of the device package can be used for decoding device revision information. Figures 7.1, 7.2, and 7.3 show how to find the Lot ID Code on the top side of the device package.

In addition, firmware can determine the revision of the device by checking the DEVICEID registers.

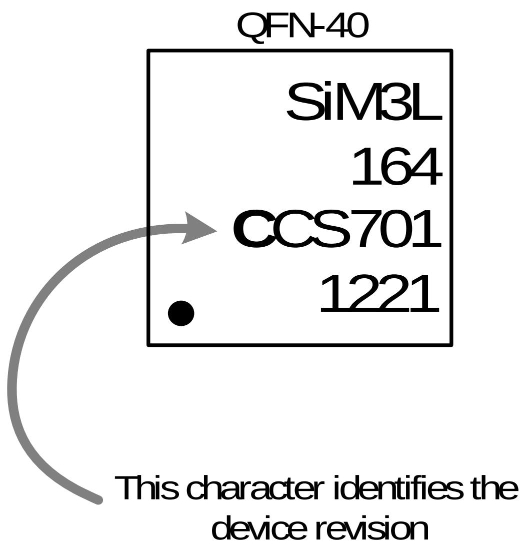

Figure 7.1. SiM3L1x7-GQ Revision Information

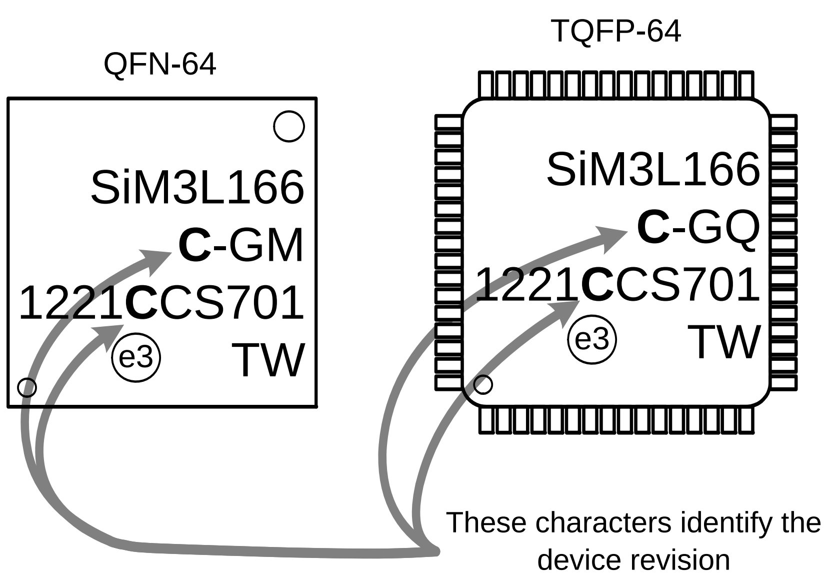

Figure 7.2. SiM3L1x6-GM and SiM3L1x6-GQ Revision Information

Document Change List

Revision 0.5 to Revision 1.0

- Updated Electrical Specifications Tables with latest characterization data and production test limits.
- Added missing signal ACCTR0_LCPUL1 to Table 6.2, “Pin Definitions and Alternate Functions for SiM3L1x6,” on page 64.
- Removed ACCTR0_LCIN1 and ACCTR0_STOP0/1 signals from Table 6.3, “Pin Definitions and Alternate Functions for SiM3L1x4,” on page 70.
- Updated Figure 6.8, “TFBGA-80 Package Drawing,” on page 79.

Revision 1.0 to Revision 1.1

- Removed all references to BGA-80 and the parts SiM3L167-C-GL and SiM3L157-C-GL.