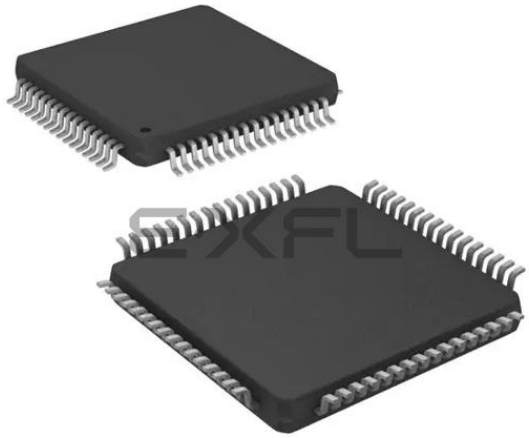

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 23x10/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/sim3l156-c-gq

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Table 3.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current						
Normal Mode[1,2,3,4]—Full speed with code executing from flash, peripheral clocks ON	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	17.5	18.9	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	6.7	7.2	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	1.15	1.4	mA
Normal Mode[1,2,3,4]—Full speed with code executing from flash, peripheral clocks OFF	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	13.3	14.5	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	5.4	5.9	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	980	1.2	µA
Normal Mode[1,2,3,4]—Full speed with code executing from flash, LDOs powered by dc-dc at 1.9 V, peripheral clocks OFF	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz V_{BAT} = 3.3 V	—	9.7	—	mA
		F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz V_{BAT} = 3.8 V	—	8.65	—	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz V_{BAT} = 3.3 V	—	4.15	—	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz V_{BAT} = 3.8 V	—	3.9	—	mA

Notes:

1. Currents are additive. For example, where I_{BAT} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded I_{VIO} is included in all I_{BAT} PM8 production test measurements.

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 2[1,2,3,4,5]—Core halted with only Port I/O clocks on (wake from pin).	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	4	7.2	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	1.47	—	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	430	—	µA
Power Mode 3[1,2,6]—Fast-Wake Mode (PM3CLKEN = 1)	I_{BAT}	V_{BAT} = 3.8 V	—	320	530	µA
		V_{BAT} = 1.8 V	—	225	—	µA
Power Mode 4[1,2,4,6]—Slower clock speed with code executing from flash, peripheral clocks ON	I_{BAT}	F_{AHB} = F_{APB} = 16 kHz, V_{BAT} = 3.8 V	—	385	640	µA
		F_{AHB} = F_{APB} = 16 kHz, V_{BAT} = 1.8 V	—	330	—	µA
Power Mode 5[1,2,4,6]—Slower clock speed with code executing from RAM, peripheral clocks ON	I_{BAT}	F_{AHB} = F_{APB} = 16 kHz, V_{BAT} = 3.8 V	—	320	490	µA
		F_{AHB} = F_{APB} = 16 kHz, V_{BAT} = 1.8 V	—	275	—	µA
Power Mode 6[1,2,4,6]—Core halted with peripheral clocks ON	I_{BAT}	F_{AHB} = F_{APB} = 16 kHz, V_{BAT} = 3.8 V	—	315	490	µA
		F_{AHB} = F_{APB} = 16 kHz, V_{BAT} = 1.8 V	—	270	—	µA
Power Mode 8[1,2]—Low Power Sleep, powered through VBAT, VIO, and VIORF at 2.4 V, 32kB of retention RAM	I_{BAT}	RTC Disabled, T_A = 25 °C	—	75	400	nA
		RTC w/ 16.4 kHz LFO, T_A = 25 °C	—	360	—	nA
		RTC w/ 32.768 kHz Crystal, T_A = 25 °C	—	670	—	nA

Notes:

1. Currents are additive. For example, where I_{BAT} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded I_{VIO} is included in all I_{BAT} PM8 production test measurements.

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SARADC0	I_{SARADC}	Sampling at 1 Msps, Internal VREF used	—	1.2	1.6	mA
		Sampling at 250 ksps, lowest power mode settings.	—	390	540	µA
Temperature Sensor	I_{TSENSE}		—	75	110	µA
Internal SAR Reference	I_{REFFS}	Normal Power Mode	—	680	—	µA
		Normal Power Mode	—	160	—	µA
VREF0	I_{REFP}		—	80	—	µA
Comparator 0 (CMP0), Comparator 1 (CMP1)	I_{CMP}	CMPMD = 11	—	0.5	2	µA
		CMPMD = 10	—	3	8	µA
		CMPMD = 01	—	10	16	µA
		CMPMD = 00	—	25	42	µA
IDAC0[8]	I_{IDAC}		—	70	100	µA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	10	22	µA
Flash Current on VBAT						
Write Operation	$I_{FLASH-W}$		—	—	8	mA
Erase Operation	$I_{FLASH-E}$		—	—	15	mA

Notes:

1. Currents are additive. For example, where I_{BAT} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded I_{VIO} is included in all I_{BAT} PM8 production test measurements.

Table 3.3. Power Mode Wake Up Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 2 or 6 Wake Time	t_{PM2}		4	—	5	clocks
Power Mode 3 Fast Wake Time (using LFO as clock source)	t_{PM3FW}		—	425	—	µs
Power Mode 8 Wake Time	t_{PM8}		—	3.8	—	µs

Notes:
1. Wake times are specified as the time from the wake source to the execution phase of the first instruction following WFI. This includes latency to recognize the wake event and fetch the first instruction (assuming wait states = 0).

Table 3.4. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{BAT} High Supply Monitor Threshold (VBATHITHEN = 1)	V_{VBATMH}	Early Warning	—	2.20	—	V
		Reset	1.95	2.05	2.1	V
V_{BAT} Low Supply Monitor Threshold (VBATHITHEN = 0)	V_{VBATML}	Early Warning	—	1.85	—	V
		Reset	1.70	1.75	1.77	V
Power-On Reset (POR) Threshold	V_{POR}	Rising Voltage on V_{BAT}	—	1.4	—	V
		Falling Voltage on V_{BAT}	0.8	1	1.3	V
V_{BAT} Ramp Time	t_{RMP}	Time to $V_{BAT} \geq 1.8$ V	10	—	3000	µs
Reset Delay from POR	t_{POR}	Relative to $V_{BAT} \geq V_{POR}$	3	—	100	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	10	—	µs
$\overline{\text{RESET}}$ Low Time to Generate Reset	t_{RSTL}		50	—	—	ns
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	$F_{AHB} > 1$ MHz	—	0.5	1.5	ms
Missing Clock Detector Trigger Frequency	F_{MCD}		—	2.5	10	kHz
V_{BAT} Supply Monitor Turn-On Time	t_{MON}		—	2	—	µs

Table 3.5. On-Chip Regulators (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Memory LDO Output Setting[5]	V_{LDOMEM}	During Programming	1.8	—	1.9	V
		During Normal Operation	1.5	—	1.9	V
Digital LDO Output Setting	V_{LDODIG}	$F_{AHB} \leq 20$ MHz	1.0	—	1.9	V
		$F_{AHB} > 20$ MHz	1.2	—	1.9	V
Analog LDO Output Setting During Normal Operation[6]	V_{LDOANA}		1.8			V

Notes:

1. See reference manual for recommended inductors.
2. Recommended: X7R or X5R ceramic capacitors with low ESR. Example: Murata GRM21BR71C225K with ESR < 10 mΩ (@ frequency > 1 MHz).
3. Input voltage specification accounts for the internal LDO dropout voltage under the maximum load condition to ensure that the LDO output voltage will remain at a valid level as long as V_{LDOIN} is at or above the specified minimum.
4. The memory LDO output should always be set equal to or lower than the output of the analog LDO. When lowering both LDOs (for example to go into PM8 under low supply conditions), first adjust the memory LDO and then the analog LDO. When raising the output of both LDOs, adjust the analog LDO before adjusting the memory LDO.
5. Output range represents the programmable output range, and does not reflect the minimum voltage under all conditions. Dropout when the input supply is close to the output setting is normal, and accounted for.
6. Analog peripheral specifications assume a 1.8 V output on the analog LDO.

Table 3.9. SAR ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}	12 Bit Mode		12		Bits
		10 Bit Mode		10		Bits
Supply Voltage Requirements (VBAT)	V_{ADC}	High Speed Mode	2.2	—	3.8	V
		Low Power Mode	1.8	—	3.8	V
Throughput Rate (High Speed Mode)	f_S	12 Bit Mode	—	—	250	ksps
		10 Bit Mode	—	—	1	Msps
Throughput Rate (Low Power Mode)	f_S	12 Bit Mode	—	—	62.5	ksps
		10 Bit Mode	—	—	250	ksps
Tracking Time	t_{TRK}	High Speed Mode	230	—	—	ns
		Low Power Mode	450	—	—	ns
SAR Clock Frequency	f_{SAR}	High Speed Mode	—	—	16.24	MHz
		Low Power Mode	—	—	4	MHz
Conversion Time	t_{CNV}	10-Bit Conversion, SAR Clock = 16 MHz, APB Clock = 40 MHz		762.5		ns
Sample/Hold Capacitor	C_{SAR}	Gain = 1	—	5	—	pF
		Gain = 0.5	—	2.5	—	pF
Input Pin Capacitance	C_{IN}	High Quality Inputs	—	18	—	pF
		Normal Inputs	—	20	—	pF
Input Mux Impedance	R_{MUX}	High Quality Inputs	—	300	—	Ω
		Normal Inputs	—	550	—	Ω
Voltage Reference Range	V_{REF}		1	—	V_{BAT}	V
Input Voltage Range*	V_{IN}	Gain = 1	0	—	V_{REF}	V
		Gain = 0.5	0	—	$2xV_{REF}$	V
Power Supply Rejection Ratio	$PSRR_{ADC}$		—	70	—	dB
DC Performance						
Integral Nonlinearity	INL	12 Bit Mode	—	±1	±1.9	LSB
		10 Bit Mode	—	±0.2	±0.5	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL	12 Bit Mode	–1	±0.7	1.8	LSB
		10 Bit Mode	—	±0.2	±0.5	LSB
Offset Error (using VREFGND)	E_{OFF}	12 Bit Mode, VREF = 2.4 V	–2	0	2	LSB
		10 Bit Mode, VREF = 2.4 V	–1	0	1	LSB

peripherals and may individually shut down and gate the clocks of any or all peripherals for power savings.

The on-chip debugging interface (SWJ-DP) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging.

Each device is specified for 1.8 to 3.8 V operation over the industrial temperature range (–40 to +85 °C). The SiM3L1xx devices are available in 40-pin or 64-pin QFN and 64-pin or 80-pin TQFP packages. All package options are lead-free and RoHS compliant. See Table 5.1 for ordering information. A block diagram is included in Figure 4.1.

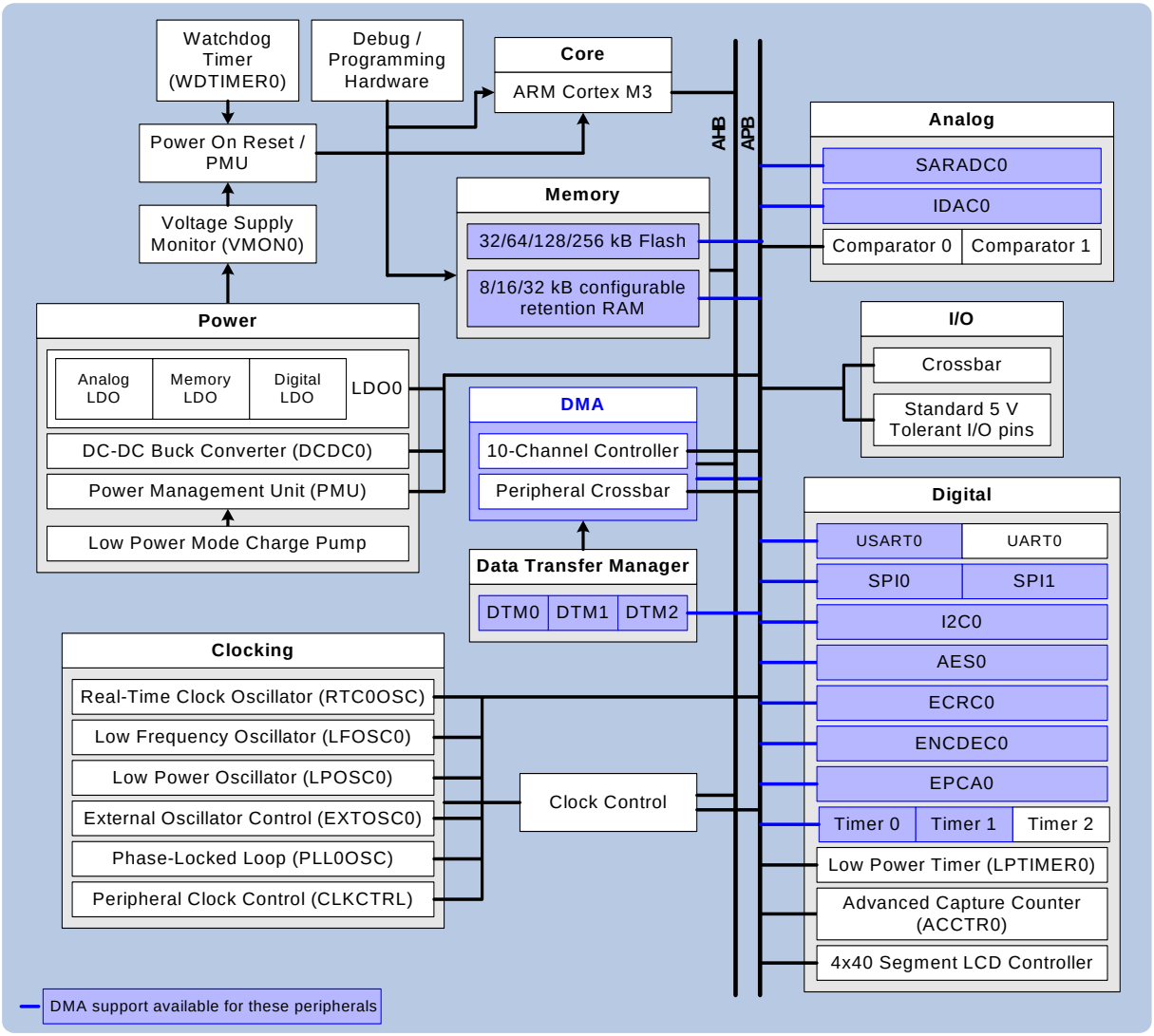

Figure 4.1. Precision32™ SiM3L1xx Family Block Diagram

- Supports synchronizing the regulator switching with the system clock.
- Automatically limits the peak inductor current if the load current rises beyond a safe limit.
- Automatically goes into bypass mode if the battery voltage cannot provide sufficient headroom.
- Sources current, but cannot sink current.

4.1.2. Three Low Dropout LDO Regulators (LDO0)

The SiM3L1xx devices include one LDO0 module with three low dropout regulators. Each of these regulators have independent switches to select the battery voltage or the output of the dc-dc converter as the input to each LDO, and an adjustable output voltage.

The LDOs consume little power and provide flexibility in choosing a power supply for the system. Each regulator can be independently adjusted between 0.8 and 1.9 V output.

4.1.3. Voltage Supply Monitor (VMON0)

The SiM3L1xx devices include a voltage supply monitor that can monitor the main supply voltage. This module includes the following features:

- Main supply “VBAT Low” (VBAT below the early warning threshold) notification.
- Holds the device in reset if the main VBAT supply drops below the VBAT Reset threshold.

The voltage supply monitor allows devices to function in known, safe operating conditions without the need for external hardware.

4.1.4. Power Management Unit (PMU)

The Power Management Unit on the SiM3L1xx manages the power systems of the device. It manages the power-up sequence during power on and the wake up sources for PM8. On power-up, the PMU ensures the core voltages are a proper value before core instruction execution begins.

The VDRV pin powers external circuitry from either the VBAT battery input voltage or the output of the dc-dc converter on VDC. The PMU includes an internal switch to select one of these sources for the VDRV pin.

The PMU has a specialized VBAT-divided-by-2 charge pump that can power some internal modules while in PM8 to save power.

The PMU module includes the following features:

- Provides the enable or disable for the analog power system, including the three LDO regulators.
- Up to 14 pin wake inputs can wake the device from Power Mode 8.
- The Low Power Timer, RTC0 (alarms and oscillator failure), Comparator 0, Advanced Capture Counter, LCD0 VBAT monitor, UART0, low power mode charge pump failure, and the RESET pin can also serve as wake sources for Power Mode 8.
- Controls which 4 kB RAM blocks are retained while in Power Mode 8.
- Provides a PMU_Asleep signal to a pin as an indicator that the device is in PM8.
- Specialized charge pump to reduce power consumption in PM8.

Provides control for the internal switch between VBAT and VDC to power the VDRV pin for external circuitry.

4.1.5. Device Power Modes

The SiM3L1xx devices feature seven low power modes in addition to normal operating mode. Several peripherals provide wake up sources for these low power modes, including the Low Power Timer (LPTIMER0), RTC0 (alarms and oscillator failure notification), Comparator 0 (CMP0), Advanced Capture Counter (ACCTR0), LCD VBAT monitor (LCD0), UART0, low power mode charge pump failure, and PMU Pin Wake.

In addition, all peripherals can have their clocks disabled to reduce power consumption whenever a peripheral is not being used using the clock control (CLKCTRL) registers.

4.1.5.1. Normal Mode (Power Mode 0) and Power Mode 4

Normal Mode and Power Mode 4 are fully operational modes with code executing from flash memory. PM4 is the same as Normal Mode, but with the clocks operating at a lower speed. This enables power to be conserved by reducing the LDO regulator outputs.

4.2. I/O

4.2.1. General Features

The SiM3L1xx ports have the following features:

- 5 V tolerant.
- Push-pull or open-drain output modes to the VIO or VIORF voltage level.
- Analog or digital modes.
- Option for high or low output drive strength.
- Port Match allows the device to recognize a change on a port pin value.
- Internal pull-up resistors are enabled or disabled on a port-by-port basis.
- Two external interrupts with up to 16 inputs each provide monitoring capability for external signals.
- Internal Pulse Generator Timer (PB0 only) to generate simple square waves and pulses.

4.2.2. Crossbar

The SiM3L1xx devices have one crossbar with the following features:

- Flexible peripheral assignment to port pins.
- Pins can be individually skipped to move peripherals as needed for design or layout considerations.

The crossbar has a fixed priority for each I/O function and assigns these functions to the port pins. When a digital resource is selected, the least-significant unassigned port pin is assigned to that resource. If a port pin is assigned, the crossbar skips that pin when assigning the next selected resource. Additionally, the crossbar will skip port pins whose associated bits in the PBSKIPEN registers are set. This provides flexibility when designing a system: pins involved with sensitive analog measurements can be moved away from digital I/O, and peripherals can be moved around the chip as needed to ease layout constraints.

- Multiple loop-back modes supported.
- Multi-processor communications support.
- Operates at 9600, 4800, 2400, or 1200 baud in Power Mode 8.

4.7.3. SPI (SPI0, SPI1)

SPI is a 3- or 4-wire communication interface that includes a clock, input data, output data, and an optional select signal.

The SPI0 and SPI1 modules include the following features:

- Supports 3- or 4-wire master or slave modes.
- Supports up to 10 MHz clock in master mode and 5 MHz clock in slave mode.
- Support for all clock phase and slave select (NSS) polarity modes.
- 16-bit programmable clock rate.
- Programmable MSB-first or LSB-first shifting.
- 8-byte FIFO buffers for both transmit and receive data paths to support high speed transfers.
- Support for multiple masters on the same data lines.

In addition, the SPI modules include several features to support autonomous DMA transfers:

- Hardware NSS control.
- Programmable FIFO threshold levels.
- Configurable FIFO data widths.
- Master or slave hardware flow control for the MISO and MOSI signals.

SPI1 is on fixed pins and supports additional flow control options using a fixed input (SPI1CTS). Neither SPI1 nor the flow control input are on the crossbar.

4.7.4. I2C (I2C0)

The I2C interface is a two-wire, bi-directional serial bus. The clock and data signals operate in open-drain mode with external pull-ups to support automatic bus arbitration.

Reads and writes to the interface are byte oriented with the I2C interface autonomously controlling the serial transfer of the data. Data can be transferred at up to 1/8th of the APB clock as a master or slave, which can be faster than allowed by the I2C specification, depending on the clock source used. A method of extending the clock-low duration is available to accommodate devices with different speed capabilities on the same bus.

The I2C interface may operate as a master and/or slave, and may function on a bus with multiple masters. The I2C provides control of SDA (serial data), SCL (serial clock) generation and synchronization, arbitration logic, and start/stop control and generation.

The I2C0 module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds.
- Can operate down to APB clock divided by 32768 or up to APB clock divided by 8.
- Support for master, slave, and multi-master modes.
- Hardware synchronization and arbitration for multi-master mode.
- Clock low extending (clock stretching) to interface with faster masters.
- Hardware support for 7-bit slave and general call address recognition.
- Firmware support for 10-bit slave address decoding.
- Ability to disable all slave states.
- Programmable clock high and low period.
- Programmable data setup/hold times.
- Spike suppression up to 2 times the APB period.

5. Ordering Information

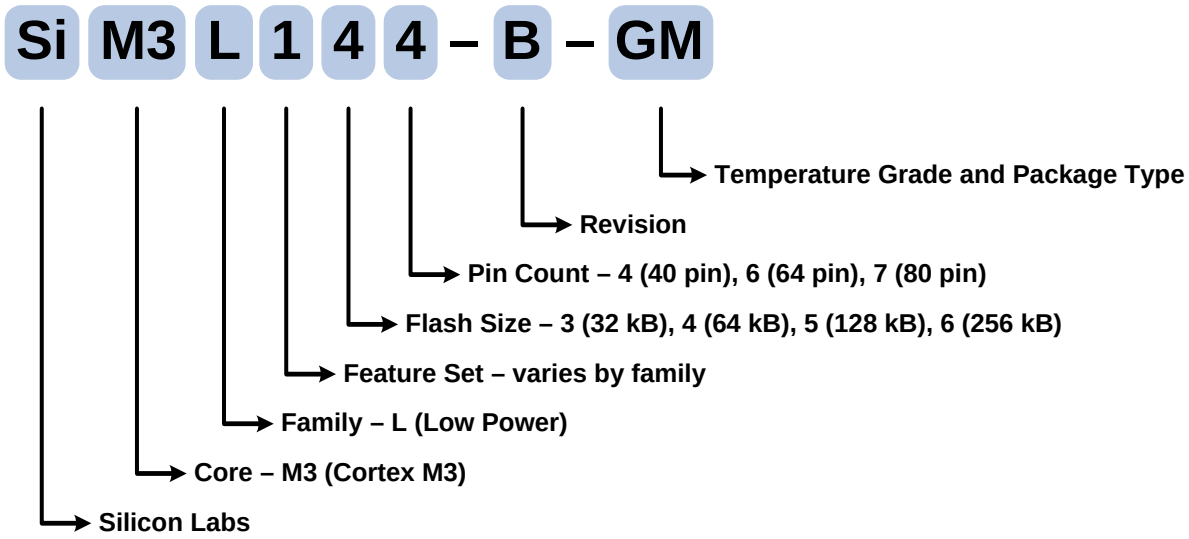

Figure 5.1. SiM3L1xx Part Numbering

All devices in the SiM3L1xx family have the following features:

- **Core:** ARM Cortex-M3 with maximum operating frequency of 50 MHz.
- **PLL.**
- **10-Channel DMA Controller.**
- **128/192/256-bit AES.**
- **16/32-bit CRC.**
- **Encoder/Decoder.**
- **DC-DC Buck Converter.**
- **Timers:** 3 x 32-bit (6 x 16-bit).
- **Real-Time Clock.**
- **Low-Power Timer.**
- **PCA:** 1 x 6 channels (Enhanced)
- **ADC:** 12-bit 250 ksps (10-bit 1 Msps) SAR.
- **DAC:** 10-bit IDAC.
- **Temperature Sensor.**
- **Internal VREF.**
- **Comparator:** 2 x low current.
- **Serial Buses:** 2 x USART, 2 x SPI, 1 x I2C

Additionally, all devices in the SiM3L1xx family include the low power mode advanced capture counter (ACCTR0), though the smaller packages (SiM3L1x4) only support some of the external inputs and outputs.

Table 6.1. Pin Definitions and Alternate Functions for SiM3L1x7 (Continued)

Pin Name	Type	Pin Numbers (TQFP-80)	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB3.4	Standard I/O	43	VIO	✓	✓	LCD0.23		INT1.12	CMP0P.6
PB3.5	Standard I/O	42	VIO	✓	✓	LCD0.22		INT1.13	CMP0N.6
PB3.6	Standard I/O	41	VIO	✓	✓	LCD0.21		INT1.14	CMP1P.6
PB3.7	Standard I/O	40	VIO	✓	✓	LCD0.20		INT1.15	CMP1N.6
PB3.8	Standard I/O	39	VIO		✓	LCD0.19			CMP0P.7
PB3.9	Standard I/O	38	VIO		✓	LCD0.18			CMP0N.7
PB3.10	Standard I/O	37	VIO		✓	LCD0.17			CMP1P.7
PB3.11	Standard I/O	36	VIO		✓	LCD0.16			CMP1N.7
PB3.12	Standard I/O	35	VIO		✓	LCD0.15			ADC0.18
PB3.13	Standard I/O	34	VIO		✓	LCD0.14			ADC0.19
PB3.14	Standard I/O	33	VIO		✓	COM0.3			
PB3.15	Standard I/O	32	VIO		✓	COM0.2			
PB4.0	Standard I/O	29	VIO		✓	COM0.1			
PB4.1	Standard I/O	28	VIO		✓	COM0.0			
PB4.2	Standard I/O	27	VIO		✓	LCD0.13			
PB4.3	Standard I/O	26	VIO		✓	LCD0.12			
PB4.4	Standard I/O	25	VIO		✓	LCD0.11			
PB4.5	Standard I/O	24	VIO		✓	LCD0.10			
PB4.6	Standard I/O	23	VIO		✓	LCD0.9		PMU_Asleep	
PB4.7	Standard I/O	22	VIO		✓	LCD0.8			
PB4.8	Standard I/O	21	VIO		✓	LCD0.7			

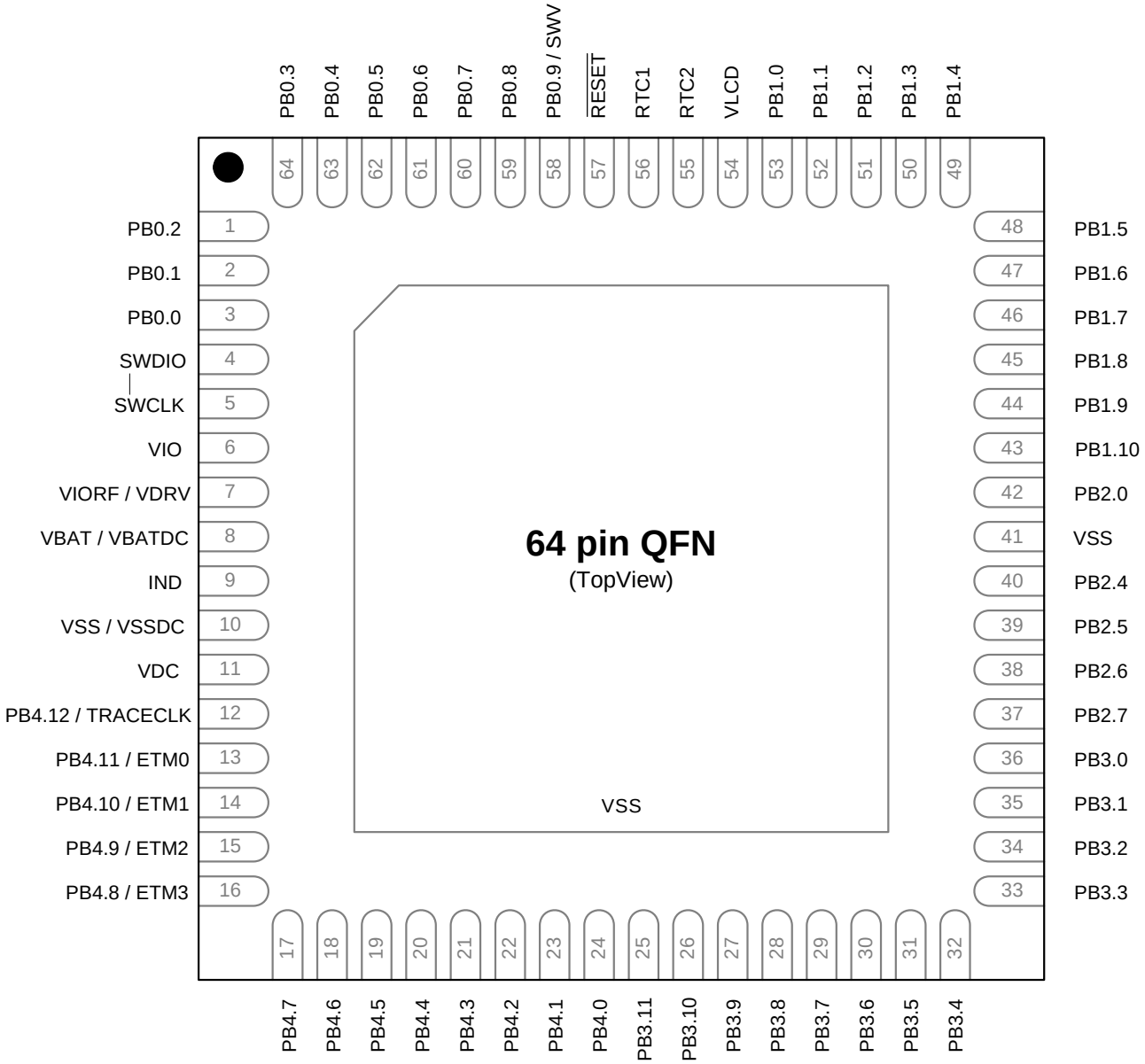

Figure 6.3. SiM3L1x6-GM Pinout

Table 6.2. Pin Definitions and Alternate Functions for SiM3L1x6

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
VSS	Ground	10 41							
VSSDC	Ground (DC-DC)	10							
VIO	Power (I/O)	6							
VIORF / VDRV	Power (RF I/O)	7							
VBAT / VBATDC		8							
VDC		11							
VLCD	Power (LCD Charge Pump)	54							
IND	DC-DC Inductor	9							
$\overline{\text{RESET}}$	Active-low Reset	57							
SWCLK	Serial Wire	5							
SWDIO	Serial Wire	4							
RTC1	RTC Oscillator Input	56							
RTC2	RTC Oscillator Output	55							
PB0.0	Standard I/O	3	VIO	XBR 0	✓		✓	INT0.0 WAKE.0	ADC0.20 VREF CMP0P.0
PB0.1	Standard I/O	2	VIO	XBR 0	✓		✓	INT0.1 WAKE.2	ADC0.22 CMP0N.0 CMP1P.0 XTAL2

Table 6.2. Pin Definitions and Alternate Functions for SiM3L1x6 (Continued)

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB1.1	Standard I/O	52	VIO	XBR0	✓	LCD0.30		LPT0T5 INT0.13 ACCTR0_LCBIAS1	CMP0N.2
PB1.2	Standard I/O	51	VIO	XBR0	✓	LCD0.29		LPT0T6 INT0.14 UART0_TX	CMP1P.2
PB1.3	Standard I/O	50	VIO	XBR0	✓	LCD0.28		LPT0T7 INT0.15 UART0_RX	CMP1N.2
PB1.4	Standard I/O	49	VIO	XBR0	✓	LCD0.27		ACCTR0_DBG0	ADC0.3
PB1.5	Standard I/O	48	VIO	XBR0	✓	LCD0.26		ACCTR0_DBG1	ADC0.4
PB1.6	Standard I/O	47	VIO	XBR0	✓	LCD0.25		RTC0TCLK_OUT	ADC0.5
PB1.7	Standard I/O	46	VIO	XBR0	✓	LCD0.24			CMP0P.3
PB1.8	Standard I/O	45	VIO	XBR0	✓	LCD0.23			CMP0N.3
PB1.9	Standard I/O	44	VIO	XBR0	✓	LCD0.22			CMP1P.3
PB1.10	Standard I/O	43	VIO	XBR0	✓	LCD0.21			CMP1N.3
PB2.0	Standard I/O	42	VIORF	XBR0	✓			LPT0T8 INT1.0 WAKE.12 SPI1_CTS	ADC0.6 CMP0P.4
PB2.4	Standard I/O	40	VIORF	XBR0	✓			LPT0T12 INT1.4 SPI1_SCLK	ADC0.7 CMP0P.5

Table 6.2. Pin Definitions and Alternate Functions for SiM3L1x6 (Continued)

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB2.5	Standard I/O	39	VIORF	XBR0	✓			LPT0T13 INT1.5 SPI1_MISO	ADC0.8 CMP0N.5
PB2.6	Standard I/O	38	VIORF	XBR0	✓			LPT0T14 INT1.6 SPI1_MOSI	ADC0.9 CMP1P.5
PB2.7	Standard I/O	37	VIORF	XBR0	✓			INT1.7 SPI1_NSS	ADC0.10 CMP1N.5
PB3.0	Standard I/O	36	VIO	XBR0	✓	LCD0.20		INT1.8	ADC0.11
PB3.1	Standard I/O	35	VIO	XBR0	✓	LCD0.19		INT1.9	ADC0.12
PB3.2	Standard I/O	34	VIO	XBR0	✓	LCD0.18		INT1.10	CMP0P.6
PB3.3	Standard I/O	33	VIO	XBR0	✓	LCD0.17		INT1.11	CMP0N.6
PB3.4	Standard I/O	32	VIO	XBR0	✓	LCD0.16		INT1.12	CMP0P.7
PB3.5	Standard I/O	31	VIO	XBR0	✓	LCD0.15		INT1.13	CMP0N.7
PB3.6	Standard I/O	30	VIO	XBR0	✓	LCD0.14		INT1.14	CMP1P.7
PB3.7	Standard I/O	29	VIO	XBR0	✓	LCD0.13		INT1.15	CMP1N.7
PB3.8	Standard I/O	28	VIO		✓	LCD0.12			ADC0.13
PB3.9	Standard I/O	27	VIO		✓	LCD0.11			ADC0.14
PB3.10	Standard I/O	26	VIO		✓	COM0.3			
PB3.11	Standard I/O	25	VIO		✓	COM0.2			

6.6.1. TQFP-64 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.6.2. TQFP-64 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.

6.6.3. TQFP-64 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.7. QFN-40 Package Specifications

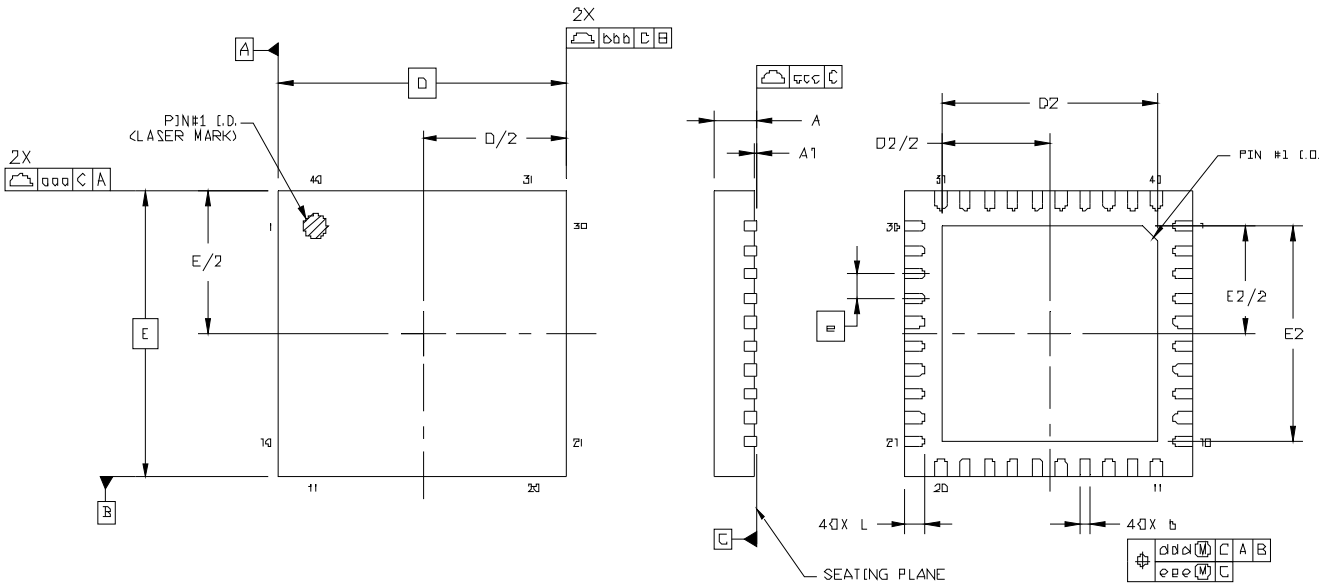

Figure 6.11. QFN-40 Package Drawing

Table 6.10. QFN-40 Package Dimensions

Dimension	Min	Nominal	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		6.00 BSC	
D2	4.35	4.50	4.65
e		0.50 BSC	
E		6.00 BSC	
E2	4.35	4.5	4.65
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.