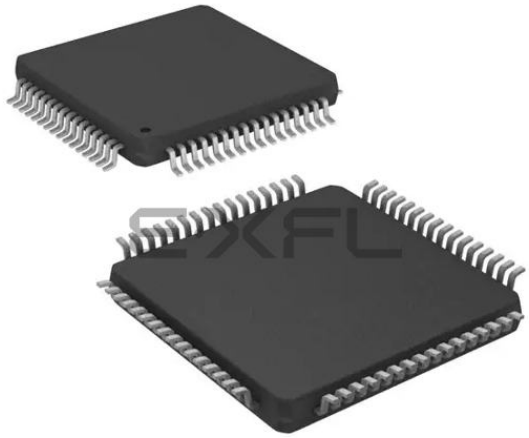

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Product Status	Not For New Designs
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Core Size	32-Bit Single-Core
Speed	50MHz
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Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 23x10/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/sim3l156-c-gqr

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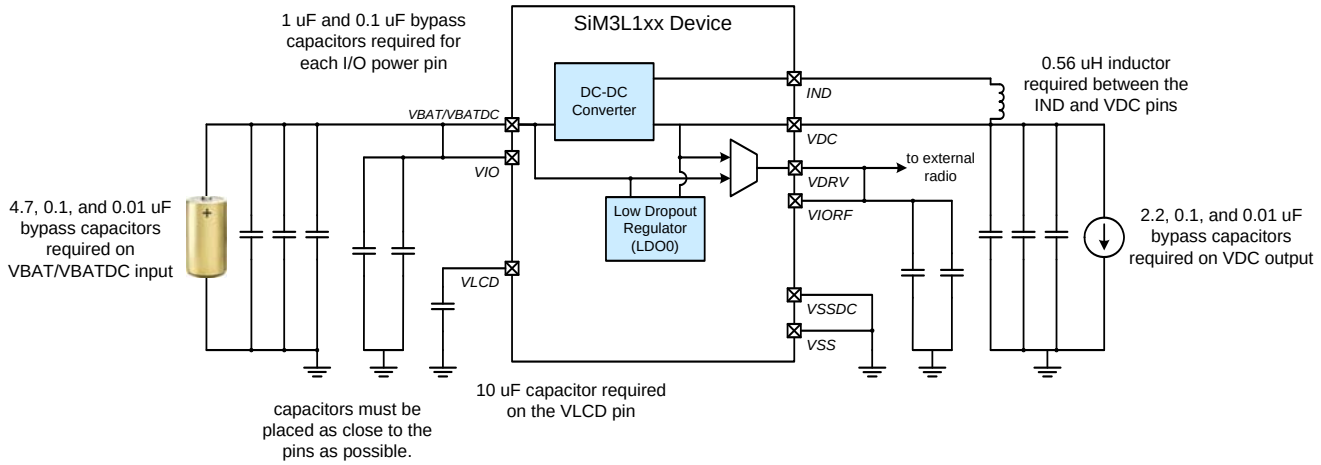

Figure 2.3. Connection Diagram with External Radio Device

Figure 2.4 shows a typical connection diagram for the power pins of the SiM3L1xx devices when the dc-dc buck converter is used and the I/O are powered separately.

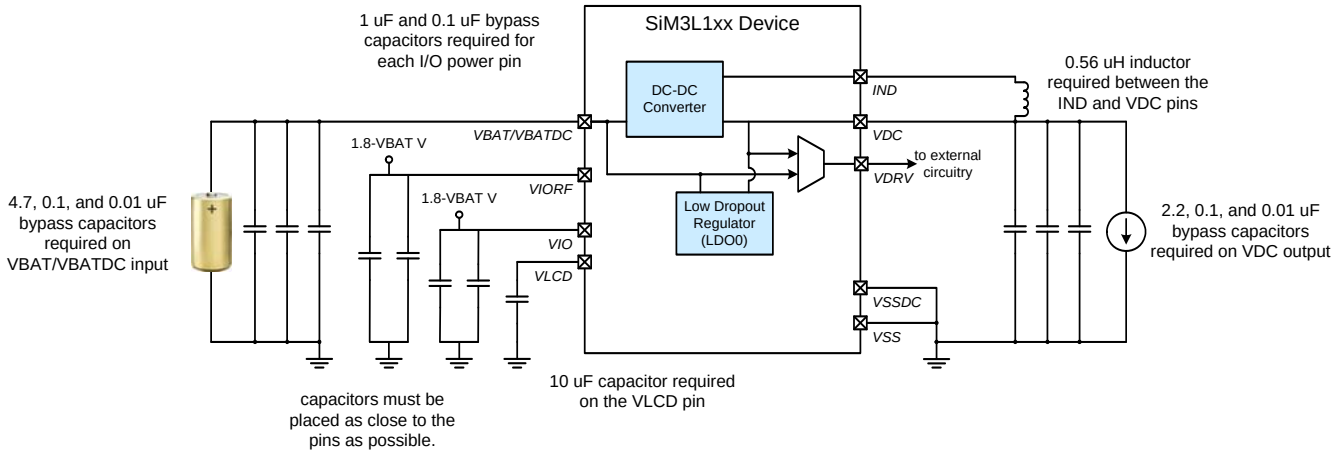

Figure 2.4. Connection Diagram with DC-DC Converter Used and I/O Powered Separately

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 2[1,2,3,4,5]—Core halted with only Port I/O clocks on (wake from pin).	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	4	7.2	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	1.47	—	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	430	—	µA
Power Mode 3[1,2,6]—Fast-Wake Mode (PM3CLKEN = 1)	I_{BAT}	V_{BAT} = 3.8 V	—	320	530	µA
		V_{BAT} = 1.8 V	—	225	—	µA
Power Mode 4[1,2,4,6]—Slower clock speed with code executing from flash, peripheral clocks ON	I_{BAT}	F_{AHB} = F_{APB} = 16 kHz, V_{BAT} = 3.8 V	—	385	640	µA
		F_{AHB} = F_{APB} = 16 kHz, V_{BAT} = 1.8 V	—	330	—	µA
Power Mode 5[1,2,4,6]—Slower clock speed with code executing from RAM, peripheral clocks ON	I_{BAT}	F_{AHB} = F_{APB} = 16 kHz, V_{BAT} = 3.8 V	—	320	490	µA
		F_{AHB} = F_{APB} = 16 kHz, V_{BAT} = 1.8 V	—	275	—	µA
Power Mode 6[1,2,4,6]—Core halted with peripheral clocks ON	I_{BAT}	F_{AHB} = F_{APB} = 16 kHz, V_{BAT} = 3.8 V	—	315	490	µA
		F_{AHB} = F_{APB} = 16 kHz, V_{BAT} = 1.8 V	—	270	—	µA
Power Mode 8[1,2]—Low Power Sleep, powered through VBAT, VIO, and VIORF at 2.4 V, 32kB of retention RAM	I_{BAT}	RTC Disabled, T_A = 25 °C	—	75	400	nA
		RTC w/ 16.4 kHz LFO, T_A = 25 °C	—	360	—	nA
		RTC w/ 32.768 kHz Crystal, T_A = 25 °C	—	670	—	nA

Notes:

1. Currents are additive. For example, where I_{BAT} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded I_{VIO} is included in all I_{BAT} PM8 production test measurements.

Table 3.3. Power Mode Wake Up Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 2 or 6 Wake Time	t_{PM2}		4	—	5	clocks
Power Mode 3 Fast Wake Time (using LFO as clock source)	t_{PM3FW}		—	425	—	µs
Power Mode 8 Wake Time	t_{PM8}		—	3.8	—	µs

Notes:
1. Wake times are specified as the time from the wake source to the execution phase of the first instruction following WFI. This includes latency to recognize the wake event and fetch the first instruction (assuming wait states = 0).

Table 3.4. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{BAT} High Supply Monitor Threshold (VBATHITHEN = 1)	V_{VBATMH}	Early Warning	—	2.20	—	V
		Reset	1.95	2.05	2.1	V
V_{BAT} Low Supply Monitor Threshold (VBATHITHEN = 0)	V_{VBATML}	Early Warning	—	1.85	—	V
		Reset	1.70	1.75	1.77	V
Power-On Reset (POR) Threshold	V_{POR}	Rising Voltage on V_{BAT}	—	1.4	—	V
		Falling Voltage on V_{BAT}	0.8	1	1.3	V
V_{BAT} Ramp Time	t_{RMP}	Time to $V_{BAT} \geq 1.8$ V	10	—	3000	µs
Reset Delay from POR	t_{POR}	Relative to $V_{BAT} \geq V_{POR}$	3	—	100	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	10	—	µs
$\overline{\text{RESET}}$ Low Time to Generate Reset	t_{RSTL}		50	—	—	ns
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	$F_{AHB} > 1$ MHz	—	0.5	1.5	ms
Missing Clock Detector Trigger Frequency	F_{MCD}		—	2.5	10	kHz
V_{BAT} Supply Monitor Turn-On Time	t_{MON}		—	2	—	µs

Table 3.5. On-Chip Regulators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC-DC Buck Converter						
Input Voltage Range	V_{DCIN}		1.8	—	3.8	V
Input Supply to Output Voltage Differential (for regulation)	V_{DCREG}		0.45	—	—	V
Output Voltage Range	V_{DCOUT}		1.25	—	3.8	V
Output Voltage Accuracy	V_{DCACC}		—	±25	—	mV
Output Current	I_{DCOUT}		—	—	90	mA
Inductor Value[1]	L_{DC}		0.47	0.56	0.68	µH
Inductor Current Rating	I_{LDC}	I_{load} < 50 mA	450	—	—	mA
		I_{load} > 50 mA	550	—	—	mA
Output Capacitor Value	C_{DCOUT}		1	2.2	10	µF
Input Capacitor Value[2]	C_{DCIN}		—	4.7	—	µF
Load Regulation	R_{load}		—	0.03	—	mV/mA
Maximum DC Load Current During Startup	I_{DCMAX}		—	—	5	mA
Switching Clock Frequency	F_{DCCLK}		1.9	2.9	3.8	MHz
Local Oscillator Frequency	F_{DCOSC}		2.4	2.9	3.4	MHz
LDO Regulators						
Input Voltage Range[3]	V_{LDOIN}	Sourced from VBAT	1.8	—	3.8	V
		Sourced from VDC	1.9	—	3.8	V
Output Voltage Range[4]	V_{LDO}		0.8	—	1.9	V
LDO Output Voltage Accuracy	V_{LDOACC}		—	±25	—	mV
Output Settings in PM8 (All LDOs)	V_{LDO}	1.8 V ≤ V_{BAT} ≤ 2.9 V	1.5			V
		1.95 V ≤ V_{BAT} ≤ 3.5 V	1.8			V
		2.0 V ≤ V_{BAT} ≤ 3.8 V	1.9			V

Notes:

1. See reference manual for recommended inductors.
2. Recommended: X7R or X5R ceramic capacitors with low ESR. Example: Murata GRM21BR71C225K with ESR < 10 mΩ (@ frequency > 1 MHz).
3. Input voltage specification accounts for the internal LDO dropout voltage under the maximum load condition to ensure that the LDO output voltage will remain at a valid level as long as V_{LDOIN} is at or above the specified minimum.
4. The memory LDO output should always be set equal to or lower than the output of the analog LDO. When lowering both LDOs (for example to go into PM8 under low supply conditions), first adjust the memory LDO and then the analog LDO. When raising the output of both LDOs, adjust the analog LDO before adjusting the memory LDO.
5. Output range represents the programmable output range, and does not reflect the minimum voltage under all conditions. Dropout when the input supply is close to the output setting is normal, and accounted for.
6. Analog peripheral specifications assume a 1.8 V output on the analog LDO.

Table 3.7. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Phase-Locked Loop (PLL0OSC)						
Calibrated Output Frequency (Free-running output mode, RANGE = 2)	$f_{PLL0OSC}$	Full Temperature and Supply Range	48.3	49	49.7	MHz
Power Supply Sensitivity (Free-running output mode, RANGE = 2)	$PSS_{PLL0OSC}$	T_A = 25 °C, Fout = 49 MHz	—	300	—	ppm/V
Temperature Sensitivity (Free-running output mode, RANGE = 2)	$TS_{PLL0OSC}$	V_{BAT} = 3.3 V, Fout = 49 MHz	—	50	—	ppm/°C
Adjustable Output Frequency Range	$f_{PLL0OSC}$		23	—	50	MHz
Lock Time	$t_{PLL0LOCK}$	f_{REF} = 20 MHz, $f_{PLL0OSC}$ = 50 MHz M=39, N=99, LOCKTH = 0	—	2.75	—	µs
		f_{REF} = 2.5 MHz, $f_{PLL0OSC}$ = 50 MHz M=19, N=399, LOCKTH = 0	—	9.45	—	µs
		f_{REF} = 32.768 kHz, $f_{PLL0OSC}$ = 50 MHz M=0, N=1524, LOCKTH = 0	—	92	—	µs
Low Power Oscillator (LPOSC0)						
Oscillator Frequency	f_{LPOSC}	Full Temperature and Supply Range	19	20	21	MHz
Divided Oscillator Frequency	f_{LPOSCD}	Full Temperature and Supply Range	2.375	2.5	2.625	MHz
Power Supply Sensitivity	PSS_{LPOSC}	T_A = 25 °C	—	0.5	—	%/V
Temperature Sensitivity	TS_{LPOSC}	V_{BAT} = 3.3 V	—	55	—	ppm/°C
Low Frequency Oscillator (LFOSC0)						
Oscillator Frequency	f_{LFOSC}	Full Temperature and Supply Range	13.4	16.4	19.7	kHz
		T_A = 25 °C, V_{BAT} = 3.3 V	15.8	16.4	17.3	kHz
Power Supply Sensitivity	PSS_{LFOSC}	T_A = 25 °C	—	2.4	—	%/V
Temperature Sensitivity	TS_{LFOSC}	V_{BAT} = 3.3 V	—	0.2	—	%/°C

Table 3.7. Internal Oscillators (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RTC0 Oscillator (RTC0OSC)						
Missing Clock Detector Trigger Frequency	f_{RTCMCD}		—	8	15	kHz
RTC External Input CMOS Clock Frequency	$f_{RTCEXTCLK}$		0	—	40	kHz
RTC Robust Duty Cycle Range	DC_{RTC}		25	—	55	%

Table 3.8. External Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency	f_{CMOS}		0*	—	50	MHz
External Crystal Frequency	f_{XTAL}		0.01	—	25	MHz
External Input CMOS Clock High Time	t_{CMOSH}		9	—	—	ns
External Input CMOS Clock Low Time	t_{CMOSL}		9	—	—	ns
Low Power Mode Charge Pump Supply Range (input from V_{BAT})	V_{BAT}		2.4	—	3.8	V
***Note:** Minimum of 10 kHz when debugging.						

Table 3.9. SAR ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}	12 Bit Mode		12		Bits
		10 Bit Mode		10		Bits
Supply Voltage Requirements (VBAT)	V_{ADC}	High Speed Mode	2.2	—	3.8	V
		Low Power Mode	1.8	—	3.8	V
Throughput Rate (High Speed Mode)	f_S	12 Bit Mode	—	—	250	ksps
		10 Bit Mode	—	—	1	Msps
Throughput Rate (Low Power Mode)	f_S	12 Bit Mode	—	—	62.5	ksps
		10 Bit Mode	—	—	250	ksps
Tracking Time	t_{TRK}	High Speed Mode	230	—	—	ns
		Low Power Mode	450	—	—	ns
SAR Clock Frequency	f_{SAR}	High Speed Mode	—	—	16.24	MHz
		Low Power Mode	—	—	4	MHz
Conversion Time	t_{CNV}	10-Bit Conversion, SAR Clock = 16 MHz, APB Clock = 40 MHz		762.5		ns
Sample/Hold Capacitor	C_{SAR}	Gain = 1	—	5	—	pF
		Gain = 0.5	—	2.5	—	pF
Input Pin Capacitance	C_{IN}	High Quality Inputs	—	18	—	pF
		Normal Inputs	—	20	—	pF
Input Mux Impedance	R_{MUX}	High Quality Inputs	—	300	—	Ω
		Normal Inputs	—	550	—	Ω
Voltage Reference Range	V_{REF}		1	—	V_{BAT}	V
Input Voltage Range*	V_{IN}	Gain = 1	0	—	V_{REF}	V
		Gain = 0.5	0	—	$2xV_{REF}$	V
Power Supply Rejection Ratio	$PSRR_{ADC}$		—	70	—	dB
DC Performance						
Integral Nonlinearity	INL	12 Bit Mode	—	±1	±1.9	LSB
		10 Bit Mode	—	±0.2	±0.5	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL	12 Bit Mode	–1	±0.7	1.8	LSB
		10 Bit Mode	—	±0.2	±0.5	LSB
Offset Error (using VREFGND)	E_{OFF}	12 Bit Mode, VREF = 2.4 V	–2	0	2	LSB
		10 Bit Mode, VREF = 2.4 V	–1	0	1	LSB

Table 3.14. Comparator (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CMPHYP = 00	—	1.37	—	mV
		CMPHYP = 01	—	3.8	—	mV
		CMPHYP = 10	—	7.8	—	mV
		CMPHYP = 11	—	15.6	—	mV
Negative Hysteresis Mode 3 (CPMD = 11)	HYS_{CP-}	CMPHYN = 00	—	1.37	—	mV
		CMPHYN = 01	—	–3.9	—	mV
		CMPHYN = 10	—	–7.9	—	mV
		CMPHYN = 11	—	–16	—	mV
Input Range (CP+ or CP–)	V_{IN}		–0.25	—	V_{BAT} + 0.25	V
Input Pin Capacitance	C_{CP}		—	7.5	—	pF
Common-Mode Rejection Ratio	$CMRR_{CP}$		—	75	—	dB
Power Supply Rejection Ratio	$PSRR_{CP}$		—	72	—	dB
Input Offset Voltage	V_{OFF}	T_A = 25 °C	–10	0	10	mV
Input Offset Tempco	TC_{OFF}		—	3.5	—	µV/°C
Reference DAC Resolution	N_{Bits}			6		bits

Table 3.15. LCD0

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Charge Pump Output Voltage Error	V_{CPERR}		—	±50	—	mV
LCD Clock Frequency	F_{LCD}		16	—	33	kHz

- Supports synchronizing the regulator switching with the system clock.
- Automatically limits the peak inductor current if the load current rises beyond a safe limit.
- Automatically goes into bypass mode if the battery voltage cannot provide sufficient headroom.
- Sources current, but cannot sink current.

4.1.2. Three Low Dropout LDO Regulators (LDO0)

The SiM3L1xx devices include one LDO0 module with three low dropout regulators. Each of these regulators have independent switches to select the battery voltage or the output of the dc-dc converter as the input to each LDO, and an adjustable output voltage.

The LDOs consume little power and provide flexibility in choosing a power supply for the system. Each regulator can be independently adjusted between 0.8 and 1.9 V output.

4.1.3. Voltage Supply Monitor (VMON0)

The SiM3L1xx devices include a voltage supply monitor that can monitor the main supply voltage. This module includes the following features:

- Main supply “VBAT Low” (VBAT below the early warning threshold) notification.
- Holds the device in reset if the main VBAT supply drops below the VBAT Reset threshold.

The voltage supply monitor allows devices to function in known, safe operating conditions without the need for external hardware.

4.1.4. Power Management Unit (PMU)

The Power Management Unit on the SiM3L1xx manages the power systems of the device. It manages the power-up sequence during power on and the wake up sources for PM8. On power-up, the PMU ensures the core voltages are a proper value before core instruction execution begins.

The VDRV pin powers external circuitry from either the VBAT battery input voltage or the output of the dc-dc converter on VDC. The PMU includes an internal switch to select one of these sources for the VDRV pin.

The PMU has a specialized VBAT-divided-by-2 charge pump that can power some internal modules while in PM8 to save power.

The PMU module includes the following features:

- Provides the enable or disable for the analog power system, including the three LDO regulators.
- Up to 14 pin wake inputs can wake the device from Power Mode 8.
- The Low Power Timer, RTC0 (alarms and oscillator failure), Comparator 0, Advanced Capture Counter, LCD0 VBAT monitor, UART0, low power mode charge pump failure, and the RESET pin can also serve as wake sources for Power Mode 8.
- Controls which 4 kB RAM blocks are retained while in Power Mode 8.
- Provides a PMU_Asleep signal to a pin as an indicator that the device is in PM8.
- Specialized charge pump to reduce power consumption in PM8.

Provides control for the internal switch between VBAT and VDC to power the VDRV pin for external circuitry.

4.1.5. Device Power Modes

The SiM3L1xx devices feature seven low power modes in addition to normal operating mode. Several peripherals provide wake up sources for these low power modes, including the Low Power Timer (LPTIMER0), RTC0 (alarms and oscillator failure notification), Comparator 0 (CMP0), Advanced Capture Counter (ACCTR0), LCD VBAT monitor (LCD0), UART0, low power mode charge pump failure, and PMU Pin Wake.

In addition, all peripherals can have their clocks disabled to reduce power consumption whenever a peripheral is not being used using the clock control (CLKCTRL) registers.

4.1.5.1. Normal Mode (Power Mode 0) and Power Mode 4

Normal Mode and Power Mode 4 are fully operational modes with code executing from flash memory. PM4 is the same as Normal Mode, but with the clocks operating at a lower speed. This enables power to be conserved by reducing the LDO regulator outputs.

4.5.4. 16/32-bit Enhanced CRC (ECRC0)

The ECRC module is designed to provide hardware calculations for flash memory verification and communications protocols. In addition to calculating a result from direct writes from firmware, the ECRC module can automatically snoop the APB bus and calculate a result from data written to or read from a particular peripheral. This allows for an automatic CRC result without directly feeding data through the ECRC module.

The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3). The 16-bit polynomial is fully programmable.

The ECRC module includes the following features:

- Support for a programmable 16-bit polynomial and one fixed 32-bit polynomial.
- Byte-level bit reversal for the CRC input.
- Byte-order reorientation of words for the CRC input.
- Word or half-word bit reversal of the CRC result.
- Ability to configure and seed an operation in a single register write.
- Support for single-cycle parallel (unrolled) CRC computation for 32-, 16-, or 8-bit blocks.
- Capability to CRC 32 bits of data per peripheral bus (APB) clock.
- Automatic APB bus snooping.
- Support for DMA writes using firmware request mode.

4.5.5. Encoder / Decoder (ENCDEC0)

The encoder / decoder module supports Manchester and Three-out-of-Six encoding and decoding from either firmware or DMA operations.

This module has the following features:

- Supports Manchester and Three-out-of-Six encoding and decoding.
- Automatic flag clearing when writing the input or reading the output data registers.
- Writing to the input data register automatically initiates an encode or decode operation.
- Optional output in one’s complement format.
- Hardware error detection for invalid input data during decode operations, which helps reduce power consumption and packet turn-around time.
- Flexible byte swapping on the input or output data.

4.6.6. Low Power Mode Advanced Capture Counter (ACCTR0)

The SiM3L1xx devices contain a low-power Advanced Capture Counter module that runs from the RTC0 clock domain and can be used with digital inputs, switch topology circuits (reed switches), or with LC resonant circuits. For switch topology circuits, the module charges one or two external lines by pulsing internal pull-up resistors and detecting whether the reed switch is open or closed. For LC resonant circuits, the inputs are periodically energized to produce a dampened sine wave and configurable discriminator circuits detect the resulting decay time-constant.

The advanced capture counter has the following general features:

- Single or differential inputs supporting single, dual, and quadrature modes of operation.
- Variety of interrupt and PM8 wake up sources.
- Provides feedback of the direction history, current and previous states, and condition flags.

The advanced capture counter has the following features for switch circuit topologies:

- Ultra low power input comparators.
- Supports a wide range of pull-up resistor values with a self-calibration engine.
- Asymmetrical integrators for low-pass filtering and switch debounce.
- Two 24-bit counters and two 24-bit digital threshold comparators.
- Supports switch flutter detection.

For LC resonant circuit topologies, the advanced capture counter includes:

- Separate minimum and maximum count registers and polarity, pulse, and toggle controls.
- Zone-based programmable timing.
- Two input comparators with support for a positive side input bias at VIO divided by 2.
- Supports a configurable excitation pulse width based on a 40 MHz oscillator and timer or an external digital stop signal.
- Two 8-bit peak counters that saturate at full scale for detecting the number of LC resonant peaks.
- Two discriminators with programmable thresholds.
- Supports a sample and hold mode for Wheatstone bridges.

All devices in the SiM3L1xx family include the low power mode advanced capture counter (ACCTR0). Table 4.2 lists the supported inputs and outputs for each of the packages.

Table 4.2. SiM3L1xx Supported Advanced Capture Counter Inputs and Outputs

Input/Output	SiM3L1x7	SiM3L1x6	SiM3L1x4
ACCTR0_IN0	✓	✓	✓
ACCTR0_IN1	✓	✓	✓
ACCTR0_LCIN0	✓	✓	
ACCTR0_LCIN1	✓	✓	✓
ACCTR0_STOP0	✓	✓	✓
ACCTR0_STOP1	✓	✓	✓
ACCTR0_LCPUL0	✓	✓	
ACCTR0_LCPUL1	✓	✓	
ACCTR0_LCBIAS0	✓	✓	
ACCTR0_LCBIAS1	✓	✓	
ACCTR0_DBG0	✓	✓	
ACCTR0_DBG1	✓	✓	

4.9. Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.
- AHB peripheral clocks to flash and RAM are enabled.
- Clocks to all APB peripherals other than the Watchdog Timer and DMAXBAR are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost.

The Port I/O latches are reset to 1 in open-drain mode. Weak pullups are enabled during and after the reset. For VBAT Supply Monitor and power-on resets, the RESET pin is driven low until the device exits the reset state.

On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to the internal low-power oscillator. The Watchdog Timer is enabled with the low frequency oscillator as its clock source. Program execution begins at location 0x00000000.

All RSTSRC0 registers may be locked against writes by setting the CLKRSTL bit in the LOCK0_PERIPHLOCK0 register to 1.

The reset sources can also optionally reset individual modules, including the low power mode charge pump, UART0, LCD0, advanced capture counter (ACCTR0), and RTC0.

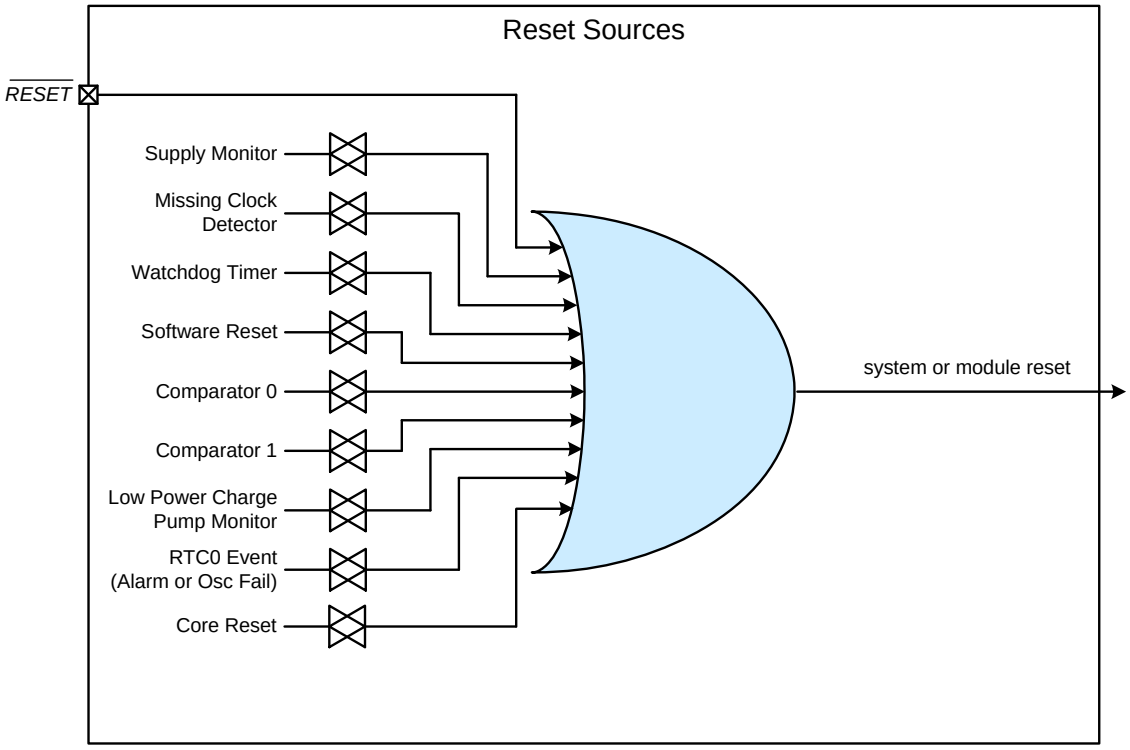

Figure 4.4. SiM3L1xx Reset Sources Block Diagram

Table 6.2. Pin Definitions and Alternate Functions for SiM3L1x6

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
VSS	Ground	10 41							
VSSDC	Ground (DC-DC)	10							
VIO	Power (I/O)	6							
VIORF / VDRV	Power (RF I/O)	7							
VBAT / VBATDC		8							
VDC		11							
VLCD	Power (LCD Charge Pump)	54							
IND	DC-DC Inductor	9							
$\overline{\text{RESET}}$	Active-low Reset	57							
SWCLK	Serial Wire	5							
SWDIO	Serial Wire	4							
RTC1	RTC Oscillator Input	56							
RTC2	RTC Oscillator Output	55							
PB0.0	Standard I/O	3	VIO	XBR 0	✓		✓	INT0.0 WAKE.0	ADC0.20 VREF CMP0P.0
PB0.1	Standard I/O	2	VIO	XBR 0	✓		✓	INT0.1 WAKE.2	ADC0.22 CMP0N.0 CMP1P.0 XTAL2

Table 6.2. Pin Definitions and Alternate Functions for SiM3L1x6 (Continued)

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB0.2	Standard I/O	1	VIO	XBR 0	✓		✓	INT0.2 WAKE.3	ADC0.23 CMP1N.0 XTAL1
PB0.3	Standard I/O	64	VIO	XBR 0	✓		✓	INT0.3 WAKE.4	ADC0.0 CMP0P.1 IDAC0
PB0.4	Standard I/O	63	VIO	XBR 0	✓		✓	INT0.4 WAKE.5 ACCTR0_STOP0	ACCTR0_IN0
PB0.5	Standard I/O	62	VIO	XBR 0	✓		✓	INT0.5 WAKE.6 ACCTR0_STOP1	ACCTR0_IN1
PB0.6	Standard I/O	61	VIO	XBR 0	✓		✓	INT0.6 WAKE.7	ACCTR0_LCIN0
PB0.7	Standard I/O	60	VIO	XBR 0	✓		✓	LPT0T0 LPT0OUT0 INT0.7 WAKE.8	ACCTR0_LCIN1
PB0.8	Standard I/O	59	VIO	XBR 0	✓		✓	LPT0T1 INT0.8 WAKE.9 ACCTR0_LCPUL0	ADC0.1 CMP0N.1
PB0.9/SWV	Standard I/O /Serial Wire Viewer	58	VIO	XBR 0	✓		✓	LPT0T2 INT0.9 WAKE.10 LPT0OUT1 ACCTR0_LCPUL1	ADC0.2 CMP1P.1
PB1.0	Standard I/O	53	VIO	XBR 0	✓	LCD0.31		LPT0T4 INT0.12 ACCTR0_LCBIAS0	CMP0P.2

Table 6.3. Pin Definitions and Alternate Functions for SiM3L1x4 (Continued)

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB2.1	Standard I/O	28	VIORF	XBR0	✓		LPT0T9 INT1.1 WAKE.13 VIORFCLK	ADC0.3 CMP0N.4
PB2.2	Standard I/O	27	VIORF	XBR0	✓		LPT0T10 INT1.2 WAKE.14	ADC0.4 CMP1P.4
PB2.3	Standard I/O	26	VIORF	XBR0	✓		LPT0T11 INT1.3 WAKE.15	ADC0.5 CMP1N.4
PB2.4	Standard I/O	24	VIORF	XBR0	✓		LPT0T12 INT1.4 SPI1_SCLK	ADC0.6 CMP0P.5
PB2.5	Standard I/O	23	VIORF	XBR0	✓		LPT0T13 INT1.5 SPI1_MISO	ADC0.7 CMP0N.5
PB2.6	Standard I/O	22	VIORF	XBR0	✓		LPT0T14 INT1.6 SPI1_MOSI	ADC0.8 CMP1P.5
PB2.7	Standard I/O	21	VIORF	XBR0	✓		INT1.7 SPI1_NSS	ADC0.9 CMP1N.5
PB3.0	Standard I/O	20	VIO	XBR0	✓		INT1.8	CMP0N.7
PB3.1	Standard I/O	19	VIO	XBR0	✓		INT1.9	CMP1P.7
PB3.2	Standard I/O	18	VIO	XBR0	✓		INT1.10	CMP1N.7
PB3.3	Standard I/O	17	VIO	XBR0	✓		INT1.11	ADC0.10
PB3.4	Standard I/O	16	VIO	XBR0	✓		INT1.12	ADC0.11
PB3.5	Standard I/O	15	VIO	XBR0	✓		INT1.13	ADC0.12

6.4. TQFP-80 Package Specifications

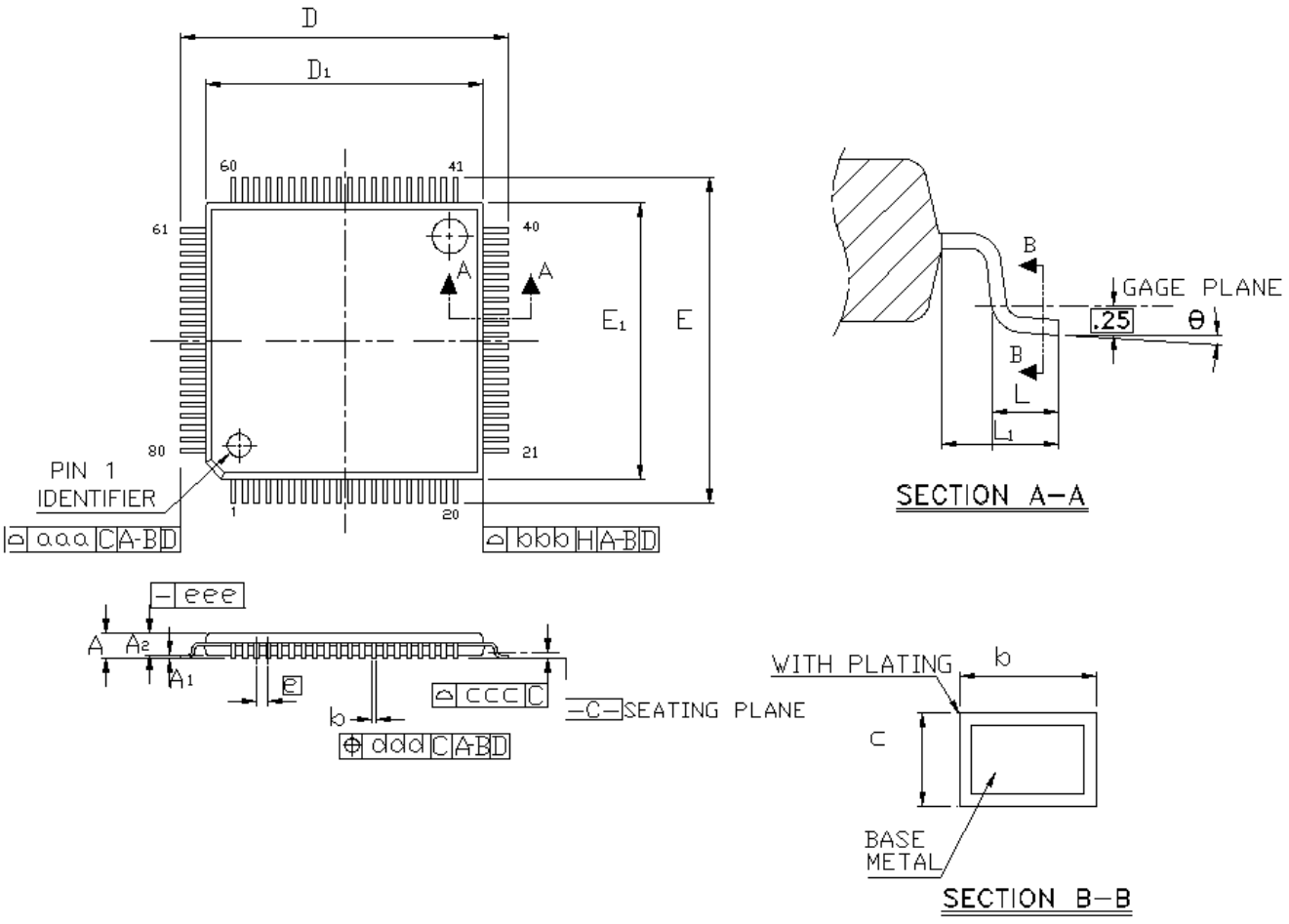

Figure 6.5. TQFP-80 Package Drawing

Table 6.4. TQFP-80 Package Dimensions

Dimension	Min	Nominal	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.20	0.27
c	0.09	—	0.20
D	14.00 BSC		
D1	12.00 BSC		
e	0.50 BSC		
E	14.00 BSC		
E1	12.00 BSC		
L	0.45	0.60	0.75
L1	1.00 Ref		
Θ	0°	3.5°	7°
aaa	0.20		
bbb	0.20		
ccc	0.08		
ddd	0.08		
eee	0.05		

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant ADD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.5. QFN-64 Package Specifications

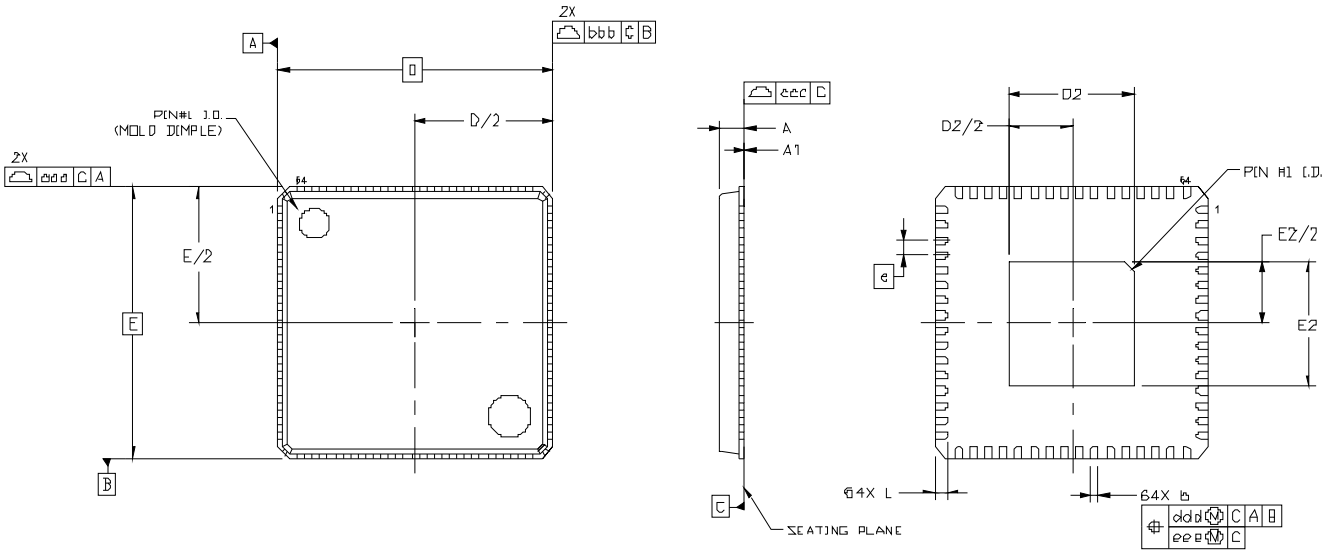

Figure 6.7. QFN-64 Package Drawing

Table 6.6. QFN-64 Package Dimensions

Dimension	Min	Nominal	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		9.00 BSC	
D2	3.95	4.10	4.25
e		0.50 BSC	
E		9.00 BSC	
E2	3.95	4.10	4.25
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.