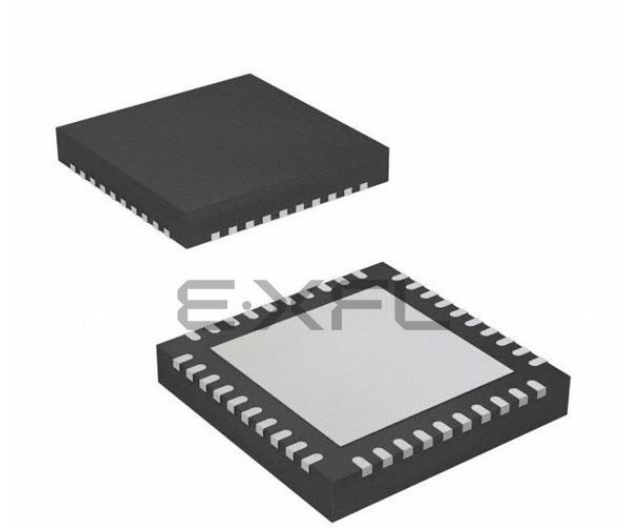

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	28
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 20x10/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/sim3l164-c-gmr

1. Related Documents and Conventions

1.1. Related Documents

This data sheet accompanies several documents to provide the complete description of the SiM3L1xx devices.

1.1.1. SiM3L1xx Reference Manual

The Silicon Laboratories SiM3L1xx Reference Manual provides the detailed description for each peripheral on the SiM3L1xx devices.

1.1.2. Hardware Access Layer (HAL) API Description

The Silicon Laboratories Hardware Access Layer (HAL) API provides C-language functions to modify and read each bit in the SiM3L1xx devices. This description can be found in the SiM3xxxx HAL API Reference Manual.

1.1.3. ARM Cortex-M3 Reference Manual

The ARM-specific features like the Nested Vectored Interrupt Controller are described in the ARM Cortex-M3 reference documentation. The online reference manual can be found here:
http://infocenter.arm.com/help/topic/com.arm.doc.subset.cortexm3/index.html#cortexm3.

1.2. Conventions

The block diagrams in this document use the following formatting conventions:

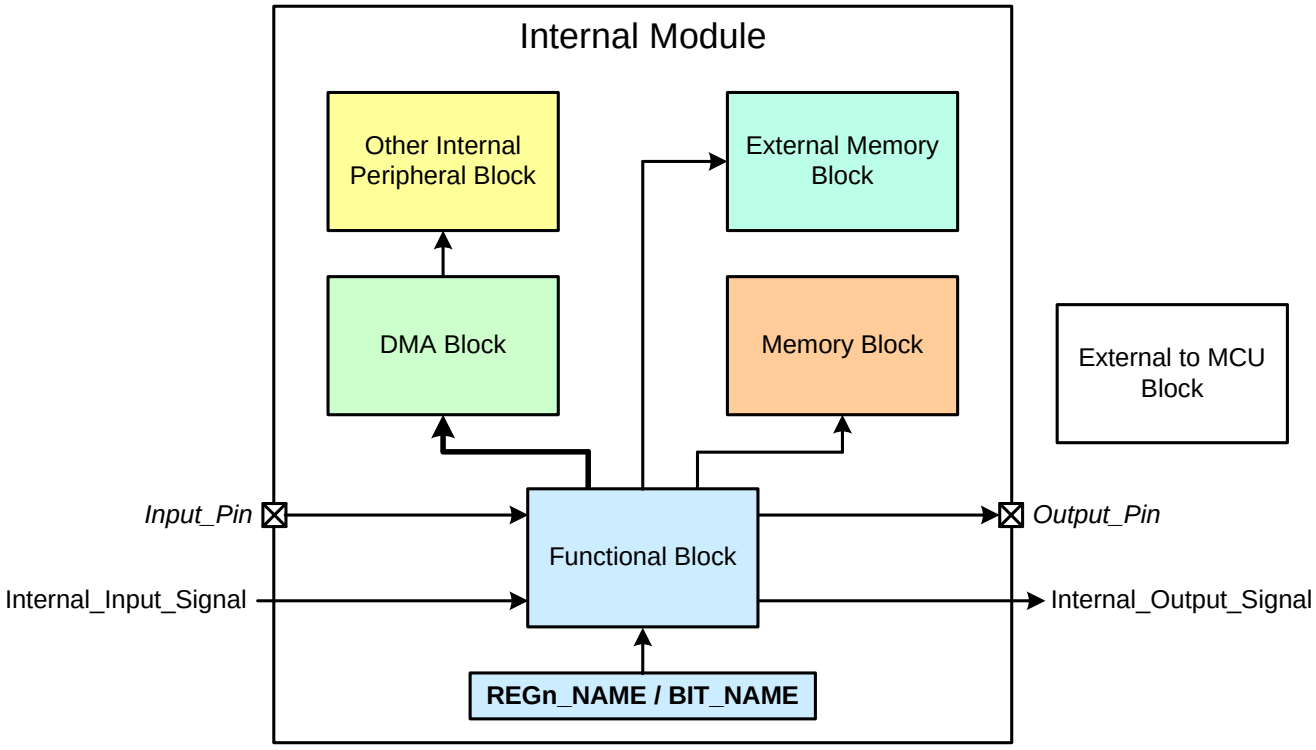


Figure 1.1. Block Diagram Conventions

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 8[1,2]—Low Power Sleep, powered by the low power mode charge pump, 32kB of retention RAM	I_{BAT}	RTC w/ 16.4 kHz LFO, V_{BAT} = 2.4 V, T_A = 25 °C	—	180	—	nA
		RTC w/ 32.768 kHz Crystal, V_{BAT} = 2.4 V, T_A = 25 °C	—	300	—	nA
		RTC w/ 16.4 kHz LFO, V_{BAT} = 3.8 V, T_A = 25 °C	—	245	—	nA
		RTC w/ 32.768 kHz Crystal, V_{BAT} = 3.8 V, T_A = 25 °C	—	390	—	nA
Unloaded V_{IO} and V_{IORF} Current[10]	I_{VIO}		—	2	—	nA
Power Mode 8 Peripheral Currents						
UART0	I_{UART0}	V_{BAT} = 3.8 V, T_A = 25 °C	—	195	600	nA
		V_{BAT} = 2.4 V, T_A = 25 °C	—	120	—	nA
LCD0[7], No segments active	I_{LCD0}	V_{BAT} = 3.8 V, T_A = 25 °C	—	495	660	nA
		V_{BAT} = 2.4 V, T_A = 25 °C	—	395	—	nA
LCD0[7], All (4 x 40) segments active	I_{LCD0}	V_{BAT} = 3.8 V, T_A = 25 °C	—	800	—	nA
		V_{BAT} = 2.4 V, T_A = 25 °C	—	580	—	nA
Advanced Capture Counter (ACCTR0), LC Single-Ended Mode, Relative to Sampling Frequency[9]	I_{ACCTR}	V_{BAT} = 2.4 V, T_A = 25 °C, CPMD = 01	—	1.11	—	nA/Hz
		V_{BAT} = 3.8 V, T_A = 25 °C, CPMD = 01	—	1.44	—	nA/Hz
		V_{BAT} = 2.4 V, T_A = 25 °C, CPMD = 10	—	1.45	—	nA/Hz
		V_{BAT} = 3.8 V, T_A = 25 °C, CPMD = 10	—	1.82	—	nA/Hz
		V_{BAT} = 2.4 V, T_A = 25 °C, CPMD = 11	—	2.15	—	nA/Hz
		V_{BAT} = 3.8 V, T_A = 25 °C, CPMD = 11	—	2.54	—	nA/Hz

Notes:

1. Currents are additive. For example, where I_{BAT} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded I_{VIO} is included in all I_{BAT} PM8 production test measurements.

Table 3.3. Power Mode Wake Up Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 2 or 6 Wake Time	t_{PM2}		4	—	5	clocks
Power Mode 3 Fast Wake Time (using LFO as clock source)	t_{PM3FW}		—	425	—	µs
Power Mode 8 Wake Time	t_{PM8}		—	3.8	—	µs

Notes:
1. Wake times are specified as the time from the wake source to the execution phase of the first instruction following WFI. This includes latency to recognize the wake event and fetch the first instruction (assuming wait states = 0).

Table 3.4. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{BAT} High Supply Monitor Threshold (VBATHITHEN = 1)	V_{VBATMH}	Early Warning	—	2.20	—	V
		Reset	1.95	2.05	2.1	V
V_{BAT} Low Supply Monitor Threshold (VBATHITHEN = 0)	V_{VBATML}	Early Warning	—	1.85	—	V
		Reset	1.70	1.75	1.77	V
Power-On Reset (POR) Threshold	V_{POR}	Rising Voltage on V_{BAT}	—	1.4	—	V
		Falling Voltage on V_{BAT}	0.8	1	1.3	V
V_{BAT} Ramp Time	t_{RMP}	Time to $V_{BAT} \geq 1.8$ V	10	—	3000	µs
Reset Delay from POR	t_{POR}	Relative to $V_{BAT} \geq V_{POR}$	3	—	100	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	10	—	µs
$\overline{\text{RESET}}$ Low Time to Generate Reset	t_{RSTL}		50	—	—	ns
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	$F_{AHB} > 1$ MHz	—	0.5	1.5	ms
Missing Clock Detector Trigger Frequency	F_{MCD}		—	2.5	10	kHz
V_{BAT} Supply Monitor Turn-On Time	t_{MON}		—	2	—	µs

Table 3.7. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Phase-Locked Loop (PLL0OSC)						
Calibrated Output Frequency (Free-running output mode, RANGE = 2)	$f_{PLL0OSC}$	Full Temperature and Supply Range	48.3	49	49.7	MHz
Power Supply Sensitivity (Free-running output mode, RANGE = 2)	$PSS_{PLL0OSC}$	T_A = 25 °C, Fout = 49 MHz	—	300	—	ppm/V
Temperature Sensitivity (Free-running output mode, RANGE = 2)	$TS_{PLL0OSC}$	V_{BAT} = 3.3 V, Fout = 49 MHz	—	50	—	ppm/°C
Adjustable Output Frequency Range	$f_{PLL0OSC}$		23	—	50	MHz
Lock Time	$t_{PLL0LOCK}$	f_{REF} = 20 MHz, $f_{PLL0OSC}$ = 50 MHz M=39, N=99, LOCKTH = 0	—	2.75	—	µs
		f_{REF} = 2.5 MHz, $f_{PLL0OSC}$ = 50 MHz M=19, N=399, LOCKTH = 0	—	9.45	—	µs
		f_{REF} = 32.768 kHz, $f_{PLL0OSC}$ = 50 MHz M=0, N=1524, LOCKTH = 0	—	92	—	µs
Low Power Oscillator (LPOSC0)						
Oscillator Frequency	f_{LPOSC}	Full Temperature and Supply Range	19	20	21	MHz
Divided Oscillator Frequency	f_{LPOSCD}	Full Temperature and Supply Range	2.375	2.5	2.625	MHz
Power Supply Sensitivity	PSS_{LPOSC}	T_A = 25 °C	—	0.5	—	%/V
Temperature Sensitivity	TS_{LPOSC}	V_{BAT} = 3.3 V	—	55	—	ppm/°C
Low Frequency Oscillator (LFOSC0)						
Oscillator Frequency	f_{LFOSC}	Full Temperature and Supply Range	13.4	16.4	19.7	kHz
		T_A = 25 °C, V_{BAT} = 3.3 V	15.8	16.4	17.3	kHz
Power Supply Sensitivity	PSS_{LFOSC}	T_A = 25 °C	—	2.4	—	%/V
Temperature Sensitivity	TS_{LFOSC}	V_{BAT} = 3.3 V	—	0.2	—	%/°C

Table 3.7. Internal Oscillators (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RTC0 Oscillator (RTC0OSC)						
Missing Clock Detector Trigger Frequency	f_{RTCMCD}		—	8	15	kHz
RTC External Input CMOS Clock Frequency	$f_{RTCEXTCLK}$		0	—	40	kHz
RTC Robust Duty Cycle Range	DC_{RTC}		25	—	55	%

Table 3.8. External Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency	f_{CMOS}		0*	—	50	MHz
External Crystal Frequency	f_{XTAL}		0.01	—	25	MHz
External Input CMOS Clock High Time	t_{CMOSH}		9	—	—	ns
External Input CMOS Clock Low Time	t_{CMOSL}		9	—	—	ns
Low Power Mode Charge Pump Supply Range (input from V_{BAT})	V_{BAT}		2.4	—	3.8	V
***Note:** Minimum of 10 kHz when debugging.						

Table 3.14. Comparator (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CMPHYP = 00	—	1.37	—	mV
		CMPHYP = 01	—	3.8	—	mV
		CMPHYP = 10	—	7.8	—	mV
		CMPHYP = 11	—	15.6	—	mV
Negative Hysteresis Mode 3 (CPMD = 11)	HYS_{CP-}	CMPHYN = 00	—	1.37	—	mV
		CMPHYN = 01	—	–3.9	—	mV
		CMPHYN = 10	—	–7.9	—	mV
		CMPHYN = 11	—	–16	—	mV
Input Range (CP+ or CP–)	V_{IN}		–0.25	—	V_{BAT} + 0.25	V
Input Pin Capacitance	C_{CP}		—	7.5	—	pF
Common-Mode Rejection Ratio	$CMRR_{CP}$		—	75	—	dB
Power Supply Rejection Ratio	$PSRR_{CP}$		—	72	—	dB
Input Offset Voltage	V_{OFF}	T_A = 25 °C	–10	0	10	mV
Input Offset Tempco	TC_{OFF}		—	3.5	—	µV/°C
Reference DAC Resolution	N_{Bits}			6		bits

Table 3.15. LCD0

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Charge Pump Output Voltage Error	V_{CPERR}		—	±50	—	mV
LCD Clock Frequency	F_{LCD}		16	—	33	kHz

4.1. Power

The SiM3L1xx devices include a dc-dc buck converter that can take an input from 1.8–3.8 V and create an output from 1.25–3.8 V. In addition, SiM3L1xx devices include three low dropout regulators as part of the LDO0 module: one LDO powers the analog subsystems, one LDO powers the flash and SRAM memory at 1.8 V, and one LDO powers the digital and core circuitry. Each of these regulators can be independently powered from the dc-dc converter or directly from the battery voltage, and their outputs are adjustable to conserve system power. SiM3L1xx devices also include a low power charge pump in the PMU module for use in low power modes (PM8) to further reduce the power consumption of the device.

Figure 4.2 shows the power system configuration of these devices.

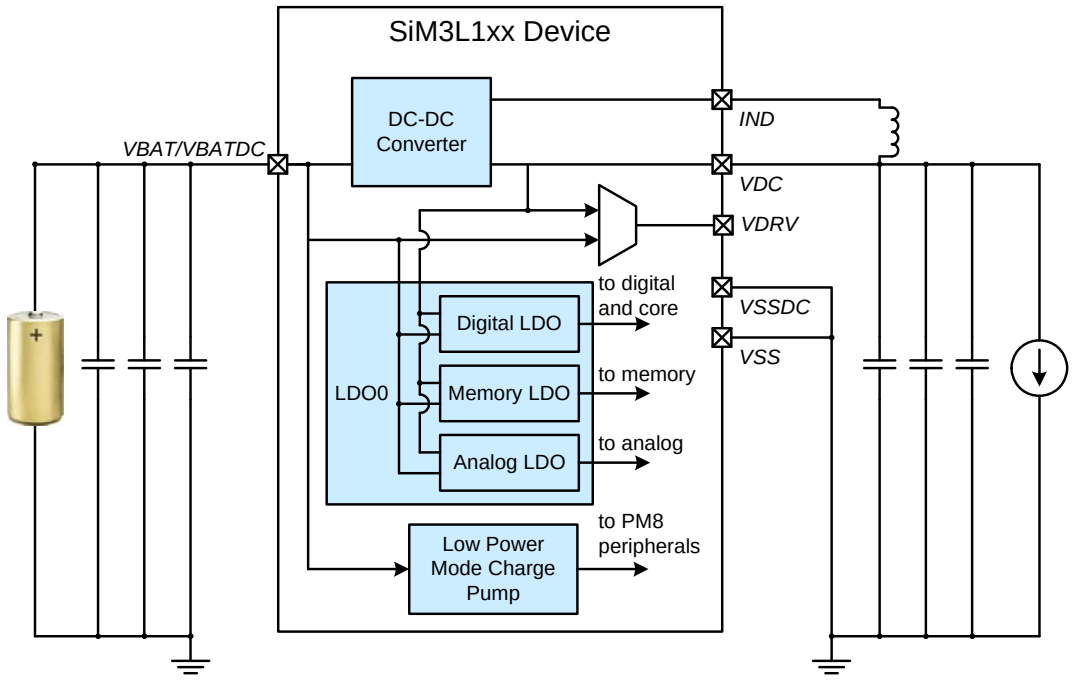


Figure 4.2. SiM3L1xx Power

4.1.1. DC-DC Buck Converter (DCDC0)

SiM3L1xx devices include an on-chip step-down dc-dc converter to efficiently utilize the energy stored in the battery, thus extending the operational life time. The dc-dc converter is a switching buck converter with a programmable output voltage that should be at least 0.45 V lower than the input battery voltage; if this criteria is not met and the converter can no longer operate, the output of the dc-dc converter automatically connects to the battery. The dc-dc converter can supply up to 100 mA and can be used to power the MCU and/or external devices in the system.

The dc-dc converter has a built in voltage reference and oscillator and will automatically limit or turn off the switching activity in case the peak inductor current rises beyond a safe limit or the output voltage rises above the programmed target value. This allows the dc-dc converter output to be safely overdriven by a secondary power source (when available) in order to preserve battery life. When enabled, the dc-dc converter can source current into the output capacitor, but cannot sink current.

The dc-dc converter includes the following features:

- Efficiently utilizes the energy stored in a battery, extending its operational lifetime.
- Input range: 1.8 to 3.8 V.
- Output range: 1.25 to 3.8 V in 50 mV (1.25–1.8 V) or 100 mV (1.8–3.8 V) steps.
- Supplies up to 100 mA.
- Includes a voltage reference and an oscillator.

4.1.6. Process/Voltage/Temperature Monitor (TIMER2 and PVTOSC0)

The Process/Voltage/Temperature monitor consists of two modules (TIMER2 and PVTOSC0) designed to monitor the digital circuit performance of the SiM3L1xx device.

The PVT oscillator (PVTOSC0) consists of two oscillators, one operating from the memory LDO and one operating from the digital LDO. These oscillators have two independent speed options and provide the clocks for two 16-bit timers in the TIMER2 module using the EX input. By monitoring the resulting counts of the TIMER2 timers, firmware can monitor the current device performance and increase the scalable LDO regulator (LDO0) output voltages as needed or decrease the output voltages to save power.

The PVT monitor has the following features:

- Two separate oscillators and timers for the memory and digital logic voltage domains.
- Two oscillator output divider settings.
- Provides a method for monitoring digital performance to allow firmware to adjust the scalable LDO regulator output voltages to the lowest level possible, saving power.

4.2. I/O

4.2.1. General Features

The SiM3L1xx ports have the following features:

- 5 V tolerant.
- Push-pull or open-drain output modes to the VIO or VIORF voltage level.
- Analog or digital modes.
- Option for high or low output drive strength.
- Port Match allows the device to recognize a change on a port pin value.
- Internal pull-up resistors are enabled or disabled on a port-by-port basis.
- Two external interrupts with up to 16 inputs each provide monitoring capability for external signals.
- Internal Pulse Generator Timer (PB0 only) to generate simple square waves and pulses.

4.2.2. Crossbar

The SiM3L1xx devices have one crossbar with the following features:

- Flexible peripheral assignment to port pins.
- Pins can be individually skipped to move peripherals as needed for design or layout considerations.

The crossbar has a fixed priority for each I/O function and assigns these functions to the port pins. When a digital resource is selected, the least-significant unassigned port pin is assigned to that resource. If a port pin is assigned, the crossbar skips that pin when assigning the next selected resource. Additionally, the crossbar will skip port pins whose associated bits in the PBSKIPEN registers are set. This provides flexibility when designing a system: pins involved with sensitive analog measurements can be moved away from digital I/O, and peripherals can be moved around the chip as needed to ease layout constraints.

4.6. Counters/Timers

4.6.1. 32-bit Timer (TIMER0, TIMER1, TIMER2)

Each timer module is independent, and includes the following features:

- Operation as a single 32-bit or two independent 16-bit timers.
- Clocking options include the APB clock, the APB clock scaled using an 8-bit prescaler, the external oscillator, or falling edges on an external input pin (synchronized to the APB clock).
- Auto-reload functionality in both 32-bit and 16-bit modes.

TIMER0 and TIMER1 have the following features:

- Up/Down count capability, controlled by an external input pin.
- Rising and falling edge capture modes.
- Low or high pulse capture modes.
- Period and duty cycle capture mode.
- Square wave output mode, which is capable of toggling an external pin at a given rate with 50% duty cycle.
- 32- or 16-bit pulse-width modulation mode.

TIMER2 does not support the standard input/output features of TIMER0 and TIMER1. The TIMER2 EX signal is internally connected to the outputs of the PVTOSC0 oscillators. TIMER2 can use any of the counting modes that use EX as an input, including up/down mode, edge capture mode, and pulse capture mode. The TIMER2 CT signal is disconnected.

4.6.2. Enhanced Programmable Counter Array (EPCA0)

The Enhanced Programmable Counter Array (EPCA) module is a timer/counter system allowing for complex timing or waveform generation. Multiple modules run from the same main counter, allowing for synchronous output waveforms.

This module includes the following features:

- Three sets of channel pairs (six channels total) capable of generating complementary waveforms.
- Center- and edge-aligned waveform generation.
- Programmable dead times that ensure channel pairs are never active at the same time.
- Programmable clock divisor and multiple options for clock source selection.
- Waveform update scheduling.
- Option to function while the core is inactive.
- Multiple synchronization triggers.
- Pulse-Width Modulation (PWM) waveform generation.

4.6.3. Real-Time Clock (RTC0)

The RTC module includes a 32-bit timer that allows up to 36 hours of independent time-keeping when used with a 32.768 kHz watch crystal. The RTC provides three alarm events in addition to a missing clock event, which can also function as interrupt, reset, or wakeup sources on SiM3L1xx devices.

The RTC module includes internal loading capacitors that are programmable to 16 discrete levels, allowing compatibility with a wide range of crystals.

The RTC timer clock can be buffered and routed to a port bank pin to provide an accurate, low frequency clock to other devices while the core is in its lowest power down mode. The module also includes a low power internal low frequency oscillator that reduces low power mode current and is available for other modules to use as a clock source.

The RTC module includes the following features:

- 32-bit timer (supports up to 36 hours) with three separate alarms.
- Option for one alarm to automatically reset the RTC timer.
- Missing clock detector.
- Can be used with the internal Low Frequency Oscillator or with an external 32.768 kHz crystal (no additional resistors or capacitors necessary).
- Programmable internal loading capacitors support a wide range of external 32.768 kHz crystals.
- The RTC timer clock (RTC0CLK) can be buffered and routed to an I/O pin to provide an accurate, low frequency clock to other devices while the core is in its lowest power down mode.
- The RTC module can be powered from the low power mode charge pump for lowest possible power consumption while in PM8.

4.6.4. Low Power Timer (LPTIMER0)

The Low Power Timer (LPTIMER) module runs from the RTC timer clock (RTC0CLK), allowing the LPTIMER to operate even if the AHB and APB clocks are disabled. The LPTIMER counter can increment using one of two clock sources: the clock selected by the RTC0 module, or rising or falling edges of an external signal.

The Low Power Timer includes the following features:

- Runs on low-frequency RTC timer clock (RTC0TCLK).
- The LPTIMER counter can increment using one of two clock sources: the RTC0TCLK or rising or falling edges of an external signal.
- Overflow and threshold-match detection.
- Timer reset on threshold-match allows square-wave generation at a variable output frequency.
- Supports PWM with configurable period and duty cycle.
- The LPTIMER module can be powered from the low power mode charge pump for lowest possible power consumption while in PM8.

4.6.5. Watchdog Timer (WDTIMER0)

The WDTIMER module includes a 16-bit timer, a programmable early warning interrupt, and a programmable reset period. The timer registers are protected from inadvertent access by an independent lock and key interface.

The watchdog timer runs from the low frequency oscillator (LFOSC0).

The Watchdog Timer has the following features:

- Programmable timeout interval.
- Optional interrupt to warn when the Watchdog Timer is nearing the reset trip value.
- Lock-out feature to prevent any modification until a system reset.

6.2. SiM3L1x6 Pin Definitions

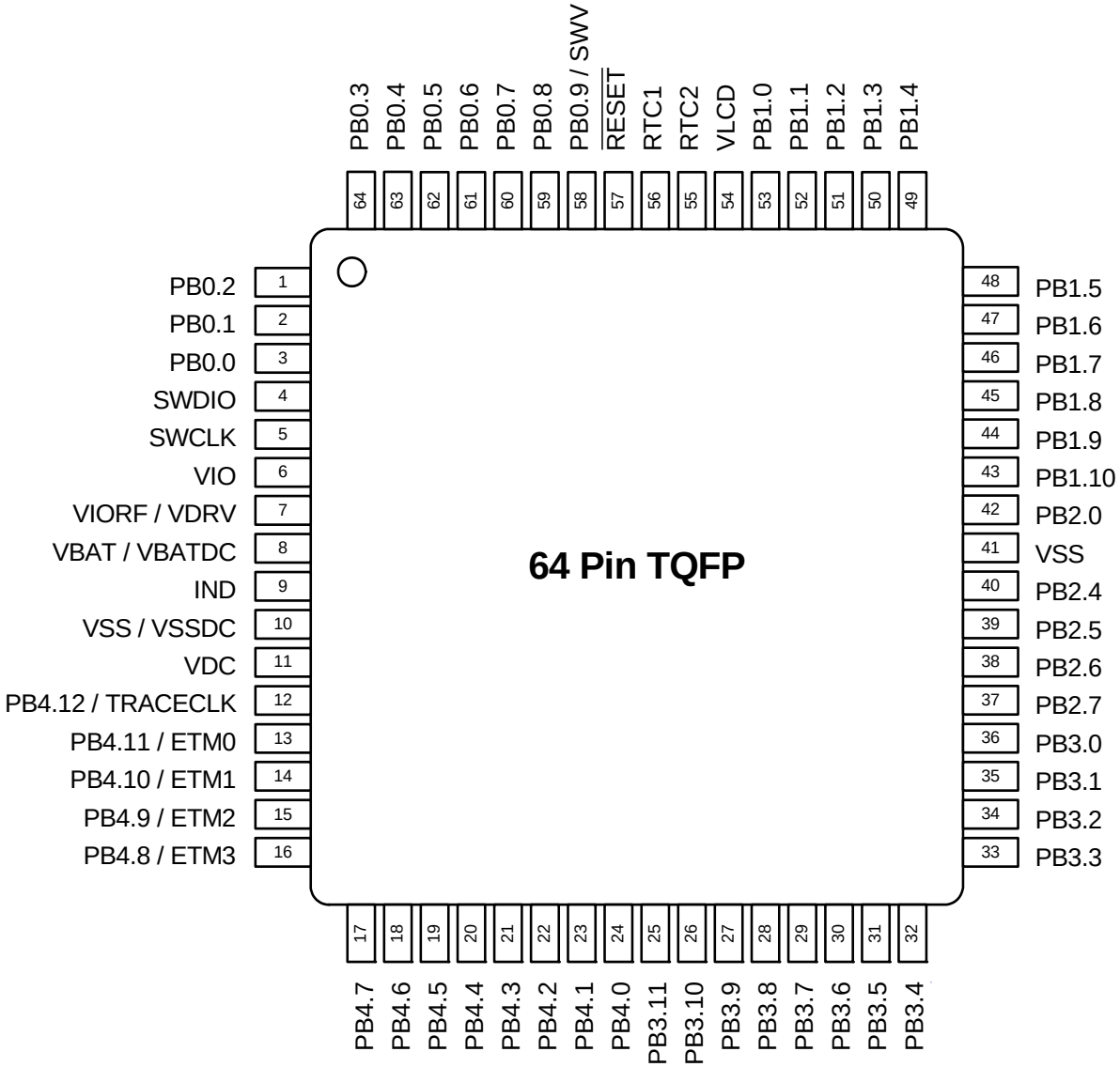


Figure 6.2. SiM3L1x6-GQ Pinout

Table 6.2. Pin Definitions and Alternate Functions for SiM3L1x6

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
VSS	Ground	10 41							
VSSDC	Ground (DC-DC)	10							
VIO	Power (I/O)	6							
VIORF / VDRV	Power (RF I/O)	7							
VBAT / VBATDC		8							
VDC		11							
VLCD	Power (LCD Charge Pump)	54							
IND	DC-DC Inductor	9							
$\overline{\text{RESET}}$	Active-low Reset	57							
SWCLK	Serial Wire	5							
SWDIO	Serial Wire	4							
RTC1	RTC Oscillator Input	56							
RTC2	RTC Oscillator Output	55							
PB0.0	Standard I/O	3	VIO	XBR 0	✓		✓	INT0.0 WAKE.0	ADC0.20 VREF CMP0P.0
PB0.1	Standard I/O	2	VIO	XBR 0	✓		✓	INT0.1 WAKE.2	ADC0.22 CMP0N.0 CMP1P.0 XTAL2

Table 6.3. Pin Definitions and Alternate Functions for SiM3L1x4 (Continued)

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB0.2	Standard I/O	40	VIO	XBR0	✓	✓	INT0.2 WAKE.3	ADC0.23 CMP0N.1 CMP1N.0 XTAL1
PB0.3	Standard I/O	39	VIO	XBR0	✓	✓	INT0.3 WAKE.4	ADC0.0 CMP0P.1 IDAC0
PB0.4	Standard I/O	38	VIO	XBR0	✓	✓	INT0.4 WAKE.5	ACCTR0_IN0
PB0.5	Standard I/O	37	VIO	XBR0	✓	✓	INT0.5 WAKE.6	ACCTR0_IN1
PB0.6/SWV	Standard I/O /Serial Wire Viewer	36	VIO	XBR0	✓	✓	LPT0T0 LPT0OUT0 INT0.6 WAKE.8	
PB0.7	Standard I/O	32	VIO	XBR0	✓	✓	LPT0T6 INT0.7 UART0_TX	CMP1P.2
PB0.8	Standard I/O	31	VIO	XBR0	✓	✓	LPT0T7 INT0.8 UART0_RX	CMP1N.2
PB0.9	Standard I/O	30	VIO	XBR0	✓	✓	LPT0T1 INT0.9 RTC0TCLK_OUT	ADC0.1
PB2.0	Standard I/O	29	VIORF	XBR0	✓		LPT0T8 INT1.0 WAKE.12 SPI1_CTS	ADC0.2 CMP0P.4

Table 6.3. Pin Definitions and Alternate Functions for SiM3L1x4 (Continued)

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB2.1	Standard I/O	28	VIORF	XBR0	✓		LPT0T9 INT1.1 WAKE.13 VIORFCLK	ADC0.3 CMP0N.4
PB2.2	Standard I/O	27	VIORF	XBR0	✓		LPT0T10 INT1.2 WAKE.14	ADC0.4 CMP1P.4
PB2.3	Standard I/O	26	VIORF	XBR0	✓		LPT0T11 INT1.3 WAKE.15	ADC0.5 CMP1N.4
PB2.4	Standard I/O	24	VIORF	XBR0	✓		LPT0T12 INT1.4 SPI1_SCLK	ADC0.6 CMP0P.5
PB2.5	Standard I/O	23	VIORF	XBR0	✓		LPT0T13 INT1.5 SPI1_MISO	ADC0.7 CMP0N.5
PB2.6	Standard I/O	22	VIORF	XBR0	✓		LPT0T14 INT1.6 SPI1_MOSI	ADC0.8 CMP1P.5
PB2.7	Standard I/O	21	VIORF	XBR0	✓		INT1.7 SPI1_NSS	ADC0.9 CMP1N.5
PB3.0	Standard I/O	20	VIO	XBR0	✓		INT1.8	CMP0N.7
PB3.1	Standard I/O	19	VIO	XBR0	✓		INT1.9	CMP1P.7
PB3.2	Standard I/O	18	VIO	XBR0	✓		INT1.10	CMP1N.7
PB3.3	Standard I/O	17	VIO	XBR0	✓		INT1.11	ADC0.10
PB3.4	Standard I/O	16	VIO	XBR0	✓		INT1.12	ADC0.11
PB3.5	Standard I/O	15	VIO	XBR0	✓		INT1.13	ADC0.12

Table 6.3. Pin Definitions and Alternate Functions for SiM3L1x4 (Continued)

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB3.6	Standard I/O	14	VIO	XBR0	✓		INT1.14	ADC0.13
PB3.7	Standard I/O	13	VIO	XBR0	✓		INT1.15	ADC0.14
PB3.8	Standard I/O	12	VIO		✓			ADC0.15
PB3.9	Standard I/O	11	VIO		✓			ADC0.16

6.4. TQFP-80 Package Specifications

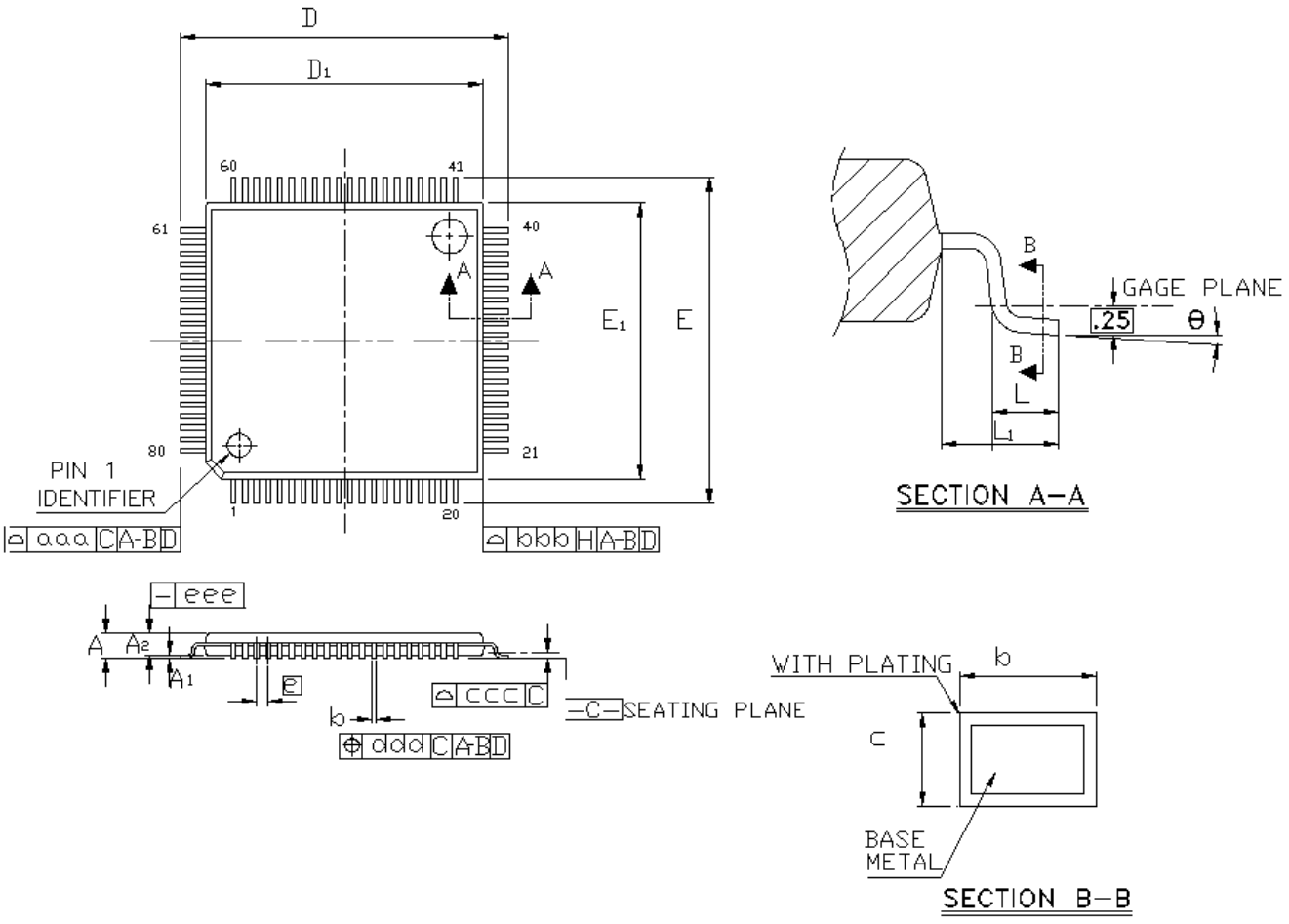


Figure 6.5. TQFP-80 Package Drawing

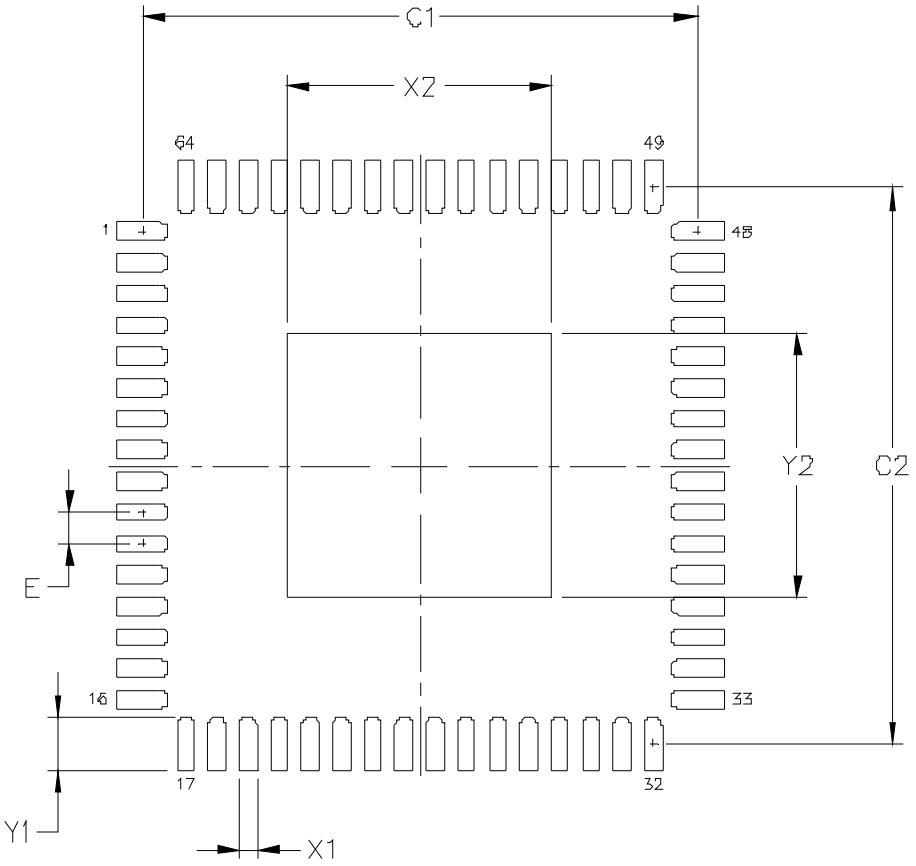


Figure 6.8. QFN-64 Landing Diagram

Table 6.7. QFN-64 Landing Diagram Dimensions

Dimension	mm
C1	8.90
C2	8.90
E	0.50
X1	0.30
Y1	0.85
X2	4.25
Y2	4.25

Notes:
1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

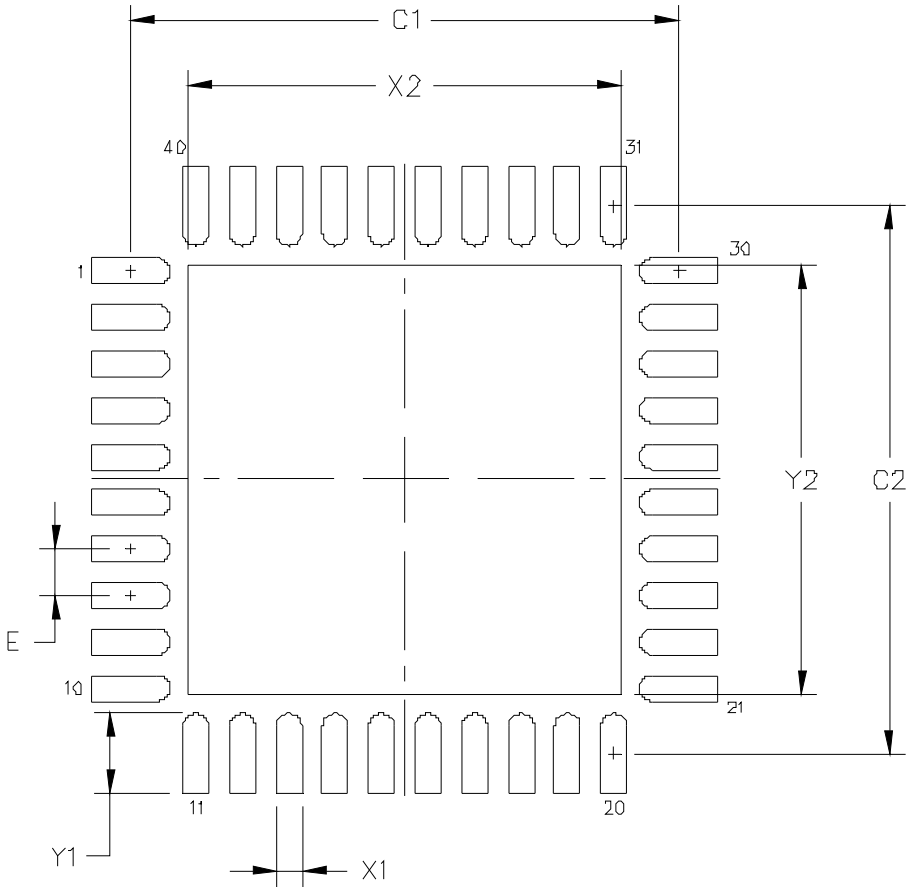
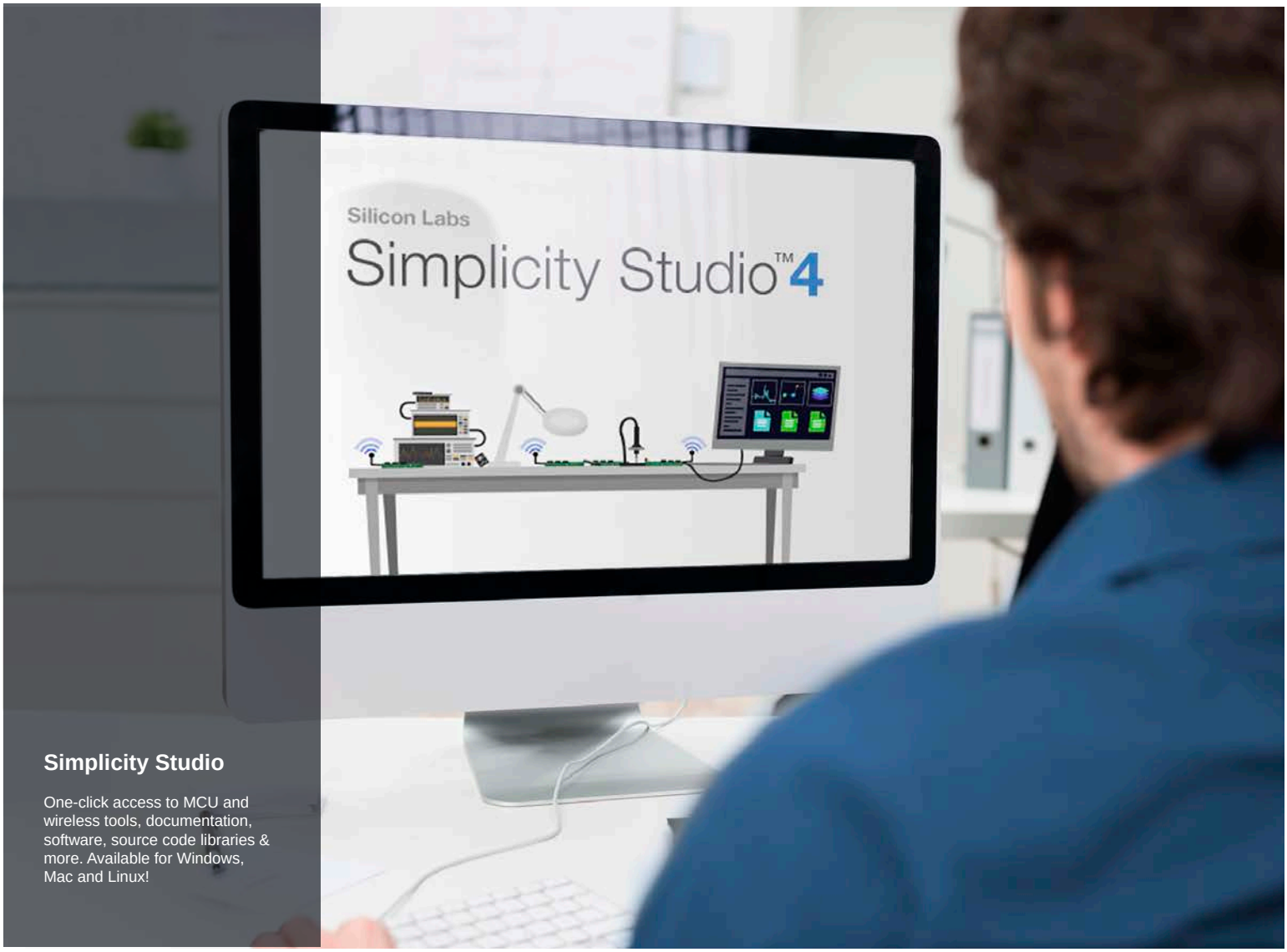


Figure 6.12. QFN-40 Landing Diagram

Table 6.11. QFN-40 Landing Diagram Dimensions

Dimension	mm
C1	5.90
C2	5.90
E	0.50
X1	0.30
Y1	0.85
X2	4.65
Y2	4.65

Notes:
1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.



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