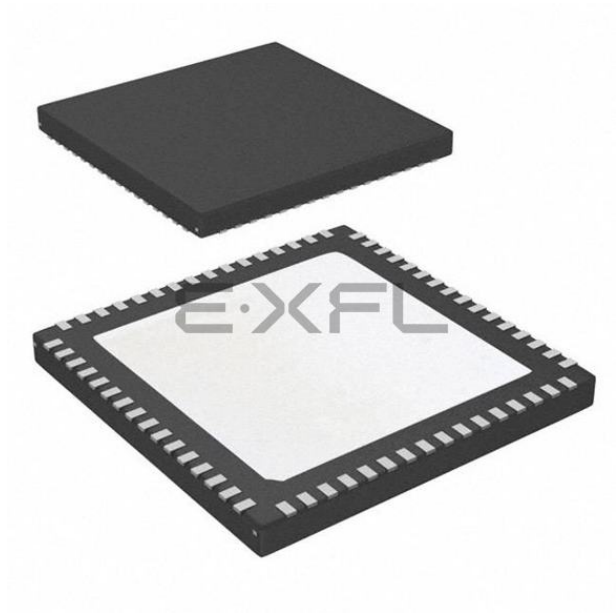

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EEPROM Size	-
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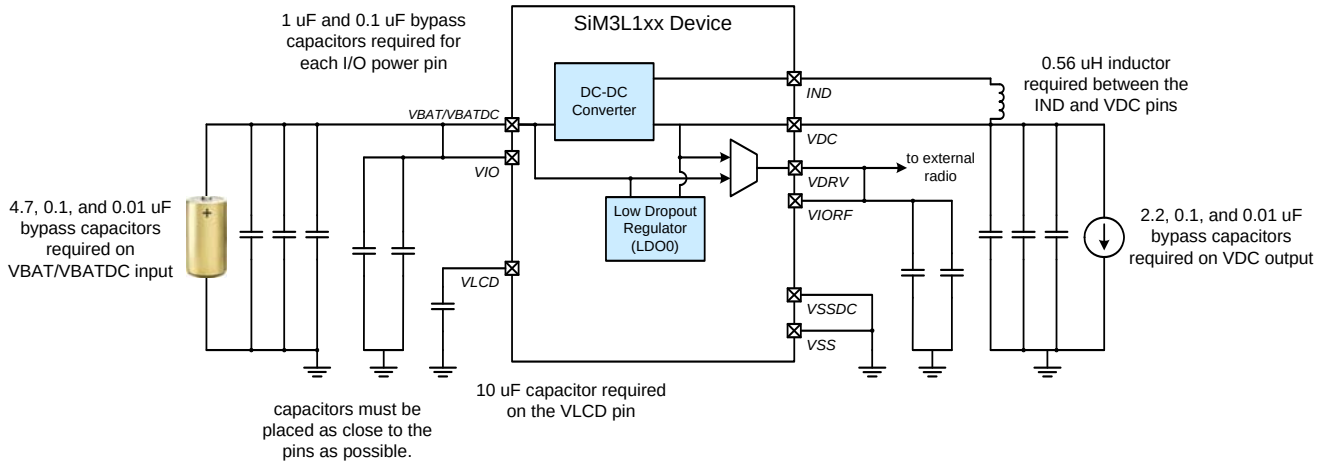

Figure 2.3. Connection Diagram with External Radio Device

Figure 2.4 shows a typical connection diagram for the power pins of the SiM3L1xx devices when the dc-dc buck converter is used and the I/O are powered separately.

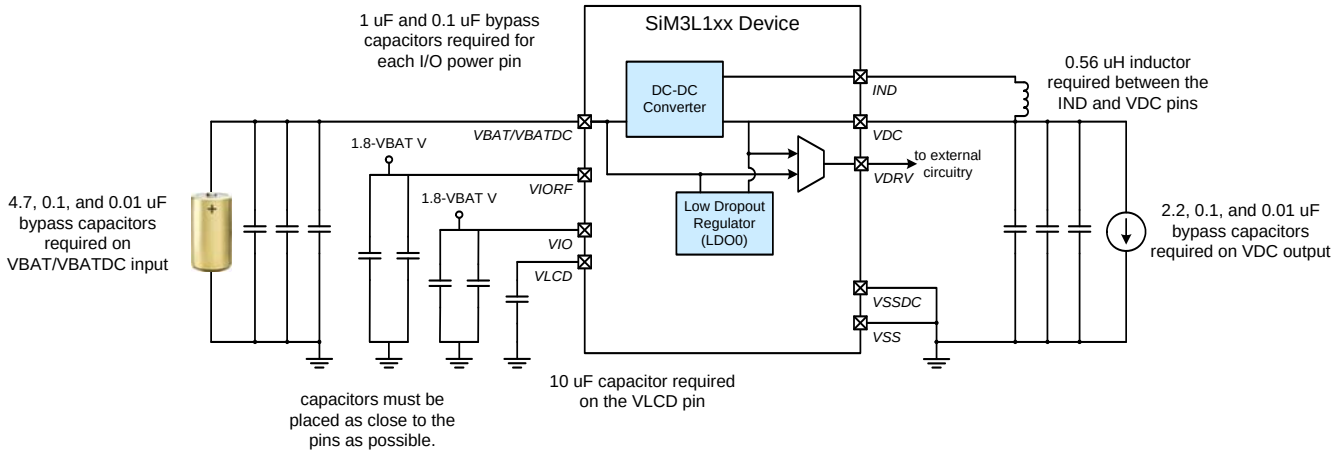

Figure 2.4. Connection Diagram with DC-DC Converter Used and I/O Powered Separately

3. Electrical Specifications

3.1. Electrical Characteristics

All electrical parameters in all Tables are specified under the conditions listed in Table 3.1, unless stated otherwise.

Table 3.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VBAT/VBATDC	V_{BAT}		1.8	—	3.8	V
Operating Supply Voltage on VDC	V_{DC}		1.25	—	3.8	V
Operating Supply Voltage on VDRV	V_{DRV}		1.25	—	3.8	V
Operating Supply Voltage on VIO	V_{IO}		1.8	—	V_{BAT}	V
Operation Supply Voltage on VIORF	V_{IORF}		1.8	—	V_{BAT}	V
Operation Supply Voltage on VLCD	V_{LCD}		1.8	—	3.8	V
System Clock Frequency (AHB)	f_{AHB}		0	—	50	MHz
Peripheral Clock Frequency (APB)	f_{APB}		0	—	50	MHz
Operating Ambient Temperature	T_A		–40	—	+85	°C
Operating Junction Temperature	T_J		–40	—	105	°C

Note: All voltages with respect to V_{SS}.

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 8[1,2]—Low Power Sleep, powered by the low power mode charge pump, 32kB of retention RAM	I_{BAT}	RTC w/ 16.4 kHz LFO, V_{BAT} = 2.4 V, T_A = 25 °C	—	180	—	nA
		RTC w/ 32.768 kHz Crystal, V_{BAT} = 2.4 V, T_A = 25 °C	—	300	—	nA
		RTC w/ 16.4 kHz LFO, V_{BAT} = 3.8 V, T_A = 25 °C	—	245	—	nA
		RTC w/ 32.768 kHz Crystal, V_{BAT} = 3.8 V, T_A = 25 °C	—	390	—	nA
Unloaded V_{IO} and V_{IORF} Current[10]	I_{VIO}		—	2	—	nA
Power Mode 8 Peripheral Currents						
UART0	I_{UART0}	V_{BAT} = 3.8 V, T_A = 25 °C	—	195	600	nA
		V_{BAT} = 2.4 V, T_A = 25 °C	—	120	—	nA
LCD0[7], No segments active	I_{LCD0}	V_{BAT} = 3.8 V, T_A = 25 °C	—	495	660	nA
		V_{BAT} = 2.4 V, T_A = 25 °C	—	395	—	nA
LCD0[7], All (4 x 40) segments active	I_{LCD0}	V_{BAT} = 3.8 V, T_A = 25 °C	—	800	—	nA
		V_{BAT} = 2.4 V, T_A = 25 °C	—	580	—	nA
Advanced Capture Counter (ACCTR0), LC Single-Ended Mode, Relative to Sampling Frequency[9]	I_{ACCTR}	V_{BAT} = 2.4 V, T_A = 25 °C, CPMD = 01	—	1.11	—	nA/Hz
		V_{BAT} = 3.8 V, T_A = 25 °C, CPMD = 01	—	1.44	—	nA/Hz
		V_{BAT} = 2.4 V, T_A = 25 °C, CPMD = 10	—	1.45	—	nA/Hz
		V_{BAT} = 3.8 V, T_A = 25 °C, CPMD = 10	—	1.82	—	nA/Hz
		V_{BAT} = 2.4 V, T_A = 25 °C, CPMD = 11	—	2.15	—	nA/Hz
		V_{BAT} = 3.8 V, T_A = 25 °C, CPMD = 11	—	2.54	—	nA/Hz

Notes:

1. Currents are additive. For example, where I_{BAT} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded I_{VIO} is included in all I_{BAT} PM8 production test measurements.

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Advanced Capture Counter (ACCTR0), LC Dual or Quadrature Mode, Relative to Sampling Frequency[9]	I_{ACCTR}	V_{BAT} = 2.4 V, T_A = 25 °C, CPMD = 01	—	1.39	—	nA/Hz
		V_{BAT} = 3.8 V, T_A = 25 °C, CPMD = 01	—	1.89	—	nA/Hz
		V_{BAT} = 2.4 V, T_A = 25 °C, CPMD = 10	—	2.08	—	nA/Hz
		V_{BAT} = 3.8 V, T_A = 25 °C, CPMD = 10	—	2.59	—	nA/Hz
		V_{BAT} = 2.4 V, T_A = 25 °C, CPMD = 11	—	3.47	—	nA/Hz
		V_{BAT} = 3.8 V, T_A = 25 °C, CPMD = 11	—	4.03	—	nA/Hz
Analog Peripheral Supply Currents						
PLL0 Oscillator (PLL0OSC)	I_{PLLOSC}	Operating at 49 MHz	—	1.4	1.6	mA
Low-Power Oscillator (LPOSC0)	I_{LPOSC}	Operating at 20 MHz	—	25	—	µA
		Operating at 2.5 MHz	—	25	—	µA
Low-Frequency Oscillator (LFOSC0)	I_{LFOSC}	Operating at 16.4 kHz	—	190	310	nA
External Oscillator (EXTOSC0)	I_{EXTOSC}	FREQCN = 111	—	3.8	4.5	mA
		FREQCN = 110	—	840	960	µA
		FREQCN = 101	—	185	230	µA
		FREQCN = 100	—	65	80	µA
		FREQCN = 011	—	25	30	µA
		FREQCN = 010	—	10	13	µA
		FREQCN = 001	—	5	7	µA
		FREQCN = 000	—	3	5	µA

Notes:

1. Currents are additive. For example, where I_{BAT} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded I_{VIO} is included in all I_{BAT} PM8 production test measurements.

Table 3.5. On-Chip Regulators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC-DC Buck Converter						
Input Voltage Range	V_{DCIN}		1.8	—	3.8	V
Input Supply to Output Voltage Differential (for regulation)	V_{DCREG}		0.45	—	—	V
Output Voltage Range	V_{DCOUT}		1.25	—	3.8	V
Output Voltage Accuracy	V_{DCACC}		—	±25	—	mV
Output Current	I_{DCOUT}		—	—	90	mA
Inductor Value[1]	L_{DC}		0.47	0.56	0.68	µH
Inductor Current Rating	I_{LDC}	I_{load} < 50 mA	450	—	—	mA
		I_{load} > 50 mA	550	—	—	mA
Output Capacitor Value	C_{DCOUT}		1	2.2	10	µF
Input Capacitor Value[2]	C_{DCIN}		—	4.7	—	µF
Load Regulation	R_{load}		—	0.03	—	mV/mA
Maximum DC Load Current During Startup	I_{DCMAX}		—	—	5	mA
Switching Clock Frequency	F_{DCCLK}		1.9	2.9	3.8	MHz
Local Oscillator Frequency	F_{DCOSC}		2.4	2.9	3.4	MHz
LDO Regulators						
Input Voltage Range[3]	V_{LDOIN}	Sourced from VBAT	1.8	—	3.8	V
		Sourced from VDC	1.9	—	3.8	V
Output Voltage Range[4]	V_{LDO}		0.8	—	1.9	V
LDO Output Voltage Accuracy	V_{LDOACC}		—	±25	—	mV
Output Settings in PM8 (All LDOs)	V_{LDO}	1.8 V ≤ V_{BAT} ≤ 2.9 V	1.5			V
		1.95 V ≤ V_{BAT} ≤ 3.5 V	1.8			V
		2.0 V ≤ V_{BAT} ≤ 3.8 V	1.9			V

Notes:

1. See reference manual for recommended inductors.
2. Recommended: X7R or X5R ceramic capacitors with low ESR. Example: Murata GRM21BR71C225K with ESR < 10 mΩ (@ frequency > 1 MHz).
3. Input voltage specification accounts for the internal LDO dropout voltage under the maximum load condition to ensure that the LDO output voltage will remain at a valid level as long as V_{LDOIN} is at or above the specified minimum.
4. The memory LDO output should always be set equal to or lower than the output of the analog LDO. When lowering both LDOs (for example to go into PM8 under low supply conditions), first adjust the memory LDO and then the analog LDO. When raising the output of both LDOs, adjust the analog LDO before adjusting the memory LDO.
5. Output range represents the programmable output range, and does not reflect the minimum voltage under all conditions. Dropout when the input supply is close to the output setting is normal, and accounted for.
6. Analog peripheral specifications assume a 1.8 V output on the analog LDO.

Table 3.7. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Phase-Locked Loop (PLL0OSC)						
Calibrated Output Frequency (Free-running output mode, RANGE = 2)	$f_{PLL0OSC}$	Full Temperature and Supply Range	48.3	49	49.7	MHz
Power Supply Sensitivity (Free-running output mode, RANGE = 2)	$PSS_{PLL0OSC}$	T_A = 25 °C, Fout = 49 MHz	—	300	—	ppm/V
Temperature Sensitivity (Free-running output mode, RANGE = 2)	$TS_{PLL0OSC}$	V_{BAT} = 3.3 V, Fout = 49 MHz	—	50	—	ppm/°C
Adjustable Output Frequency Range	$f_{PLL0OSC}$		23	—	50	MHz
Lock Time	$t_{PLL0LOCK}$	f_{REF} = 20 MHz, $f_{PLL0OSC}$ = 50 MHz M=39, N=99, LOCKTH = 0	—	2.75	—	µs
		f_{REF} = 2.5 MHz, $f_{PLL0OSC}$ = 50 MHz M=19, N=399, LOCKTH = 0	—	9.45	—	µs
		f_{REF} = 32.768 kHz, $f_{PLL0OSC}$ = 50 MHz M=0, N=1524, LOCKTH = 0	—	92	—	µs
Low Power Oscillator (LPOSC0)						
Oscillator Frequency	f_{LPOSC}	Full Temperature and Supply Range	19	20	21	MHz
Divided Oscillator Frequency	f_{LPOSCD}	Full Temperature and Supply Range	2.375	2.5	2.625	MHz
Power Supply Sensitivity	PSS_{LPOSC}	T_A = 25 °C	—	0.5	—	%/V
Temperature Sensitivity	TS_{LPOSC}	V_{BAT} = 3.3 V	—	55	—	ppm/°C
Low Frequency Oscillator (LFOSC0)						
Oscillator Frequency	f_{LFOSC}	Full Temperature and Supply Range	13.4	16.4	19.7	kHz
		T_A = 25 °C, V_{BAT} = 3.3 V	15.8	16.4	17.3	kHz
Power Supply Sensitivity	PSS_{LFOSC}	T_A = 25 °C	—	2.4	—	%/V
Temperature Sensitivity	TS_{LFOSC}	V_{BAT} = 3.3 V	—	0.2	—	%/°C

Table 3.9. SAR ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}	12 Bit Mode		12		Bits
		10 Bit Mode		10		Bits
Supply Voltage Requirements (VBAT)	V_{ADC}	High Speed Mode	2.2	—	3.8	V
		Low Power Mode	1.8	—	3.8	V
Throughput Rate (High Speed Mode)	f_S	12 Bit Mode	—	—	250	ksps
		10 Bit Mode	—	—	1	Msps
Throughput Rate (Low Power Mode)	f_S	12 Bit Mode	—	—	62.5	ksps
		10 Bit Mode	—	—	250	ksps
Tracking Time	t_{TRK}	High Speed Mode	230	—	—	ns
		Low Power Mode	450	—	—	ns
SAR Clock Frequency	f_{SAR}	High Speed Mode	—	—	16.24	MHz
		Low Power Mode	—	—	4	MHz
Conversion Time	t_{CNV}	10-Bit Conversion, SAR Clock = 16 MHz, APB Clock = 40 MHz		762.5		ns
Sample/Hold Capacitor	C_{SAR}	Gain = 1	—	5	—	pF
		Gain = 0.5	—	2.5	—	pF
Input Pin Capacitance	C_{IN}	High Quality Inputs	—	18	—	pF
		Normal Inputs	—	20	—	pF
Input Mux Impedance	R_{MUX}	High Quality Inputs	—	300	—	Ω
		Normal Inputs	—	550	—	Ω
Voltage Reference Range	V_{REF}		1	—	V_{BAT}	V
Input Voltage Range*	V_{IN}	Gain = 1	0	—	V_{REF}	V
		Gain = 0.5	0	—	$2xV_{REF}$	V
Power Supply Rejection Ratio	$PSRR_{ADC}$		—	70	—	dB
DC Performance						
Integral Nonlinearity	INL	12 Bit Mode	—	±1	±1.9	LSB
		10 Bit Mode	—	±0.2	±0.5	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL	12 Bit Mode	–1	±0.7	1.8	LSB
		10 Bit Mode	—	±0.2	±0.5	LSB
Offset Error (using VREFGND)	E_{OFF}	12 Bit Mode, VREF = 2.4 V	–2	0	2	LSB
		10 Bit Mode, VREF = 2.4 V	–1	0	1	LSB

Table 3.11. ACCTR (Advanced Capture Counter)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LC Comparator Response Time, CMPMD = 11 (Highest Speed)	t_{RESP0}	+100 mV Differential	—	100	—	ns
		–100 mV Differential	—	150	—	ns
LC Comparator Response Time, CMPMD = 00 (Lowest Power)	t_{RESP3}	+100 mV Differential	—	1.4	—	µs
		–100 mV Differential	—	3.5	—	µs
LC Comparator Positive Hysteresis Mode 0 (CPMD = 11)	HYS_{CP+}	CMPHYP = 00	—	0.37	—	mV
		CMPHYP = 01	—	7.9	—	mV
		CMPHYP = 10	—	16.7	—	mV
		CMPHYP = 11	—	32.8	—	mV
LC Comparator Negative Hysteresis Mode 0 (CPMD = 11)	HYS_{CP-}	CMPHYN = 00	—	0.37	—	mV
		CMPHYN = 01	—	–7.9	—	mV
		CMPHYN = 10	—	–16.1	—	mV
		CMPHYN = 11	—	–32.7	—	mV
LC Comparator Positive Hysteresis Mode 1 (CPMD = 10)	HYS_{CP+}	CMPHYP = 00	—	0.47	—	mV
		CMPHYP = 01	—	5.85	—	mV
		CMPHYP = 10	—	12	—	mV
		CMPHYP = 11	—	24.4	—	mV
LC Comparator Negative Hysteresis Mode 1 (CPMD = 10)	HYS_{CP-}	CMPHYN = 00	—	0.47	—	mV
		CMPHYN = 01	—	–6.0	—	mV
		CMPHYN = 10	—	–12.1	—	mV
		CMPHYN = 11	—	–24.6	—	mV
LC Comparator Positive Hysteresis Mode 2 (CPMD = 01)	HYS_{CP+}	CMPHYP = 00	—	0.66	—	mV
		CMPHYP = 01	—	4.55	—	mV
		CMPHYP = 10	—	9.3	—	mV
		CMPHYP = 11	—	19	—	mV
LC Comparator Negative Hysteresis Mode 2 (CPMD = 01)	HYS_{CP-}	CMPHYN = 00	—	0.6	—	mV
		CMPHYN = 01	—	–4.5	—	mV
		CMPHYN = 10	—	–9.5	—	mV
		CMPHYN = 11	—	–19	—	mV

Table 3.14. Comparator (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CMPHYP = 00	—	1.37	—	mV
		CMPHYP = 01	—	3.8	—	mV
		CMPHYP = 10	—	7.8	—	mV
		CMPHYP = 11	—	15.6	—	mV
Negative Hysteresis Mode 3 (CPMD = 11)	HYS_{CP-}	CMPHYN = 00	—	1.37	—	mV
		CMPHYN = 01	—	–3.9	—	mV
		CMPHYN = 10	—	–7.9	—	mV
		CMPHYN = 11	—	–16	—	mV
Input Range (CP+ or CP–)	V_{IN}		–0.25	—	V_{BAT} + 0.25	V
Input Pin Capacitance	C_{CP}		—	7.5	—	pF
Common-Mode Rejection Ratio	$CMRR_{CP}$		—	75	—	dB
Power Supply Rejection Ratio	$PSRR_{CP}$		—	72	—	dB
Input Offset Voltage	V_{OFF}	T_A = 25 °C	–10	0	10	mV
Input Offset Tempco	TC_{OFF}		—	3.5	—	µV/°C
Reference DAC Resolution	N_{Bits}			6		bits

Table 3.15. LCD0

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Charge Pump Output Voltage Error	V_{CPERR}		—	±50	—	mV
LCD Clock Frequency	F_{LCD}		16	—	33	kHz

4.2. I/O

4.2.1. General Features

The SiM3L1xx ports have the following features:

- 5 V tolerant.
- Push-pull or open-drain output modes to the VIO or VIORF voltage level.
- Analog or digital modes.
- Option for high or low output drive strength.
- Port Match allows the device to recognize a change on a port pin value.
- Internal pull-up resistors are enabled or disabled on a port-by-port basis.
- Two external interrupts with up to 16 inputs each provide monitoring capability for external signals.
- Internal Pulse Generator Timer (PB0 only) to generate simple square waves and pulses.

4.2.2. Crossbar

The SiM3L1xx devices have one crossbar with the following features:

- Flexible peripheral assignment to port pins.
- Pins can be individually skipped to move peripherals as needed for design or layout considerations.

The crossbar has a fixed priority for each I/O function and assigns these functions to the port pins. When a digital resource is selected, the least-significant unassigned port pin is assigned to that resource. If a port pin is assigned, the crossbar skips that pin when assigning the next selected resource. Additionally, the crossbar will skip port pins whose associated bits in the PBSKIPEN registers are set. This provides flexibility when designing a system: pins involved with sensitive analog measurements can be moved away from digital I/O, and peripherals can be moved around the chip as needed to ease layout constraints.

4.3.1. PLL (PLL0)

The PLL module consists of a dedicated Digitally-Controlled Oscillator (DCO) that can be used in Free-Running mode without a reference frequency, Frequency-Locked to a reference frequency, or Phase-Locked to a reference frequency. The reference frequency for Frequency-Lock and Phase-Lock modes can use one of multiple sources (including the external oscillator) to provide maximum flexibility for different application needs. Because the PLL module generates its own clock, the DCO can be locked to a particular reference frequency and then moved to Free-Running mode to reduce system power and noise.

The PLL module includes the following features:

- Three output ranges with output frequencies ranging from 23 to 50 MHz.
- Multiple reference frequency inputs, including the RTC0 oscillator, Low Power Oscillator, and external oscillator.
- Three output modes: Free-Running Digitally-Controlled Oscillator, Frequency-Locked, and Phase-Locked.
- Able to sense the rising edge or falling edge of the reference source.
- DCO frequency LSB dithering to provide finer average output frequencies.
- Spectrum spreading to reduce generated system noise.
- Low jitter and fast lock times.\
- All output frequency updates (including dithering and spectrum spreading) can be temporarily suspended using the STALL bit during noise-sensitive measurements.

4.3.2. Low Power Oscillator (LPOSC0)

The Low Power Oscillator is the default AHB oscillator on SiM3L1xx devices and enables or disables automatically, as needed.

The default output frequency of this oscillator is factory calibrated to 20 MHz, and a divided 2.5 MHz version of this clock is also available as an AHB clock source.

The Low Power Oscillator has the following features:

- 20 MHz and divided 2.5 MHz frequencies available for the AHB clock.
- Automatically starts and stops as needed.

4.3.3. Low Frequency Oscillator (LFOSC0)

The low frequency oscillator (LFOSC) provides a low power internal clock source for the RTC0 timer and other peripherals on the device. No external components are required to use the low frequency oscillator, and the RTC1 and RTC2 pins do not need to be shorted together.

The Low Frequency Oscillator has the following features:

- 16.4 kHz output frequency.

4.3.4. External Oscillators (EXTOSC0)

The EXTOSC0 external oscillator circuit may drive an external crystal, ceramic resonator, capacitor, or RC network. A CMOS clock may also provide a clock input. The external oscillator output may be selected as the AHB clock or used to clock other modules independent of the AHB clock selection.

The External Oscillator control has the following features:

- Support for external crystal, resonator, RC, C, or CMOS oscillators.
- Support for external CMOS frequencies from 10 kHz to 50 MHz.
- Support for external crystal frequencies from 10 kHz to 25 MHz.
- Various drive strengths for flexible crystal oscillator support.
- Internal frequency divide-by-two option available.

4.5. Data Peripherals

4.5.1. 10-Channel DMA Controller

The DMA facilitates autonomous peripheral operation, allowing the core to finish tasks more quickly without spending time polling or waiting for peripherals to interrupt. This helps reduce the overall power consumption of the system, as the device can spend more time in low-power modes.

The DMA controller has the following features:

- Utilizes ARM PrimeCell uDMA architecture.
- Implements 10 channels.
- DMA crossbar supports DTM0, DTM1, DTM2, SARADC0, IDAC0, I2C0, SPI0, SPI1, USART0, AES0, ENCDEC0, EPCA0, external pin triggers, and timers.
- Supports primary, alternate, and scatter-gather data structures to implement various types of transfers.
- Access allowed to all AHB and APB memory space.

4.5.2. Data Transfer Managers (DTM0, DTM1, DTM2)

The Data Transfer Manager is a module that collects DMA request signals from various peripherals and generates a series of master DMA requests based on a state-driven configuration. This master request drives a set of DMA channels to perform functions such as assembling and transferring communication packets to external devices. This capability saves power by allowing the core to remain in a low power mode during complex transfer operations. A combination of simple and peripheral scatter-gather DMA configurations can be used to perform complex operations while reducing memory requirements.

The DTM acts as a side channel for the peripheral's DMA control signals. When active, it manages the DMA control signals for the peripherals. When the DTMn module is inactive, the peripherals communicate directly to the DMA module.

The DTMn module has the following features:

- State descriptions stored in RAM with up to 15 states supported per module.
- Supports up to 15 source peripherals and up to 15 destination peripherals per module, in addition to memory or peripherals that do not require a data request.
- Includes error detection and an optional transfer timeout.
- Includes notifications for state transitions.

4.5.3. 128/192/256-bit Hardware AES Encryption (AES0)

The basic AES block cipher is implemented in hardware. The integrated hardware support for Cipher Block Chaining (CBC) and Counter (CTR) algorithms results in identical performance, memory bandwidth, and memory footprint between the most basic Electronic Codebook (ECB) algorithm and these more complex algorithms. This hardware accelerator translates to more core bandwidth available for other functions or a power savings for low-power applications.

The AES module includes the following features:

- Operates on 4-word (16-byte) blocks.
- Supports key sizes of 128, 192, and 256 bits for both encryption and decryption.
- Generates the round key for decryption operations.
- All cipher operations can be performed without any firmware intervention for multiple 4-word blocks (up to 32 kB).
- Support for various chained and stream-ciphering configurations with XOR paths on both the input and output.
- Internal 4-word FIFOs to facilitate DMA operations.
- Integrated key storage.
- Hardware acceleration for Electronic Codebook (ECB), Cipher-Block Chaining (CBC), and Counter (CTR) algorithms utilizing integrated counterblock generation and previous-block caching.

4.5.4. 16/32-bit Enhanced CRC (ECRC0)

The ECRC module is designed to provide hardware calculations for flash memory verification and communications protocols. In addition to calculating a result from direct writes from firmware, the ECRC module can automatically snoop the APB bus and calculate a result from data written to or read from a particular peripheral. This allows for an automatic CRC result without directly feeding data through the ECRC module.

The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3). The 16-bit polynomial is fully programmable.

The ECRC module includes the following features:

- Support for a programmable 16-bit polynomial and one fixed 32-bit polynomial.
- Byte-level bit reversal for the CRC input.
- Byte-order reorientation of words for the CRC input.
- Word or half-word bit reversal of the CRC result.
- Ability to configure and seed an operation in a single register write.
- Support for single-cycle parallel (unrolled) CRC computation for 32-, 16-, or 8-bit blocks.
- Capability to CRC 32 bits of data per peripheral bus (APB) clock.
- Automatic APB bus snooping.
- Support for DMA writes using firmware request mode.

4.5.5. Encoder / Decoder (ENCDEC0)

The encoder / decoder module supports Manchester and Three-out-of-Six encoding and decoding from either firmware or DMA operations.

This module has the following features:

- Supports Manchester and Three-out-of-Six encoding and decoding.
- Automatic flag clearing when writing the input or reading the output data registers.
- Writing to the input data register automatically initiates an encode or decode operation.
- Optional output in one’s complement format.
- Hardware error detection for invalid input data during decode operations, which helps reduce power consumption and packet turn-around time.
- Flexible byte swapping on the input or output data.

- Multiple loop-back modes supported.
- Multi-processor communications support.
- Operates at 9600, 4800, 2400, or 1200 baud in Power Mode 8.

4.7.3. SPI (SPI0, SPI1)

SPI is a 3- or 4-wire communication interface that includes a clock, input data, output data, and an optional select signal.

The SPI0 and SPI1 modules include the following features:

- Supports 3- or 4-wire master or slave modes.
- Supports up to 10 MHz clock in master mode and 5 MHz clock in slave mode.
- Support for all clock phase and slave select (NSS) polarity modes.
- 16-bit programmable clock rate.
- Programmable MSB-first or LSB-first shifting.
- 8-byte FIFO buffers for both transmit and receive data paths to support high speed transfers.
- Support for multiple masters on the same data lines.

In addition, the SPI modules include several features to support autonomous DMA transfers:

- Hardware NSS control.
- Programmable FIFO threshold levels.
- Configurable FIFO data widths.
- Master or slave hardware flow control for the MISO and MOSI signals.

SPI1 is on fixed pins and supports additional flow control options using a fixed input (SPI1CTS). Neither SPI1 nor the flow control input are on the crossbar.

4.7.4. I2C (I2C0)

The I2C interface is a two-wire, bi-directional serial bus. The clock and data signals operate in open-drain mode with external pull-ups to support automatic bus arbitration.

Reads and writes to the interface are byte oriented with the I2C interface autonomously controlling the serial transfer of the data. Data can be transferred at up to 1/8th of the APB clock as a master or slave, which can be faster than allowed by the I2C specification, depending on the clock source used. A method of extending the clock-low duration is available to accommodate devices with different speed capabilities on the same bus.

The I2C interface may operate as a master and/or slave, and may function on a bus with multiple masters. The I2C provides control of SDA (serial data), SCL (serial clock) generation and synchronization, arbitration logic, and start/stop control and generation.

The I2C0 module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds.
- Can operate down to APB clock divided by 32768 or up to APB clock divided by 8.
- Support for master, slave, and multi-master modes.
- Hardware synchronization and arbitration for multi-master mode.
- Clock low extending (clock stretching) to interface with faster masters.
- Hardware support for 7-bit slave and general call address recognition.
- Firmware support for 10-bit slave address decoding.
- Ability to disable all slave states.
- Programmable clock high and low period.
- Programmable data setup/hold times.
- Spike suppression up to 2 times the APB period.

4.9. Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.
- AHB peripheral clocks to flash and RAM are enabled.
- Clocks to all APB peripherals other than the Watchdog Timer and DMAXBAR are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost.

The Port I/O latches are reset to 1 in open-drain mode. Weak pullups are enabled during and after the reset. For VBAT Supply Monitor and power-on resets, the RESET pin is driven low until the device exits the reset state.

On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to the internal low-power oscillator. The Watchdog Timer is enabled with the low frequency oscillator as its clock source. Program execution begins at location 0x00000000.

All RSTSRC0 registers may be locked against writes by setting the CLKRSTL bit in the LOCK0_PERIPHLOCK0 register to 1.

The reset sources can also optionally reset individual modules, including the low power mode charge pump, UART0, LCD0, advanced capture counter (ACCTR0), and RTC0.

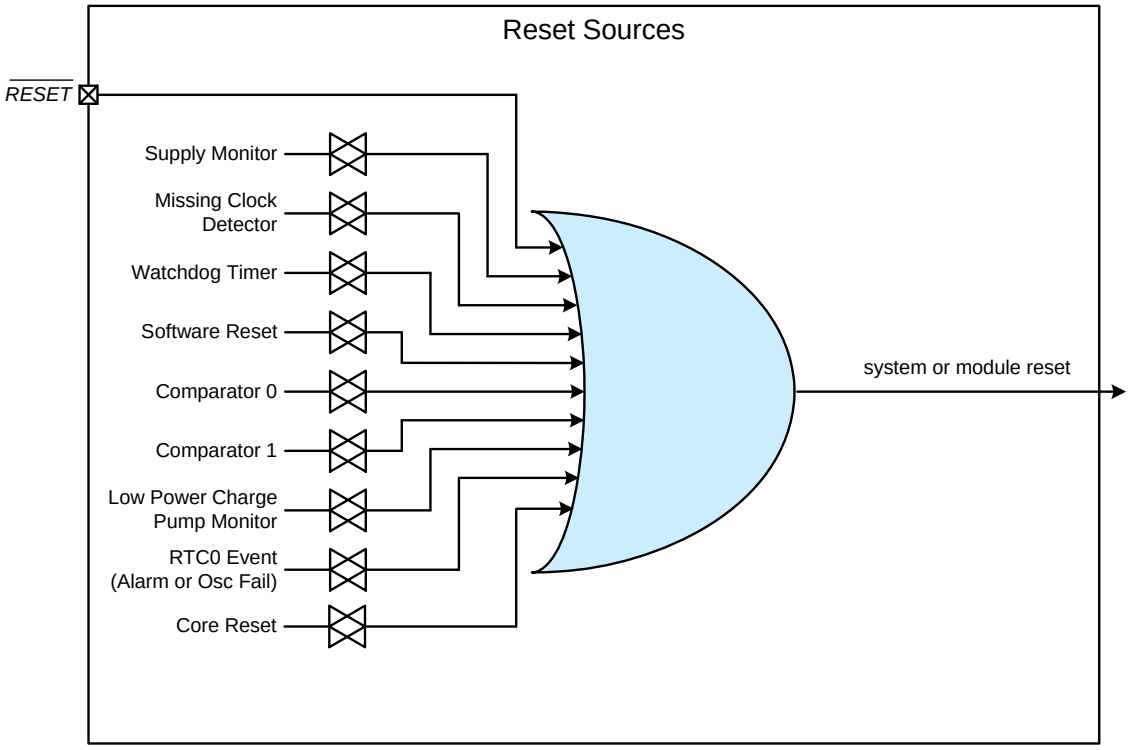

Figure 4.4. SiM3L1xx Reset Sources Block Diagram

Table 6.2. Pin Definitions and Alternate Functions for SiM3L1x6 (Continued)

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB0.2	Standard I/O	1	VIO	XBR 0	✓		✓	INT0.2 WAKE.3	ADC0.23 CMP1N.0 XTAL1
PB0.3	Standard I/O	64	VIO	XBR 0	✓		✓	INT0.3 WAKE.4	ADC0.0 CMP0P.1 IDAC0
PB0.4	Standard I/O	63	VIO	XBR 0	✓		✓	INT0.4 WAKE.5 ACCTR0_STOP0	ACCTR0_IN0
PB0.5	Standard I/O	62	VIO	XBR 0	✓		✓	INT0.5 WAKE.6 ACCTR0_STOP1	ACCTR0_IN1
PB0.6	Standard I/O	61	VIO	XBR 0	✓		✓	INT0.6 WAKE.7	ACCTR0_LCIN0
PB0.7	Standard I/O	60	VIO	XBR 0	✓		✓	LPT0T0 LPT0OUT0 INT0.7 WAKE.8	ACCTR0_LCIN1
PB0.8	Standard I/O	59	VIO	XBR 0	✓		✓	LPT0T1 INT0.8 WAKE.9 ACCTR0_LCPUL0	ADC0.1 CMP0N.1
PB0.9/SWV	Standard I/O /Serial Wire Viewer	58	VIO	XBR 0	✓		✓	LPT0T2 INT0.9 WAKE.10 LPT0OUT1 ACCTR0_LCPUL1	ADC0.2 CMP1P.1
PB1.0	Standard I/O	53	VIO	XBR 0	✓	LCD0.31		LPT0T4 INT0.12 ACCTR0_LCBIAS0	CMP0P.2

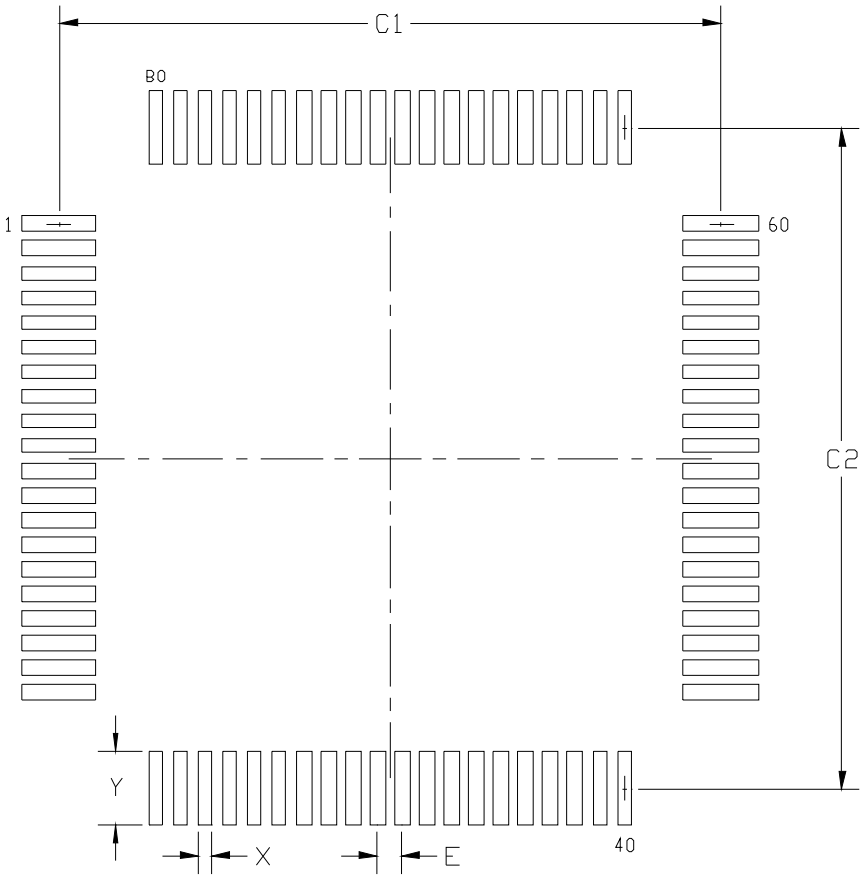

Figure 6.6. TQFP-80 Landing Diagram

Table 6.5. TQFP-80 Landing Diagram Dimensions

Dimension	Min	Max
C1	13.30	13.40
C2	13.30	13.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

6.7.1. QFN-40 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.7.2. QFN-40 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 3x3 array of 1.1 mm square openings on a 1.6 mm pitch should be used for the center ground pad.

6.7.3. QFN-40 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. Revision Specific Behavior

This chapter describes any differences between released revisions of the device.

7.1. Revision Identification

The Lot ID Code on the top side of the device package can be used for decoding device revision information. Figures 7.1, 7.2, and 7.3 show how to find the Lot ID Code on the top side of the device package.

In addition, firmware can determine the revision of the device by checking the DEVICEID registers.

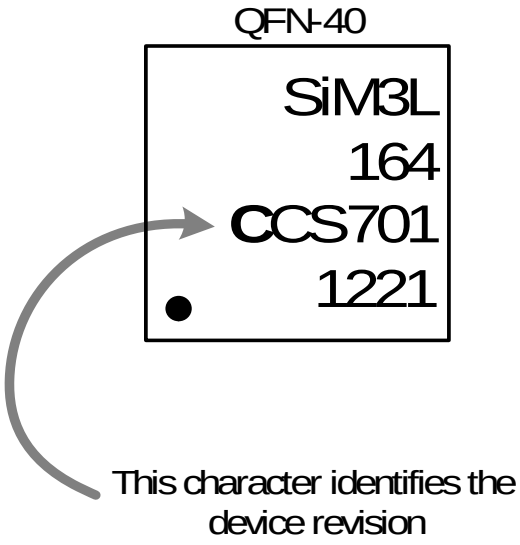

Figure 7.1. SiM3L1x7-GQ Revision Information

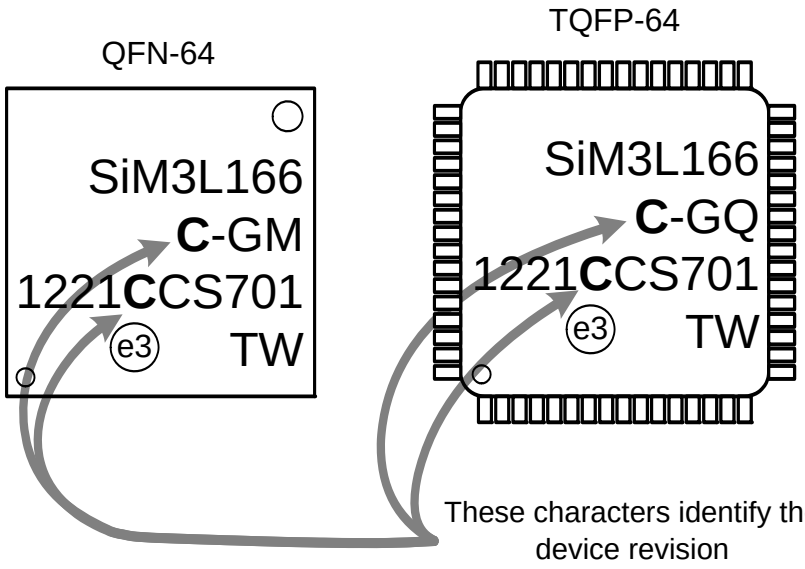

Figure 7.2. SiM3L1x6-GM and SiM3L1x6-GQ Revision Information