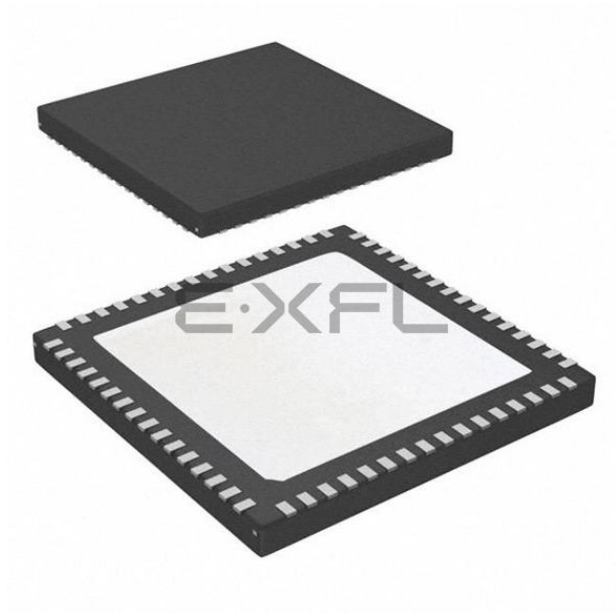

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | I²C, IrDA, SmartCard, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT |
| Number of I/O | 51 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.8V |
| Data Converters | A/D 23x10/12b; D/A 1x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-VFQFN Exposed Pad |
| Supplier Device Package | 64-QFN (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/sim3l166-c-gmr |

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**Table 3.2. Power Consumption (Continued)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Advanced Capture Counter (ACCTR0), LC Dual or Quadrature Mode, Relative to Sampling Frequency[9] | $I_{ACCTR}$ | $V_{BAT}$ = 2.4 V, $T_A$ = 25 °C, CPMD = 01 | — | 1.39 | — | nA/Hz |
| | | $V_{BAT}$ = 3.8 V, $T_A$ = 25 °C, CPMD = 01 | — | 1.89 | — | nA/Hz |
| | | $V_{BAT}$ = 2.4 V, $T_A$ = 25 °C, CPMD = 10 | — | 2.08 | — | nA/Hz |
| | | $V_{BAT}$ = 3.8 V, $T_A$ = 25 °C, CPMD = 10 | — | 2.59 | — | nA/Hz |
| | | $V_{BAT}$ = 2.4 V, $T_A$ = 25 °C, CPMD = 11 | — | 3.47 | — | nA/Hz |
| | | $V_{BAT}$ = 3.8 V, $T_A$ = 25 °C, CPMD = 11 | — | 4.03 | — | nA/Hz |
| **Analog Peripheral Supply Currents** | | | | | | |
| PLL0 Oscillator (PLL0OSC) | $I_{PLLOSC}$ | Operating at 49 MHz | — | 1.4 | 1.6 | mA |
| Low-Power Oscillator (LPOSC0) | $I_{LPOSC}$ | Operating at 20 MHz | — | 25 | — | µA |
| | | Operating at 2.5 MHz | — | 25 | — | µA |
| Low-Frequency Oscillator (LFOSC0) | $I_{LFOSC}$ | Operating at 16.4 kHz | — | 190 | 310 | nA |
| External Oscillator (EXTOSC0) | $I_{EXTOSC}$ | FREQCN = 111 | — | 3.8 | 4.5 | mA |
| | | FREQCN = 110 | — | 840 | 960 | µA |
| | | FREQCN = 101 | — | 185 | 230 | µA |
| | | FREQCN = 100 | — | 65 | 80 | µA |
| | | FREQCN = 011 | — | 25 | 30 | µA |
| | | FREQCN = 010 | — | 10 | 13 | µA |
| | | FREQCN = 001 | — | 5 | 7 | µA |
| | | FREQCN = 000 | — | 3 | 5 | µA |

**Notes:**

1. Currents are additive. For example, where $I_{BAT}$ is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded $I_{VIO}$ is included in all $I_{BAT}$ PM8 production test measurements.

**Table 3.2. Power Consumption (Continued)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SARADC0 | $I_{SARADC}$ | Sampling at 1 Msps, Internal VREF used | — | 1.2 | 1.6 | mA |
| | | Sampling at 250 ksps, lowest power mode settings. | — | 390 | 540 | µA |
| Temperature Sensor | $I_{TSENSE}$ | | — | 75 | 110 | µA |
| Internal SAR Reference | $I_{REFFS}$ | Normal Power Mode | — | 680 | — | µA |
| | | Normal Power Mode | — | 160 | — | µA |
| VREF0 | $I_{REFP}$ | | — | 80 | — | µA |
| Comparator 0 (CMP0), Comparator 1 (CMP1) | $I_{CMP}$ | CMPMD = 11 | — | 0.5 | 2 | µA |
| | | CMPMD = 10 | — | 3 | 8 | µA |
| | | CMPMD = 01 | — | 10 | 16 | µA |
| | | CMPMD = 00 | — | 25 | 42 | µA |
| IDAC0[8] | $I_{IDAC}$ | | — | 70 | 100 | µA |
| Voltage Supply Monitor (VMON0) | $I_{VMON}$ | | — | 10 | 22 | µA |
| **Flash Current on VBAT** | | | | | | |
| Write Operation | $I_{FLASH-W}$ | | — | — | 8 | mA |
| Erase Operation | $I_{FLASH-E}$ | | — | — | 15 | mA |

**Notes:**

1. Currents are additive. For example, where $I_{BAT}$ is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded $I_{VIO}$ is included in all $I_{BAT}$ PM8 production test measurements.

**Table 3.7. Internal Oscillators (Continued)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **RTC0 Oscillator (RTC0OSC)** | | | | | | |
| Missing Clock Detector Trigger Frequency | $f_{RTCMCD}$ | | — | 8 | 15 | kHz |
| RTC External Input CMOS Clock Frequency | $f_{RTCEXTCLK}$ | | 0 | — | 40 | kHz |
| RTC Robust Duty Cycle Range | $DC_{RTC}$ | | 25 | — | 55 | % |

**Table 3.8. External Oscillator**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| External Input CMOS Clock Frequency | $f_{CMOS}$ | | 0* | — | 50 | MHz |
| External Crystal Frequency | $f_{XTAL}$ | | 0.01 | — | 25 | MHz |
| External Input CMOS Clock High Time | $t_{CMOSH}$ | | 9 | — | — | ns |
| External Input CMOS Clock Low Time | $t_{CMOSL}$ | | 9 | — | — | ns |
| Low Power Mode Charge Pump Supply Range (input from $V_{BAT}$) | $V_{BAT}$ | | 2.4 | — | 3.8 | V |
| ***Note:** Minimum of 10 kHz when debugging. | | | | | | |

**Table 3.9. SAR ADC**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Resolution | $N_{bits}$ | 12 Bit Mode | | 12 | | Bits |
| | | 10 Bit Mode | | 10 | | Bits |
| Supply Voltage Requirements (VBAT) | $V_{ADC}$ | High Speed Mode | 2.2 | — | 3.8 | V |
| | | Low Power Mode | 1.8 | — | 3.8 | V |
| Throughput Rate (High Speed Mode) | $f_S$ | 12 Bit Mode | — | — | 250 | ksps |
| | | 10 Bit Mode | — | — | 1 | Msps |
| Throughput Rate (Low Power Mode) | $f_S$ | 12 Bit Mode | — | — | 62.5 | ksps |
| | | 10 Bit Mode | — | — | 250 | ksps |
| Tracking Time | $t_{TRK}$ | High Speed Mode | 230 | — | — | ns |
| | | Low Power Mode | 450 | — | — | ns |
| SAR Clock Frequency | $f_{SAR}$ | High Speed Mode | — | — | 16.24 | MHz |
| | | Low Power Mode | — | — | 4 | MHz |
| Conversion Time | $t_{CNV}$ | 10-Bit Conversion, SAR Clock = 16 MHz, APB Clock = 40 MHz | | 762.5 | | ns |
| Sample/Hold Capacitor | $C_{SAR}$ | Gain = 1 | — | 5 | — | pF |
| | | Gain = 0.5 | — | 2.5 | — | pF |
| Input Pin Capacitance | $C_{IN}$ | High Quality Inputs | — | 18 | — | pF |
| | | Normal Inputs | — | 20 | — | pF |
| Input Mux Impedance | $R_{MUX}$ | High Quality Inputs | — | 300 | — | Ω |
| | | Normal Inputs | — | 550 | — | Ω |
| Voltage Reference Range | $V_{REF}$ | | 1 | — | $V_{BAT}$ | V |
| Input Voltage Range* | $V_{IN}$ | Gain = 1 | 0 | — | $V_{REF}$ | V |
| | | Gain = 0.5 | 0 | — | $2xV_{REF}$ | V |
| Power Supply Rejection Ratio | $PSRR_{ADC}$ | | — | 70 | — | dB |
| **DC Performance** | | | | | | |
| Integral Nonlinearity | INL | 12 Bit Mode | — | ±1 | ±1.9 | LSB |
| | | 10 Bit Mode | — | ±0.2 | ±0.5 | LSB |
| Differential Nonlinearity (Guaranteed Monotonic) | DNL | 12 Bit Mode | –1 | ±0.7 | 1.8 | LSB |
| | | 10 Bit Mode | — | ±0.2 | ±0.5 | LSB |
| Offset Error (using VREFGND) | $E_{OFF}$ | 12 Bit Mode, VREF = 2.4 V | –2 | 0 | 2 | LSB |
| | | 10 Bit Mode, VREF = 2.4 V | –1 | 0 | 1 | LSB |

### Table 3.12. Voltage Reference Electrical Characteristics

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Internal Fast Settling Reference** | | | | | | |
| Output Voltage | $V_{REFFS}$ | –40 to +85 °C, $V_{BAT}$ = 1.8–3.8 V | 1.6 | 1.65 | 1.7 | V |
| Temperature Coefficient | $TC_{REFFS}$ | | — | 50 | — | ppm/°C |
| Turn-on Time | $t_{REFFS}$ | | — | — | 1.5 | µs |
| Power Supply Rejection | $PSRR_{REFFS}$ | | — | 400 | — | ppm/V |
| **Internal Precision Reference** | | | | | | |
| Valid Supply Range | $V_{BAT}$ | VREF2X = 0 | 1.8 | — | 3.8 | V |
| | | VREF2X = 1 | 2.7 | — | 3.8 | V |
| Output Voltage | $V_{REFP}$ | 25 °C ambient, VREF2X = 0 | 1.17 | 1.2 | 1.23 | V |
| | | 25 °C ambient, VREF2X = 1 | 2.35 | 2.4 | 2.45 | V |
| Short-Circuit Current | $I_{SC}$ | | — | — | 10 | mA |
| Temperature Coefficient | $TC_{VREFP}$ | | — | 35 | — | ppm/°C |
| Load Regulation | $LR_{VREFP}$ | Load = 0 to 200 µA to VREFGND | — | 4.5 | — | ppm/µA |
| Load Capacitor | $C_{VREFP}$ | Load = 0 to 200 µA to VREFGND | 0.1 | — | — | µF |
| Turn-on Time | $t_{VREFPON}$ | 4.7 µF tantalum, 0.1 µF ceramic bypass | — | 3.8 | — | ms |
| | | 0.1 µF ceramic bypass | — | 200 | — | µs |
| Power Supply Rejection | $PSRR_{VREFP}$ | VREF2X = 0 | — | 320 | — | ppm/V |
| | | VREF2X = 1 | — | 560 | — | ppm/V |
| **External Reference** | | | | | | |
| Input Current | $I_{EXTREF}$ | Sample Rate = 250 ksps; VREF = 3.0 V | — | 5.25 | — | µA |

### Table 3.13. Temperature Sensor

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Offset | $V_{OFF}$ | $T_A$ = 0 °C | — | 760 | — | mV |
| Offset Error* | $E_{OFF}$ | $T_A$ = 0 °C | — | ±14 | — | mV |
| Slope | M | | — | 2.77 | — | mV/°C |
| Slope Error* | $E_M$ | | — | ±25 | — | µV/°C |
| Linearity | | | — | 1 | — | °C |
| Turn-on Time | | | — | 1.8 | — | µs |

***Note:** Absolute input pin voltage is limited by the lower of the supply at VBAT and VIO.

**Table 3.16. Port I/O**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output High Voltage (PB0, PB1, PB3, or PB4) | $V_{OH}$ | Low Drive, $I_{OH}$ = –1 mA | $V_{IO}$ – 0.7 | — | — | V |
| | | Low Drive, $I_{OH}$ = –10 µA | $V_{IO}$ – 0.1 | — | — | V |
| | | High Drive, $I_{OH}$ = –3 mA | $V_{IO}$ – 0.7 | — | — | V |
| | | High Drive, $I_{OH}$ = –10 µA | $V_{IO}$ – 0.1 | — | — | V |
| Output High Voltage (PB2) | $V_{OH}$ | Low Drive, $I_{OH}$ = –1 mA | $V_{IORF}$ – 0.7 | — | — | V |
| | | Low Drive, $I_{OH}$ = –10 µA | $V_{IORF}$ – 0.1 | — | — | V |
| | | High Drive, $I_{OH}$ = –3 mA | $V_{IORF}$ – 0.7 | — | — | V |
| | | High Drive, $I_{OH}$ = –10 µA | $V_{IORF}$ – 0.1 | — | — | V |
| Output Low Voltage (any Port I/O pin or $\overline{\text{RESET}}$[1]) | $V_{OL}$ | Low Drive, $I_{OL}$ = 1.4 mA | — | — | 0.6 | V |
| | | Low Drive, $I_{OL}$ = 10 µA | — | — | 0.1 | V |
| | | High Drive, $I_{OL}$ = 8.5 mA | — | — | 0.6 | V |
| | | High Drive, $I_{OL}$ = 10 µA | — | — | 0.1 | V |
| Input High Voltage (PB0, PB1, PB3, PB4 or $\overline{\text{RESET}}$) | $V_{IH}$ | | $V_{IO}$ – 0.6 | — | — | V |
| Input High Voltage (PB2) | $V_{IH}$ | | $V_{IORF}$ – 0.6 | — | — | V |
| Input Low Voltage any Port I/O pin or $\overline{\text{RESET}}$) | $V_{IL}$ | | — | — | 0.6 | V |
| Weak Pull-Up Current[2] (per pin) | $I_{PU}$ | $V_{IO}$ or $V_{IORF}$ = 1.8 | -6 | -3.5 | -2 | µA |
| | | $V_{IO}$ or $V_{IORF}$ = 3.8 | -32 | -20 | -10 | µA |
| Input Leakage (Pullups off or Analog) | $I_{LK}$ | $0 \le V_{IN} \le V_{IO}$ or $V_{IORF}$ | -1 | — | 1 | µA |

**Notes:**

1. Specifications for $\overline{\text{RESET}}$ $V_{OL}$ adhere to the low drive setting.
2. On the SiM3L1x6 and SiM3L1x4 devices, the SWV pin will have double the weak pull-up current specified whenever the device is held in reset.

## 3.2. Thermal Conditions

### Table 3.17. Thermal Conditions

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Thermal Resistance* | $\theta_{JA}$ | TQFP-80 Packages | — | 40 | — | °C/W |
| | | QFN-64 Packages | — | 25 | — | °C/W |
| | | TQFP-64 Packages | — | 30 | — | °C/W |
| | | QFN-40 Packages | — | 30 | — | °C/W |
| ***Note:** Thermal resistance assumes a multi-layer PCB with the exposed pad soldered to a topside PCB pad. | | | | | | |

## 3.3. Absolute Maximum Ratings

Stresses above those listed under Table 3.18 may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 3.18. Absolute Maximum Ratings**

| Parameter | Symbol | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Ambient Temperature Under Bias | $T_{BIAS}$ | | –55 | 125 | °C |
| Storage Temperature | $T_{STG}$ | | –65 | 150 | °C |
| Voltage on VBAT/VBATDC | $V_{BAT}$ | | $V_{SS}$–0.3 | 4.2 | V |
| Voltage on VDC | $V_{DC}$ | | $V_{SSDC}$–0.3 | 4.2 | V |
| Voltage on VDRV | $V_{DRV}$ | | $V_{SS}$–0.3 | 4.2 | V |
| Voltage on VIO | $V_{IO}$ | | $V_{SS}$–0.3 | 4.2 | V |
| Voltage on VIORF | $V_{IORF}$ | | $V_{SS}$–0.3 | 4.2 | V |
| Voltage on VLCD | $V_{LCD}$ | | $V_{SS}$–0.3 | 4.2 | V |
| Voltage on I/O (PB0, PB1, PB3, PB4) or $\overline{\text{RESET}}$[1] | $V_{IN}$ | $V_{IO} \geq 3.3$ V | $V_{SS}$–0.3 | 5.8 | V |
| | | $V_{IO} < 3.3$ V | $V_{SS}$–0.3 | $V_{IO}$+2.5 | V |
| Voltage on PB2 I/O Pins[1] | $V_{IN}$ | $V_{IORF} \geq 3.3$ V | $V_{SS}$–0.3 | 5.8 | V |
| | | $V_{IORF} < 3.3$ V | $V_{SS}$–0.3 | $V_{IORF}$+2.5 | V |
| Total Current Sunk into Supply Pins | $I_{SUPP}$ | VBAT/VBATDC, VIO, VIORF, VDRV, VDC, VLCD | — | 400 | mA |
| Total Current Sourced out of Ground Pins[2] | $I_{VSS}$ | $V_{SS}$, $V_{SSDC}$ | 400 | — | mA |
| Current Sourced or Sunk by any I/O Pin | $I_{PIO}$ | All I/O and $\overline{\text{RESET}}$ | –100 | 100 | mA |
| Power Dissipation at $T_A$ = 85 °C | $P_D$ | TQFP-80 Packages | — | 500 | mW |
| | | QFN-64 Packages | — | 800 | mW |
| | | TQFP-64 Packages | — | 650 | mW |
| | | QFN-40 Packages | — | 650 | mW |

**Notes:**
1. Exceeding the minimum $V_{IO}$ voltage may cause current to flow through adjacent device pins.
2. VSS and VSSDC provide separate return current paths for device supplies, but are not isolated. They must always be connected to the same potential on board.

## 4.2. I/O

### 4.2.1. General Features

The SiM3L1xx ports have the following features:

- 5 V tolerant.
- Push-pull or open-drain output modes to the VIO or VIORF voltage level.
- Analog or digital modes.
- Option for high or low output drive strength.
- Port Match allows the device to recognize a change on a port pin value.
- Internal pull-up resistors are enabled or disabled on a port-by-port basis.
- Two external interrupts with up to 16 inputs each provide monitoring capability for external signals.
- Internal Pulse Generator Timer (PB0 only) to generate simple square waves and pulses.

### 4.2.2. Crossbar

The SiM3L1xx devices have one crossbar with the following features:

- Flexible peripheral assignment to port pins.
- Pins can be individually skipped to move peripherals as needed for design or layout considerations.

The crossbar has a fixed priority for each I/O function and assigns these functions to the port pins. When a digital resource is selected, the least-significant unassigned port pin is assigned to that resource. If a port pin is assigned, the crossbar skips that pin when assigning the next selected resource. Additionally, the crossbar will skip port pins whose associated bits in the PBSKIPEN registers are set. This provides flexibility when designing a system: pins involved with sensitive analog measurements can be moved away from digital I/O, and peripherals can be moved around the chip as needed to ease layout constraints.

### 4.5.4. 16/32-bit Enhanced CRC (ECRC0)

The ECRC module is designed to provide hardware calculations for flash memory verification and communications protocols. In addition to calculating a result from direct writes from firmware, the ECRC module can automatically snoop the APB bus and calculate a result from data written to or read from a particular peripheral. This allows for an automatic CRC result without directly feeding data through the ECRC module.

The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3). The 16-bit polynomial is fully programmable.

The ECRC module includes the following features:

- Support for a programmable 16-bit polynomial and one fixed 32-bit polynomial.
- Byte-level bit reversal for the CRC input.
- Byte-order reorientation of words for the CRC input.
- Word or half-word bit reversal of the CRC result.
- Ability to configure and seed an operation in a single register write.
- Support for single-cycle parallel (unrolled) CRC computation for 32-, 16-, or 8-bit blocks.
- Capability to CRC 32 bits of data per peripheral bus (APB) clock.
- Automatic APB bus snooping.
- Support for DMA writes using firmware request mode.

### 4.5.5. Encoder / Decoder (ENCDEC0)

The encoder / decoder module supports Manchester and Three-out-of-Six encoding and decoding from either firmware or DMA operations.

This module has the following features:

- Supports Manchester and Three-out-of-Six encoding and decoding.
- Automatic flag clearing when writing the input or reading the output data registers.
- Writing to the input data register automatically initiates an encode or decode operation.
- Optional output in one’s complement format.
- Hardware error detection for invalid input data during decode operations, which helps reduce power consumption and packet turn-around time.
- Flexible byte swapping on the input or output data.

### 4.6.3. Real-Time Clock (RTC0)

The RTC module includes a 32-bit timer that allows up to 36 hours of independent time-keeping when used with a 32.768 kHz watch crystal. The RTC provides three alarm events in addition to a missing clock event, which can also function as interrupt, reset, or wakeup sources on SiM3L1xx devices.

The RTC module includes internal loading capacitors that are programmable to 16 discrete levels, allowing compatibility with a wide range of crystals.

The RTC timer clock can be buffered and routed to a port bank pin to provide an accurate, low frequency clock to other devices while the core is in its lowest power down mode. The module also includes a low power internal low frequency oscillator that reduces low power mode current and is available for other modules to use as a clock source.

The RTC module includes the following features:

- 32-bit timer (supports up to 36 hours) with three separate alarms.
- Option for one alarm to automatically reset the RTC timer.
- Missing clock detector.
- Can be used with the internal Low Frequency Oscillator or with an external 32.768 kHz crystal (no additional resistors or capacitors necessary).
- Programmable internal loading capacitors support a wide range of external 32.768 kHz crystals.
- The RTC timer clock (RTC0CLK) can be buffered and routed to an I/O pin to provide an accurate, low frequency clock to other devices while the core is in its lowest power down mode.
- The RTC module can be powered from the low power mode charge pump for lowest possible power consumption while in PM8.

### 4.6.4. Low Power Timer (LPTIMER0)

The Low Power Timer (LPTIMER) module runs from the RTC timer clock (RTC0CLK), allowing the LPTIMER to operate even if the AHB and APB clocks are disabled. The LPTIMER counter can increment using one of two clock sources: the clock selected by the RTC0 module, or rising or falling edges of an external signal.

The Low Power Timer includes the following features:

- Runs on low-frequency RTC timer clock (RTC0TCLK).
- The LPTIMER counter can increment using one of two clock sources: the RTC0TCLK or rising or falling edges of an external signal.
- Overflow and threshold-match detection.
- Timer reset on threshold-match allows square-wave generation at a variable output frequency.
- Supports PWM with configurable period and duty cycle.
- The LPTIMER module can be powered from the low power mode charge pump for lowest possible power consumption while in PM8.

### 4.6.5. Watchdog Timer (WDTIMER0)

The WDTIMER module includes a 16-bit timer, a programmable early warning interrupt, and a programmable reset period. The timer registers are protected from inadvertent access by an independent lock and key interface.

The watchdog timer runs from the low frequency oscillator (LFOSC0).

The Watchdog Timer has the following features:

- Programmable timeout interval.
- Optional interrupt to warn when the Watchdog Timer is nearing the reset trip value.
- Lock-out feature to prevent any modification until a system reset.

## 4.10. Security

The peripherals on the SiM3L1xx devices have a register lock and key mechanism that prevents undesired accesses of the peripherals from firmware. Each bit in the PERIPHLOCKx registers controls a set of peripherals. A key sequence must be written to the KEY register to modify bits in PERIPHLOCKx. Any subsequent write to KEY will then inhibit accesses of PERIPHLOCKx until it is unlocked again through KEY. Reading the KEY register indicates the current status of the PERIPHLOCKx lock state.

If a peripheral's registers are locked, all writes will be ignored. The registers can be read, regardless of the peripheral's lock state.

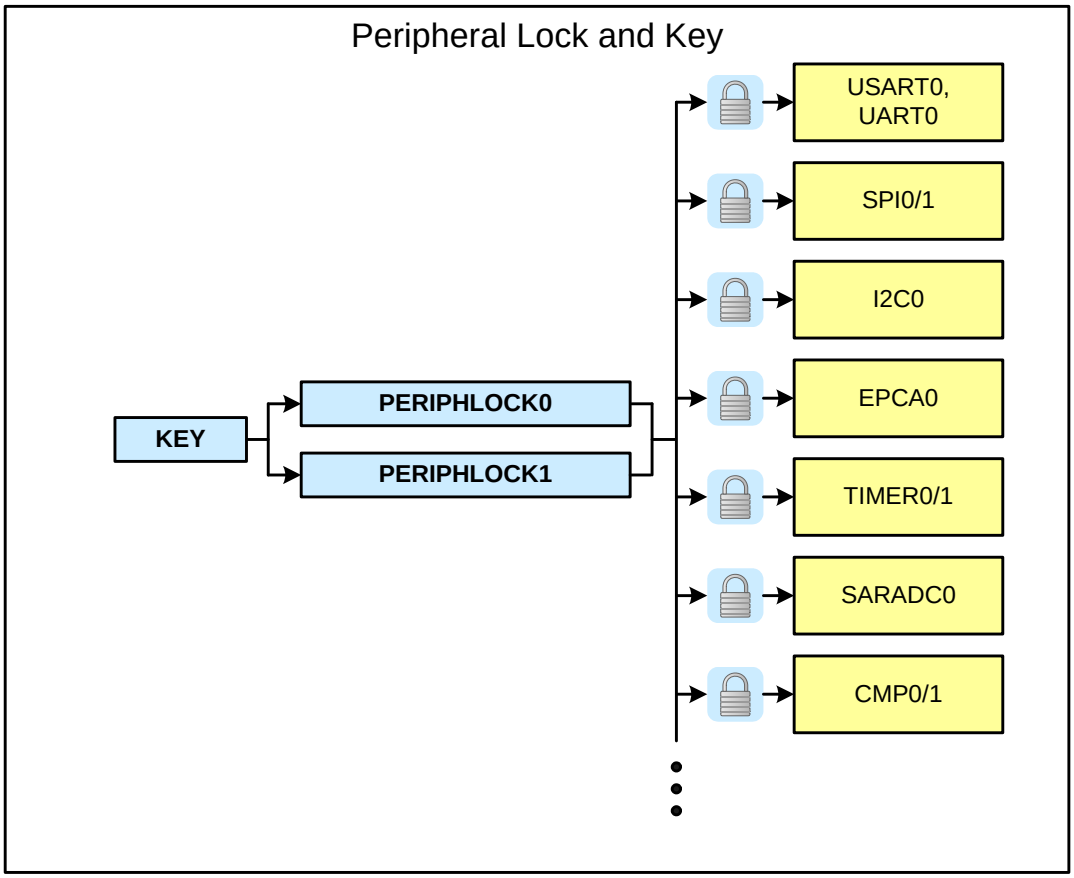



**Figure 4.5. SiM3L1xx Security Block Diagram**

## 4.11. On-Chip Debugging

The SiM3L1xx devices include JTAG and Serial Wire programming and debugging interfaces and ETM for instruction trace. The JTAG interface is supported on SiM3L1x7 devices only, and does not include boundary scan capabilites. The ETM interface is supported on SiM3L1x7, and SiM3L1x6 devices only. The JTAG and ETM interfaces can be optionally enabled to provide more visibility while debugging at the cost of using several Port I/O pins. Additionally, if the core is configured for Serial Wire (SW) mode and not JTAG, then the Serial Wire Viewer (SWV) is available to provide a single pin to send out TPIU messages. Serial Wire Viewer is supported on all SiM3Lxxx devices.

Most peripherals on SiM3L1xx devices have the option to halt or continue functioning when the core halts in debug mode.

**Table 6.1. Pin Definitions and Alternate Functions for SiM3L1x7 (Continued)**

| Pin Name | Type | Pin Numbers (TQFP-80) | I/O Voltage Domain | Crossbar Capability | Port Match | LCD Interface | Output Toggle Logic | External Trigger Inputs / Digital Functions | Analog Functions |
|---|---|---|---|---|---|---|---|---|---|
| PB3.4 | Standard I/O | 43 | VIO | ✓ | ✓ | LCD0.23 | | INT1.12 | CMP0P.6 |
| PB3.5 | Standard I/O | 42 | VIO | ✓ | ✓ | LCD0.22 | | INT1.13 | CMP0N.6 |
| PB3.6 | Standard I/O | 41 | VIO | ✓ | ✓ | LCD0.21 | | INT1.14 | CMP1P.6 |
| PB3.7 | Standard I/O | 40 | VIO | ✓ | ✓ | LCD0.20 | | INT1.15 | CMP1N.6 |
| PB3.8 | Standard I/O | 39 | VIO | | ✓ | LCD0.19 | | | CMP0P.7 |
| PB3.9 | Standard I/O | 38 | VIO | | ✓ | LCD0.18 | | | CMP0N.7 |
| PB3.10 | Standard I/O | 37 | VIO | | ✓ | LCD0.17 | | | CMP1P.7 |
| PB3.11 | Standard I/O | 36 | VIO | | ✓ | LCD0.16 | | | CMP1N.7 |
| PB3.12 | Standard I/O | 35 | VIO | | ✓ | LCD0.15 | | | ADC0.18 |
| PB3.13 | Standard I/O | 34 | VIO | | ✓ | LCD0.14 | | | ADC0.19 |
| PB3.14 | Standard I/O | 33 | VIO | | ✓ | COM0.3 | | | |
| PB3.15 | Standard I/O | 32 | VIO | | ✓ | COM0.2 | | | |
| PB4.0 | Standard I/O | 29 | VIO | | ✓ | COM0.1 | | | |
| PB4.1 | Standard I/O | 28 | VIO | | ✓ | COM0.0 | | | |
| PB4.2 | Standard I/O | 27 | VIO | | ✓ | LCD0.13 | | | |
| PB4.3 | Standard I/O | 26 | VIO | | ✓ | LCD0.12 | | | |
| PB4.4 | Standard I/O | 25 | VIO | | ✓ | LCD0.11 | | | |
| PB4.5 | Standard I/O | 24 | VIO | | ✓ | LCD0.10 | | | |
| PB4.6 | Standard I/O | 23 | VIO | | ✓ | LCD0.9 | | PMU_Asleep | |
| PB4.7 | Standard I/O | 22 | VIO | | ✓ | LCD0.8 | | | |
| PB4.8 | Standard I/O | 21 | VIO | | ✓ | LCD0.7 | | | |

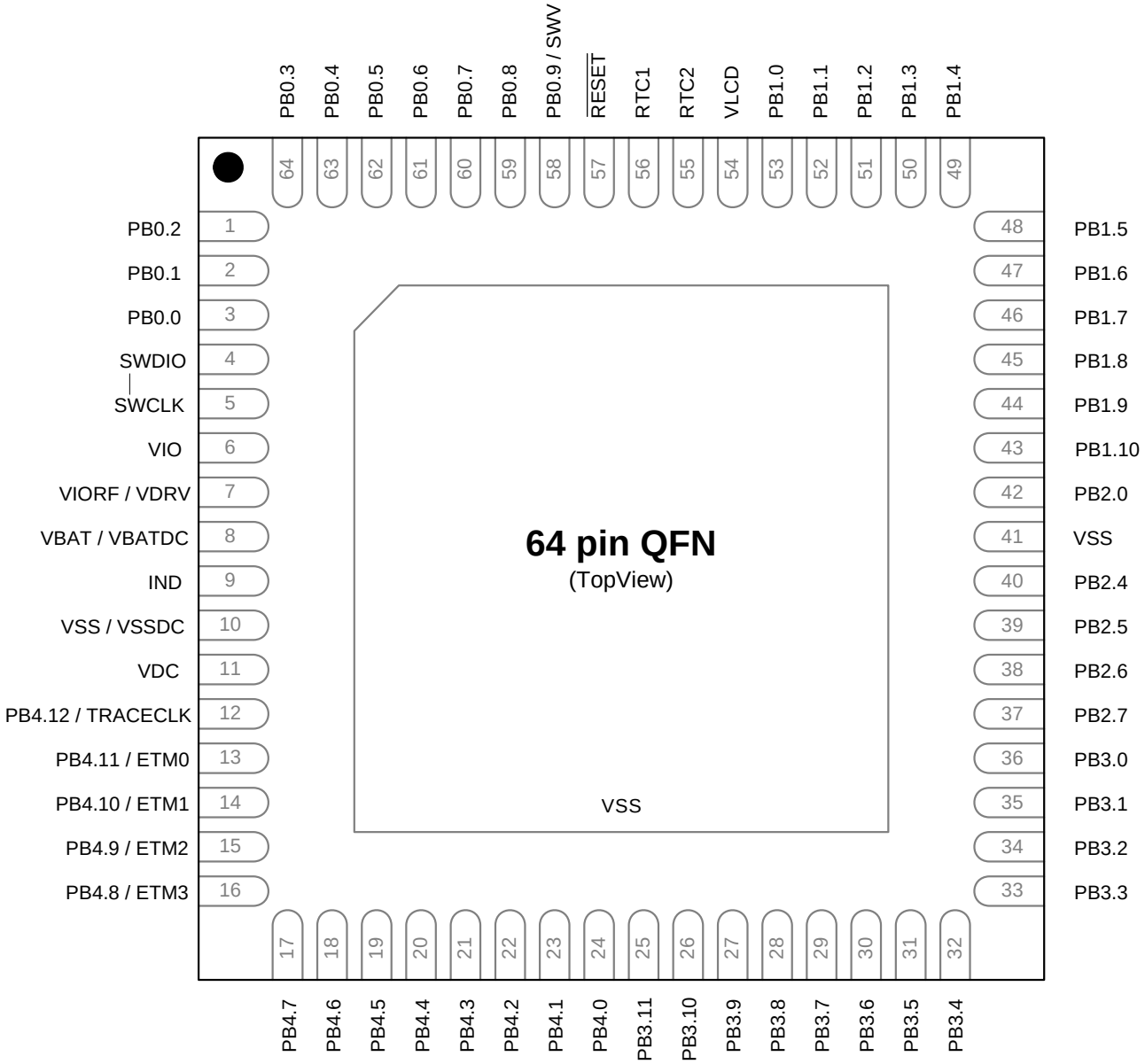



**Figure 6.3. SiM3L1x6-GM Pinout**

**Table 6.3. Pin Definitions and Alternate Functions for SiM3L1x4**

| Pin Name | Type | Pin Numbers | I/O Voltage Domain | Crossbar Capability | Port Match | Output Toggle Logic | External Trigger Inputs / Digital Functions | Analog Functions |
|---|---|---|---|---|---|---|---|---|
| VSS | Ground | 9<br>25 | | | | | | |
| VSSDC | Ground (DC-DC) | 9 | | | | | | |
| VIO | Power (I/O) | 5 | | | | | | |
| VIORF / VDRV | Power (RF I/O) | 6 | | | | | | |
| VBAT / VBATDC | | 7 | | | | | | |
| VDC | | 10 | | | | | | |
| IND | DC-DC Inductor | 8 | | | | | | |
| $\overline{\text{RESET}}$ | Active-low Reset | 35 | | | | | | |
| SWCLK | Serial Wire | 4 | | | | | | |
| SWDIO | Serial Wire | 3 | | | | | | |
| RTC1 | RTC Oscillator Input | 34 | | | | | | |
| RTC2 | RTC Oscillator Output | 33 | | | | | | |
| PB0.0 | Standard I/O | 2 | VIO | XBR0 | ✓ | ✓ | INT0.0<br>WAKE.0 | ADC0.20<br>VREF<br>CMP0P.0 |
| PB0.1 | Standard I/O | 1 | VIO | XBR0 | ✓ | ✓ | INT0.1<br>WAKE.2 | ADC0.22<br>CMP0N.0<br>CMP1P.0<br>XTAL2 |

**Table 6.4. TQFP-80 Package Dimensions**

| Dimension | Min | Nominal | Max |
|---|---|---|---|
| A | — | — | 1.20 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| b | 0.17 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| D | 14.00 BSC | | |
| D1 | 12.00 BSC | | |
| e | 0.50 BSC | | |
| E | 14.00 BSC | | |
| E1 | 12.00 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 Ref | | |
| Θ | 0° | 3.5° | 7° |
| aaa | 0.20 | | |
| bbb | 0.20 | | |
| ccc | 0.08 | | |
| ddd | 0.08 | | |
| eee | 0.05 | | |

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant ADD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

### 6.5.1. QFN-64 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

### 6.5.2. QFN-64 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 3x3 array of 1.0 mm square openings on a 1.5 mm pitch should be used for the center ground pad.

### 6.5.3. QFN-64 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 6.6. TQFP-64 Package Specifications

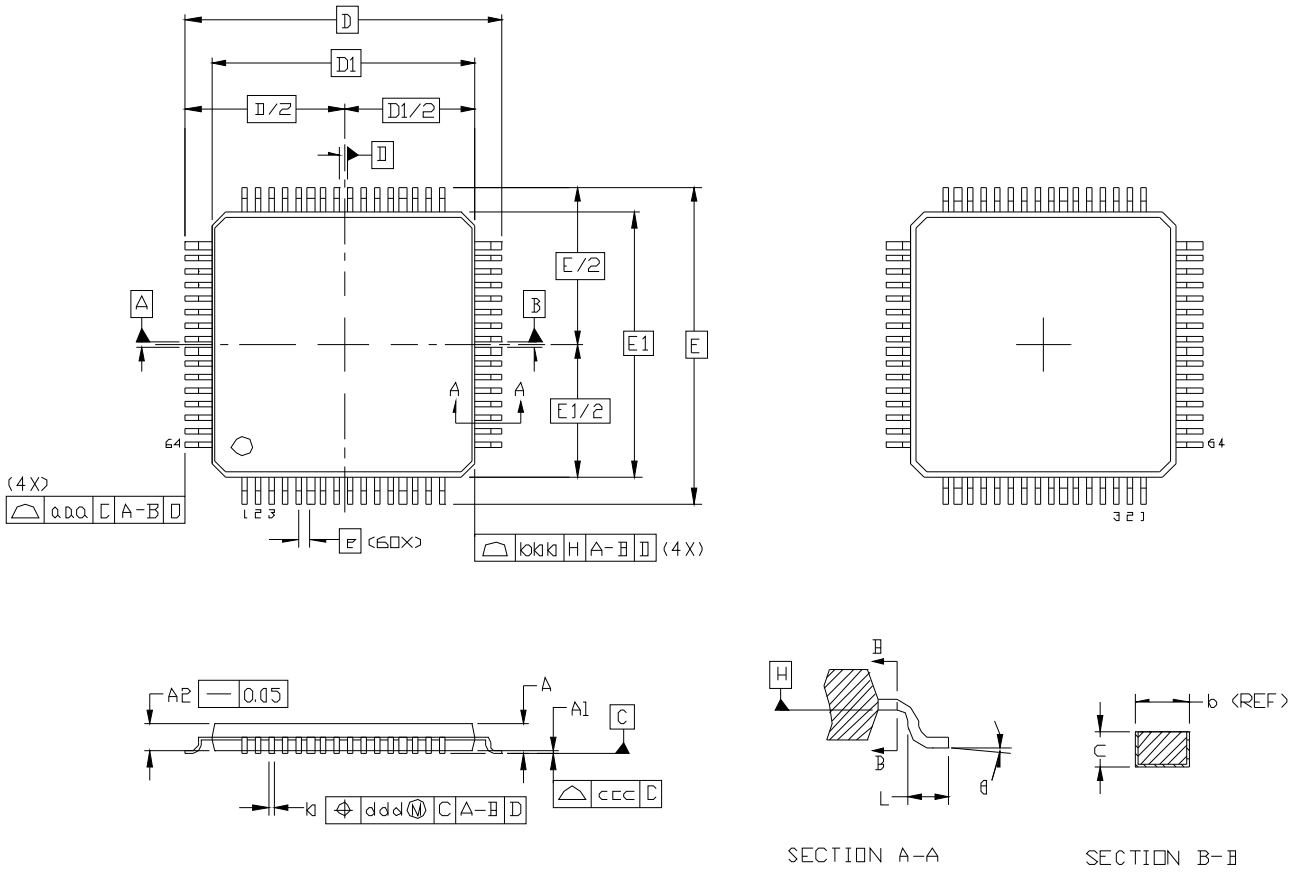
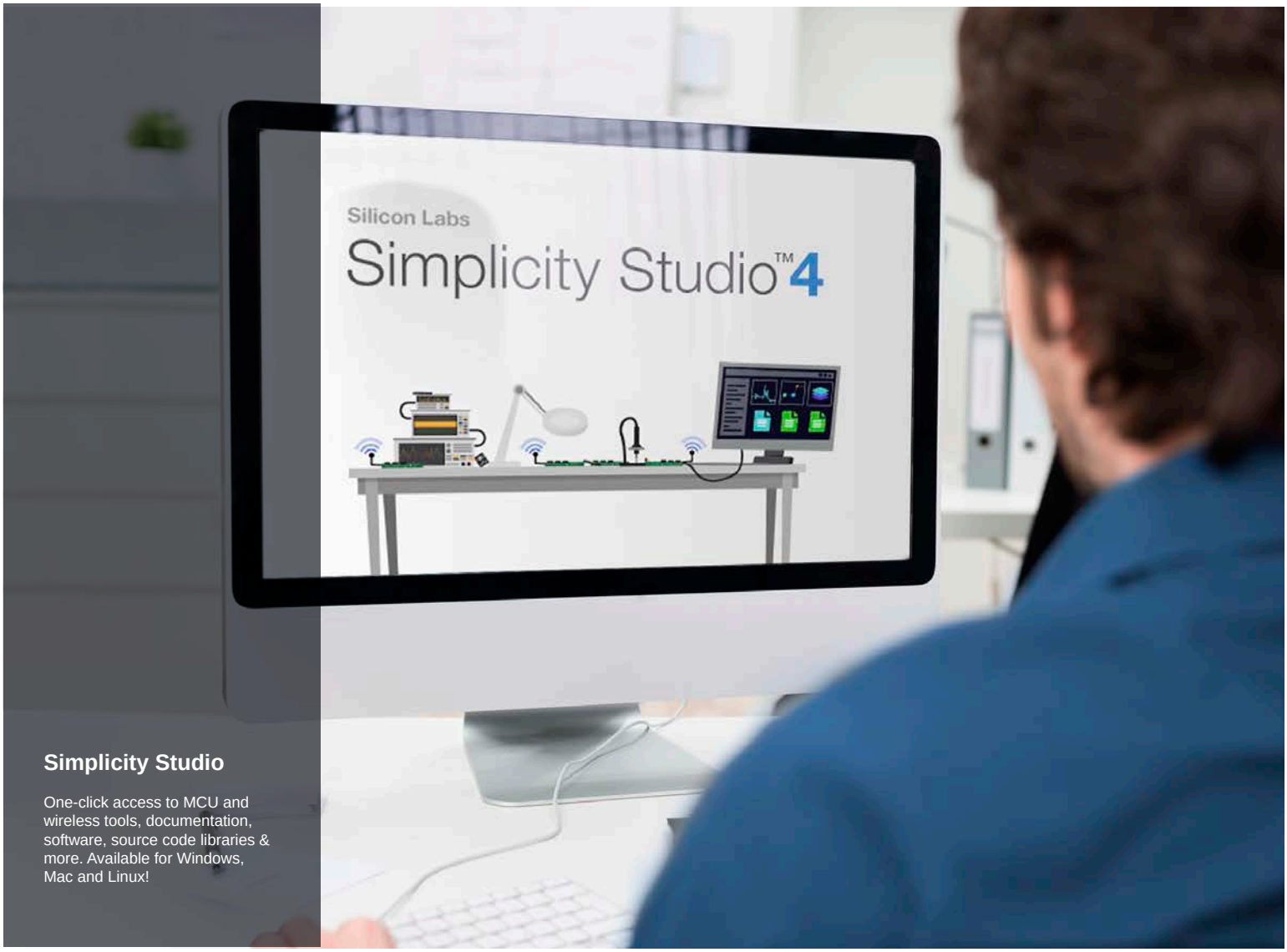



**Figure 6.9. TQFP-64 Package Drawing**

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