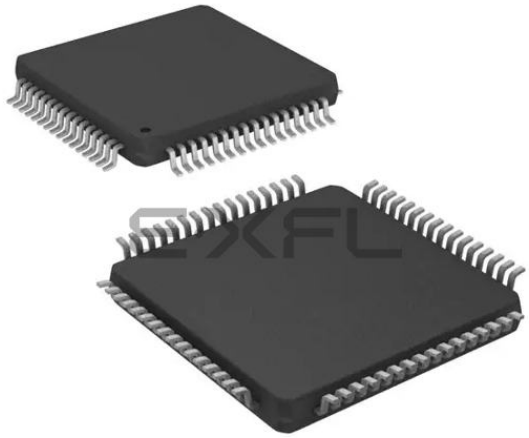

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Table 3.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current						
Normal Mode[1,2,3,4]—Full speed with code executing from flash, peripheral clocks ON	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	17.5	18.9	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	6.7	7.2	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	1.15	1.4	mA
Normal Mode[1,2,3,4]—Full speed with code executing from flash, peripheral clocks OFF	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	13.3	14.5	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	5.4	5.9	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	980	1.2	µA
Normal Mode[1,2,3,4]—Full speed with code executing from flash, LDOs powered by dc-dc at 1.9 V, peripheral clocks OFF	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz V_{BAT} = 3.3 V	—	9.7	—	mA
		F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz V_{BAT} = 3.8 V	—	8.65	—	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz V_{BAT} = 3.3 V	—	4.15	—	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz V_{BAT} = 3.8 V	—	3.9	—	mA

Notes:

1. Currents are additive. For example, where I_{BAT} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded I_{VIO} is included in all I_{BAT} PM8 production test measurements.

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 1[1,2,3,4]—Full speed with code executing from RAM, peripheral clocks ON	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	13.4	16.6	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	4.7	—	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	810	—	µA
Power Mode 1[1,2,3,4]—Full speed with code executing from RAM, peripheral clocks OFF	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	9.4	12.5	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	3.3	—	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	630	—	µA
Power Mode 1[1,2,3,4]—Full speed with code executing from RAM, LDOs powered by dc-dc at 1.9 V, peripheral clocks OFF	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz V_{BAT} = 3.3 V	—	7.05	—	mA
		F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz V_{BAT} = 3.8 V	—	6.3	—	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz V_{BAT} = 3.3 V	—	2.75	—	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz V_{BAT} = 3.8 V	—	2.6	—	mA
Power Mode 2[1,2,3,4,5]—Core halted with peripheral clocks ON	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	7.6	11.3	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	2.75	—	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	575	—	µA

Notes:

1. Currents are additive. For example, where I_{BAT} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded I_{VIO} is included in all I_{BAT} PM8 production test measurements.

Table 3.3. Power Mode Wake Up Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 2 or 6 Wake Time	t_{PM2}		4	—	5	clocks
Power Mode 3 Fast Wake Time (using LFO as clock source)	t_{PM3FW}		—	425	—	µs
Power Mode 8 Wake Time	t_{PM8}		—	3.8	—	µs

Notes:
1. Wake times are specified as the time from the wake source to the execution phase of the first instruction following WFI. This includes latency to recognize the wake event and fetch the first instruction (assuming wait states = 0).

Table 3.4. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{BAT} High Supply Monitor Threshold (VBATHITHEN = 1)	V_{VBATMH}	Early Warning	—	2.20	—	V
		Reset	1.95	2.05	2.1	V
V_{BAT} Low Supply Monitor Threshold (VBATHITHEN = 0)	V_{VBATML}	Early Warning	—	1.85	—	V
		Reset	1.70	1.75	1.77	V
Power-On Reset (POR) Threshold	V_{POR}	Rising Voltage on V_{BAT}	—	1.4	—	V
		Falling Voltage on V_{BAT}	0.8	1	1.3	V
V_{BAT} Ramp Time	t_{RMP}	Time to $V_{BAT} \geq 1.8$ V	10	—	3000	µs
Reset Delay from POR	t_{POR}	Relative to $V_{BAT} \geq V_{POR}$	3	—	100	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	10	—	µs
$\overline{\text{RESET}}$ Low Time to Generate Reset	t_{RSTL}		50	—	—	ns
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	$F_{AHB} > 1$ MHz	—	0.5	1.5	ms
Missing Clock Detector Trigger Frequency	F_{MCD}		—	2.5	10	kHz
V_{BAT} Supply Monitor Turn-On Time	t_{MON}		—	2	—	µs

Table 3.9. SAR ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}	12 Bit Mode		12		Bits
		10 Bit Mode		10		Bits
Supply Voltage Requirements (VBAT)	V_{ADC}	High Speed Mode	2.2	—	3.8	V
		Low Power Mode	1.8	—	3.8	V
Throughput Rate (High Speed Mode)	f_S	12 Bit Mode	—	—	250	ksps
		10 Bit Mode	—	—	1	Msps
Throughput Rate (Low Power Mode)	f_S	12 Bit Mode	—	—	62.5	ksps
		10 Bit Mode	—	—	250	ksps
Tracking Time	t_{TRK}	High Speed Mode	230	—	—	ns
		Low Power Mode	450	—	—	ns
SAR Clock Frequency	f_{SAR}	High Speed Mode	—	—	16.24	MHz
		Low Power Mode	—	—	4	MHz
Conversion Time	t_{CNV}	10-Bit Conversion, SAR Clock = 16 MHz, APB Clock = 40 MHz		762.5		ns
Sample/Hold Capacitor	C_{SAR}	Gain = 1	—	5	—	pF
		Gain = 0.5	—	2.5	—	pF
Input Pin Capacitance	C_{IN}	High Quality Inputs	—	18	—	pF
		Normal Inputs	—	20	—	pF
Input Mux Impedance	R_{MUX}	High Quality Inputs	—	300	—	Ω
		Normal Inputs	—	550	—	Ω
Voltage Reference Range	V_{REF}		1	—	V_{BAT}	V
Input Voltage Range*	V_{IN}	Gain = 1	0	—	V_{REF}	V
		Gain = 0.5	0	—	$2xV_{REF}$	V
Power Supply Rejection Ratio	$PSRR_{ADC}$		—	70	—	dB
DC Performance						
Integral Nonlinearity	INL	12 Bit Mode	—	±1	±1.9	LSB
		10 Bit Mode	—	±0.2	±0.5	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL	12 Bit Mode	–1	±0.7	1.8	LSB
		10 Bit Mode	—	±0.2	±0.5	LSB
Offset Error (using VREFGND)	E_{OFF}	12 Bit Mode, VREF = 2.4 V	–2	0	2	LSB
		10 Bit Mode, VREF = 2.4 V	–1	0	1	LSB

Table 3.10. IDAC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static Performance						
Resolution	N_{bits}			10		Bits
Integral Nonlinearity	INL		—	±0.5	±2	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL		—	±0.5	±1	LSB
Output Compliance Range	V_{OCR}		—	—	V_{BAT} – 1.0	V
Full Scale Output Current	I_{OUT}	2 mA Range, T_A = 25 °C	1.98	2.046	2.1	mA
		1 mA Range, T_A = 25 °C	0.99	1.023	1.05	mA
		0.5 mA Range, T_A = 25 °C	491	511.5	525	µA
Offset Error	E_{OFF}		—	250	—	nA
Full Scale Error Tempco	TC_{FS}	2 mA Range	—	100	—	ppm/°C
VBAT Power Supply Rejection Ratio		2 mA Range	—	–220	—	ppm/V
Test Load Impedance (to V_{SS})	R_{TEST}		—	1	—	kΩ
Dynamic Performance						
Output Settling Time to 1/2 LSB		min output to max output	—	1.2	—	µs
Startup Time			—	3	—	µs

Table 3.11. ACCTR (Advanced Capture Counter)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LC Comparator Response Time, CMPMD = 11 (Highest Speed)	t_{RESP0}	+100 mV Differential	—	100	—	ns
		–100 mV Differential	—	150	—	ns
LC Comparator Response Time, CMPMD = 00 (Lowest Power)	t_{RESP3}	+100 mV Differential	—	1.4	—	µs
		–100 mV Differential	—	3.5	—	µs
LC Comparator Positive Hysteresis Mode 0 (CPMD = 11)	HYS_{CP+}	CMPHYP = 00	—	0.37	—	mV
		CMPHYP = 01	—	7.9	—	mV
		CMPHYP = 10	—	16.7	—	mV
		CMPHYP = 11	—	32.8	—	mV
LC Comparator Negative Hysteresis Mode 0 (CPMD = 11)	HYS_{CP-}	CMPHYN = 00	—	0.37	—	mV
		CMPHYN = 01	—	–7.9	—	mV
		CMPHYN = 10	—	–16.1	—	mV
		CMPHYN = 11	—	–32.7	—	mV
LC Comparator Positive Hysteresis Mode 1 (CPMD = 10)	HYS_{CP+}	CMPHYP = 00	—	0.47	—	mV
		CMPHYP = 01	—	5.85	—	mV
		CMPHYP = 10	—	12	—	mV
		CMPHYP = 11	—	24.4	—	mV
LC Comparator Negative Hysteresis Mode 1 (CPMD = 10)	HYS_{CP-}	CMPHYN = 00	—	0.47	—	mV
		CMPHYN = 01	—	–6.0	—	mV
		CMPHYN = 10	—	–12.1	—	mV
		CMPHYN = 11	—	–24.6	—	mV
LC Comparator Positive Hysteresis Mode 2 (CPMD = 01)	HYS_{CP+}	CMPHYP = 00	—	0.66	—	mV
		CMPHYP = 01	—	4.55	—	mV
		CMPHYP = 10	—	9.3	—	mV
		CMPHYP = 11	—	19	—	mV
LC Comparator Negative Hysteresis Mode 2 (CPMD = 01)	HYS_{CP-}	CMPHYN = 00	—	0.6	—	mV
		CMPHYN = 01	—	–4.5	—	mV
		CMPHYN = 10	—	–9.5	—	mV
		CMPHYN = 11	—	–19	—	mV

Table 3.14. Comparator (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CMPHYP = 00	—	1.37	—	mV
		CMPHYP = 01	—	3.8	—	mV
		CMPHYP = 10	—	7.8	—	mV
		CMPHYP = 11	—	15.6	—	mV
Negative Hysteresis Mode 3 (CPMD = 11)	HYS_{CP-}	CMPHYN = 00	—	1.37	—	mV
		CMPHYN = 01	—	–3.9	—	mV
		CMPHYN = 10	—	–7.9	—	mV
		CMPHYN = 11	—	–16	—	mV
Input Range (CP+ or CP–)	V_{IN}		–0.25	—	V_{BAT} + 0.25	V
Input Pin Capacitance	C_{CP}		—	7.5	—	pF
Common-Mode Rejection Ratio	$CMRR_{CP}$		—	75	—	dB
Power Supply Rejection Ratio	$PSRR_{CP}$		—	72	—	dB
Input Offset Voltage	V_{OFF}	T_A = 25 °C	–10	0	10	mV
Input Offset Tempco	TC_{OFF}		—	3.5	—	µV/°C
Reference DAC Resolution	N_{Bits}			6		bits

Table 3.15. LCD0

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Charge Pump Output Voltage Error	V_{CPERR}		—	±50	—	mV
LCD Clock Frequency	F_{LCD}		16	—	33	kHz

Table 3.16. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (PB0, PB1, PB3, or PB4)	V_{OH}	Low Drive, I_{OH} = –1 mA	V_{IO} – 0.7	—	—	V
		Low Drive, I_{OH} = –10 µA	V_{IO} – 0.1	—	—	V
		High Drive, I_{OH} = –3 mA	V_{IO} – 0.7	—	—	V
		High Drive, I_{OH} = –10 µA	V_{IO} – 0.1	—	—	V
Output High Voltage (PB2)	V_{OH}	Low Drive, I_{OH} = –1 mA	V_{IORF} – 0.7	—	—	V
		Low Drive, I_{OH} = –10 µA	V_{IORF} – 0.1	—	—	V
		High Drive, I_{OH} = –3 mA	V_{IORF} – 0.7	—	—	V
		High Drive, I_{OH} = –10 µA	V_{IORF} – 0.1	—	—	V
Output Low Voltage (any Port I/O pin or $\overline{\text{RESET}}$[1])	V_{OL}	Low Drive, I_{OL} = 1.4 mA	—	—	0.6	V
		Low Drive, I_{OL} = 10 µA	—	—	0.1	V
		High Drive, I_{OL} = 8.5 mA	—	—	0.6	V
		High Drive, I_{OL} = 10 µA	—	—	0.1	V
Input High Voltage (PB0, PB1, PB3, PB4 or $\overline{\text{RESET}}$)	V_{IH}		V_{IO} – 0.6	—	—	V
Input High Voltage (PB2)	V_{IH}		V_{IORF} – 0.6	—	—	V
Input Low Voltage any Port I/O pin or $\overline{\text{RESET}}$)	V_{IL}		—	—	0.6	V
Weak Pull-Up Current[2] (per pin)	I_{PU}	V_{IO} or V_{IORF} = 1.8	-6	-3.5	-2	µA
		V_{IO} or V_{IORF} = 3.8	-32	-20	-10	µA
Input Leakage (Pullups off or Analog)	I_{LK}	$0 \le V_{IN} \le V_{IO}$ or V_{IORF}	-1	—	1	µA

Notes:

1. Specifications for $\overline{\text{RESET}}$ V_{OL} adhere to the low drive setting.
2. On the SiM3L1x6 and SiM3L1x4 devices, the SWV pin will have double the weak pull-up current specified whenever the device is held in reset.

4.1.5.6. Power Mode Summary

The power modes described above are summarized in Table 4.1. Table 3.2 and Table 3.3 provide more information on the power consumption and wake up times for each mode.

Table 4.1. SiM3L1xx Power Modes

Mode	Description	Notes
Normal	■ Core operating at full speed ■ Code executing from flash	■ Full device operation
Power Mode 1 (PM1)	■ Core operating at full speed ■ Code executing from RAM	■ Full device operation ■ Higher CPU bandwidth than PM0 (RAM can operate with zero wait states at any frequency)
Power Mode 2 (PM2)	■ Core halted ■ AHB, APB and all peripherals operational at full speed	■ Fast wakeup from any interrupt source
Power Mode 3 (PM3)	■ All clocks to core and peripherals stopped ■ Faster wake enabled by keeping LFOSC0 or RTC0TCLK active	■ Wake on any wake source or reset source defined in the PMU
Power Mode 4 (PM4)	■ Core operating at low speed ■ Code executing from flash	■ Same capabilities as PM0, operating at lower speed ■ Lower clock speed enables lower LDO output settings to save power
Power Mode 5 (PM5)	■ Core operating at low speed ■ Code executing from RAM	■ Same capabilities as PM1, operating at lower speed ■ Lower clock speed enables lower LDO output settings to save power
Power Mode 6 (PM6)	■ Core halted ■ AHB, APB and all peripherals operational at low speed	■ Same capabilities as PM2, operating at lower speed ■ Lower clock speed enables lower LDO output settings to save power ■ When running from LFOSC0, power is similar to PM3, but the device wakes much faster
Power Mode 8 (PM8)	■ Low power sleep ■ LDO regulators are disabled and all active circuitry operates directly from VBAT ■ The following functions are available: ACCTR0, RTC0, UART0 running from RTC0TCLK, LPTIMER0, port match, and the LCD controller ■ Register and RAM state retention	■ Lowest power consumption ■ Wake on any wake source or reset source defined in the PMU

4.4. Integrated LCD Controller (LCD0)

SiM3L1xx devices contain an LCD segment driver and on-chip bias generation that supports static, 2-mux, 3-mux and 4-mux LCDs with 1/2 or 1/3 bias. The on-chip charge pump with programmable output voltage allows software contrast control which is independent of the supply voltage. LCD timing is derived from the RTC timer clock (RTC0TCLK) to allow precise control over the refresh rate.

The SiM3L1xx devices use registers to store the enabled/disabled state of individual LCD segments. All LCD waveforms are generated on-chip based on the contents of these registers with flexible waveform control to reduce power consumption wherever possible. An LCD blinking function is also supported on a subset of LCD segments.

The LCD0 module has the following features:

- Up to 40 segment pins and 4 common pins.
- Supports LCDs with 1/2 or 1/3 bias.
- Includes an on-chip charge pump with programmable output that allows firmware to control the contrast independent of the supply voltage.
- The RTC timer clock (RTC0TCLK) determines the LCD timing and refresh rate.
- All LCD waveforms are generated on-chip based on the contents of the LCD0 registers with flexible waveform control.
- LCD segments can be placed in a discharge state for a configurable number of RTC clock cycles before switching to the next state to reduce power consumption due to display loading.
- Includes a VBAT monitor that can serve as a wakeup source for Power Mode 8.
- Supports four hardware auto-contrast modes: bypass, constant, minimum, and auto-bypass.
- Supports hardware blinking for up to 8 segments.

4.6.3. Real-Time Clock (RTC0)

The RTC module includes a 32-bit timer that allows up to 36 hours of independent time-keeping when used with a 32.768 kHz watch crystal. The RTC provides three alarm events in addition to a missing clock event, which can also function as interrupt, reset, or wakeup sources on SiM3L1xx devices.

The RTC module includes internal loading capacitors that are programmable to 16 discrete levels, allowing compatibility with a wide range of crystals.

The RTC timer clock can be buffered and routed to a port bank pin to provide an accurate, low frequency clock to other devices while the core is in its lowest power down mode. The module also includes a low power internal low frequency oscillator that reduces low power mode current and is available for other modules to use as a clock source.

The RTC module includes the following features:

- 32-bit timer (supports up to 36 hours) with three separate alarms.
- Option for one alarm to automatically reset the RTC timer.
- Missing clock detector.
- Can be used with the internal Low Frequency Oscillator or with an external 32.768 kHz crystal (no additional resistors or capacitors necessary).
- Programmable internal loading capacitors support a wide range of external 32.768 kHz crystals.
- The RTC timer clock (RTC0CLK) can be buffered and routed to an I/O pin to provide an accurate, low frequency clock to other devices while the core is in its lowest power down mode.
- The RTC module can be powered from the low power mode charge pump for lowest possible power consumption while in PM8.

4.6.4. Low Power Timer (LPTIMER0)

The Low Power Timer (LPTIMER) module runs from the RTC timer clock (RTC0CLK), allowing the LPTIMER to operate even if the AHB and APB clocks are disabled. The LPTIMER counter can increment using one of two clock sources: the clock selected by the RTC0 module, or rising or falling edges of an external signal.

The Low Power Timer includes the following features:

- Runs on low-frequency RTC timer clock (RTC0TCLK).
- The LPTIMER counter can increment using one of two clock sources: the RTC0TCLK or rising or falling edges of an external signal.
- Overflow and threshold-match detection.
- Timer reset on threshold-match allows square-wave generation at a variable output frequency.
- Supports PWM with configurable period and duty cycle.
- The LPTIMER module can be powered from the low power mode charge pump for lowest possible power consumption while in PM8.

4.6.5. Watchdog Timer (WDTIMER0)

The WDTIMER module includes a 16-bit timer, a programmable early warning interrupt, and a programmable reset period. The timer registers are protected from inadvertent access by an independent lock and key interface.

The watchdog timer runs from the low frequency oscillator (LFOSC0).

The Watchdog Timer has the following features:

- Programmable timeout interval.
- Optional interrupt to warn when the Watchdog Timer is nearing the reset trip value.
- Lock-out feature to prevent any modification until a system reset.

4.6.6. Low Power Mode Advanced Capture Counter (ACCTR0)

The SiM3L1xx devices contain a low-power Advanced Capture Counter module that runs from the RTC0 clock domain and can be used with digital inputs, switch topology circuits (reed switches), or with LC resonant circuits. For switch topology circuits, the module charges one or two external lines by pulsing internal pull-up resistors and detecting whether the reed switch is open or closed. For LC resonant circuits, the inputs are periodically energized to produce a dampened sine wave and configurable discriminator circuits detect the resulting decay time-constant.

The advanced capture counter has the following general features:

- Single or differential inputs supporting single, dual, and quadrature modes of operation.
- Variety of interrupt and PM8 wake up sources.
- Provides feedback of the direction history, current and previous states, and condition flags.

The advanced capture counter has the following features for switch circuit topologies:

- Ultra low power input comparators.
- Supports a wide range of pull-up resistor values with a self-calibration engine.
- Asymmetrical integrators for low-pass filtering and switch debounce.
- Two 24-bit counters and two 24-bit digital threshold comparators.
- Supports switch flutter detection.

For LC resonant circuit topologies, the advanced capture counter includes:

- Separate minimum and maximum count registers and polarity, pulse, and toggle controls.
- Zone-based programmable timing.
- Two input comparators with support for a positive side input bias at VIO divided by 2.
- Supports a configurable excitation pulse width based on a 40 MHz oscillator and timer or an external digital stop signal.
- Two 8-bit peak counters that saturate at full scale for detecting the number of LC resonant peaks.
- Two discriminators with programmable thresholds.
- Supports a sample and hold mode for Wheatstone bridges.

All devices in the SiM3L1xx family include the low power mode advanced capture counter (ACCTR0). Table 4.2 lists the supported inputs and outputs for each of the packages.

Table 4.2. SiM3L1xx Supported Advanced Capture Counter Inputs and Outputs

Input/Output	SiM3L1x7	SiM3L1x6	SiM3L1x4
ACCTR0_IN0	✓	✓	✓
ACCTR0_IN1	✓	✓	✓
ACCTR0_LCIN0	✓	✓	
ACCTR0_LCIN1	✓	✓	✓
ACCTR0_STOP0	✓	✓	✓
ACCTR0_STOP1	✓	✓	✓
ACCTR0_LCPUL0	✓	✓	
ACCTR0_LCPUL1	✓	✓	
ACCTR0_LCBIAS0	✓	✓	
ACCTR0_LCBIAS1	✓	✓	
ACCTR0_DBG0	✓	✓	
ACCTR0_DBG1	✓	✓	

Table 6.1. Pin Definitions and Alternate Functions for SiM3L1x7 (Continued)

Pin Name	Type	Pin Numbers (TQFP-80)	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB0.0	Standard I/O	4	VIO	✓	✓		✓	INT0.0 WAKE.0	ADC0.20 VREF CMP0P.0
PB0.1	Standard I/O	3	VIO	✓	✓		✓	INT0.1 WAKE.1	ADC0.21 VREFGND CMP0N.0
PB0.2	Standard I/O	2	VIO	✓	✓		✓	INT0.2 WAKE.2	ADC0.22 CMP1P.0 XTAL2
PB0.3	Standard I/O	1	VIO	✓	✓		✓	INT0.3 WAKE.3	ADC0.23 CMP1N.0 XTAL1
PB0.4	Standard I/O	80	VIO	✓	✓		✓	INT0.4 WAKE.4	ADC0.0 CMP0P.1 IDAC0
PB0.5	Standard I/O	79	VIO	✓	✓		✓	INT0.5 WAKE.5 ACCTR0_STOP0	ACCTR0_IN0
PB0.6	Standard I/O	78	VIO	✓	✓		✓	INT0.6 WAKE.6 ACCTR0_STOP1	ACCTR0_IN1
PB0.7	Standard I/O	77	VIO	✓	✓		✓	INT0.7 WAKE.7	ACCTR0_LCIN0
PB0.8	Standard I/O	76	VIO	✓	✓		✓	LPT0T0 LPT0OUT0 INT0.8 WAKE.8	ACCTR0_LCIN1

Table 6.3. Pin Definitions and Alternate Functions for SiM3L1x4 (Continued)

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB2.1	Standard I/O	28	VIORF	XBR0	✓		LPT0T9 INT1.1 WAKE.13 VIORFCLK	ADC0.3 CMP0N.4
PB2.2	Standard I/O	27	VIORF	XBR0	✓		LPT0T10 INT1.2 WAKE.14	ADC0.4 CMP1P.4
PB2.3	Standard I/O	26	VIORF	XBR0	✓		LPT0T11 INT1.3 WAKE.15	ADC0.5 CMP1N.4
PB2.4	Standard I/O	24	VIORF	XBR0	✓		LPT0T12 INT1.4 SPI1_SCLK	ADC0.6 CMP0P.5
PB2.5	Standard I/O	23	VIORF	XBR0	✓		LPT0T13 INT1.5 SPI1_MISO	ADC0.7 CMP0N.5
PB2.6	Standard I/O	22	VIORF	XBR0	✓		LPT0T14 INT1.6 SPI1_MOSI	ADC0.8 CMP1P.5
PB2.7	Standard I/O	21	VIORF	XBR0	✓		INT1.7 SPI1_NSS	ADC0.9 CMP1N.5
PB3.0	Standard I/O	20	VIO	XBR0	✓		INT1.8	CMP0N.7
PB3.1	Standard I/O	19	VIO	XBR0	✓		INT1.9	CMP1P.7
PB3.2	Standard I/O	18	VIO	XBR0	✓		INT1.10	CMP1N.7
PB3.3	Standard I/O	17	VIO	XBR0	✓		INT1.11	ADC0.10
PB3.4	Standard I/O	16	VIO	XBR0	✓		INT1.12	ADC0.11
PB3.5	Standard I/O	15	VIO	XBR0	✓		INT1.13	ADC0.12

Table 6.8. TQFP-64 Package Dimensions

Dimension	Min	Nominal	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	—	0.20
D	12.00 BSC		
D1	10.00 BSC		
e	0.50 BSC		
E	12.00 BSC		
E1	10.00 BSC		
L	0.45	0.60	0.75
Θ	0°	3.5°	7°
aaa	—	—	0.20
bbb	—	—	0.20
ccc	—	—	0.08
ddd	—	—	0.08

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant ACD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

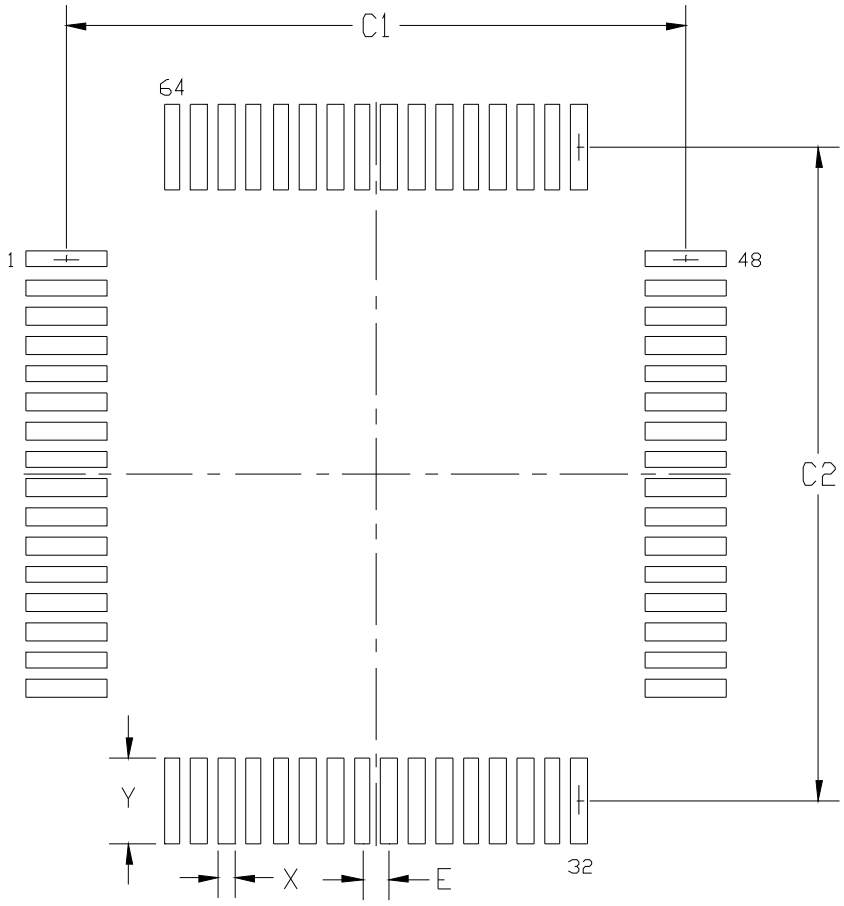

Figure 6.10. TQFP-64 Landing Diagram

Table 6.9. TQFP-64 Landing Diagram Dimensions

Dimension	Min	Max
C1	11.30	11.40
C2	11.30	11.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

6.7. QFN-40 Package Specifications

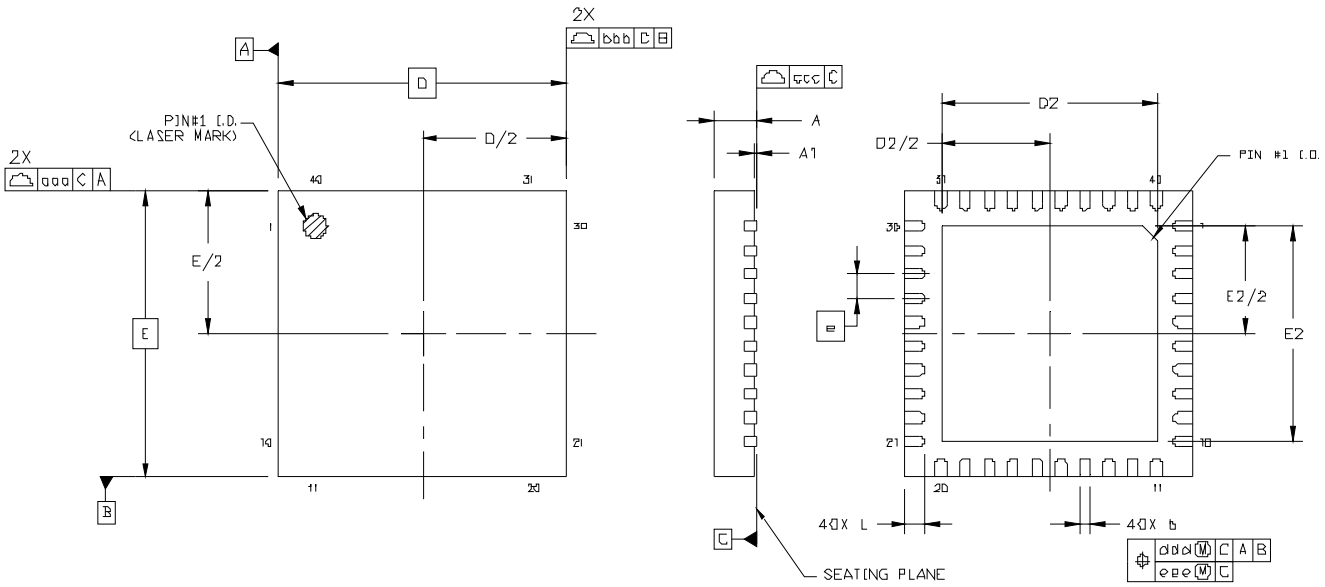

Figure 6.11. QFN-40 Package Drawing

Table 6.10. QFN-40 Package Dimensions

Dimension	Min	Nominal	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		6.00 BSC	
D2	4.35	4.50	4.65
e		0.50 BSC	
E		6.00 BSC	
E2	4.35	4.5	4.65
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

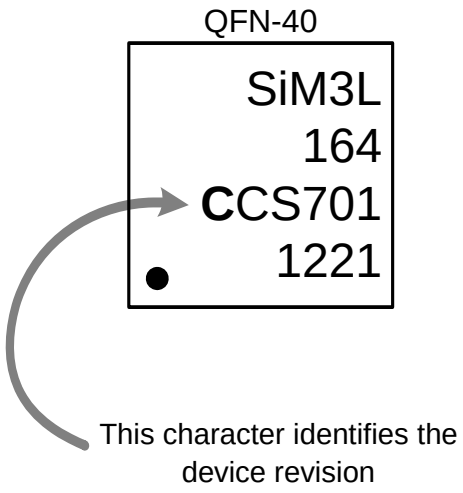

Figure 7.3. SiM3L1x4-GM Revision Information

Document Change List

Revision 0.5 to Revision 1.0

- Updated Electrical Specifications Tables with latest characterization data and production test limits.
- Added missing signal ACCTR0_LCPUL1 to Table 6.2, “Pin Definitions and Alternate Functions for SiM3L1x6,” on page 64.
- Removed ACCTR0_LCIN1 and ACCTR0_STOP0/1 signals from Table 6.3, “Pin Definitions and Alternate Functions for SiM3L1x4,” on page 70.
- Updated Figure 6.8, “TFBGA-80 Package Drawing,” on page 79.

Revision 1.0 to Revision 1.1

- Removed all references to BGA-80 and the parts SiM3L167-C-GL and SiM3L157-C-GL.