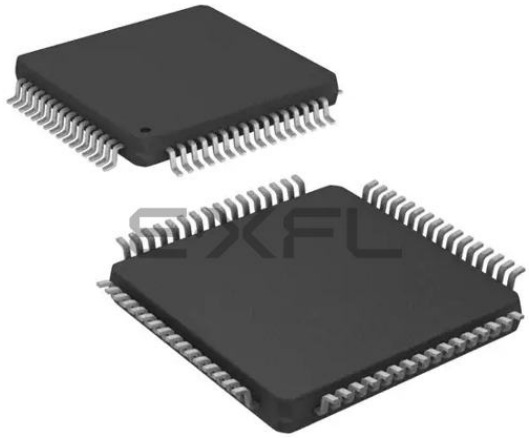

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Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 23x10/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/sim3l166-c-gqr

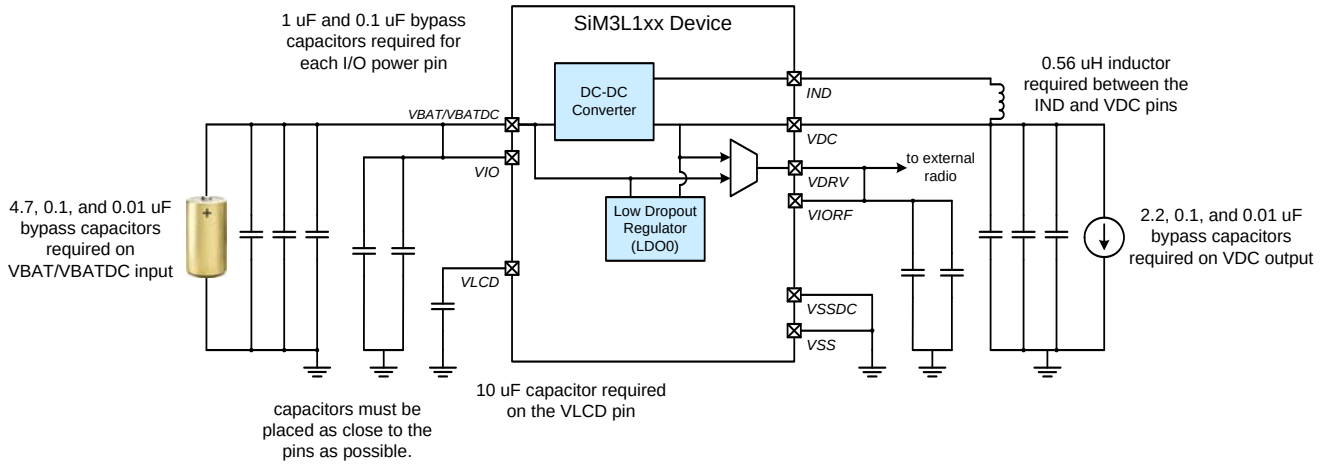

Figure 2.3. Connection Diagram with External Radio Device

Figure 2.4 shows a typical connection diagram for the power pins of the SiM3L1xx devices when the dc-dc buck converter is used and the I/O are powered separately.

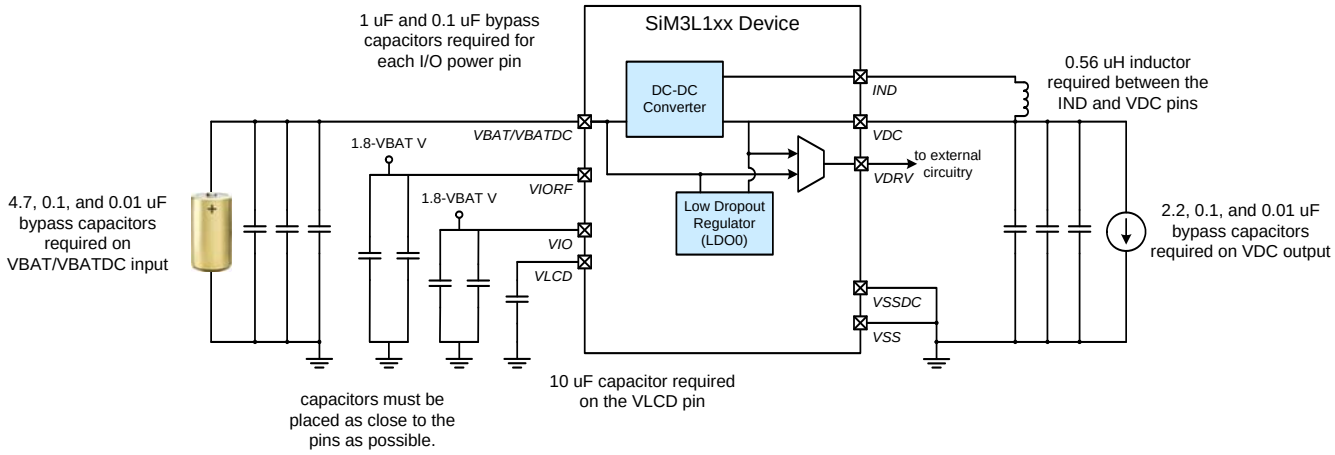

Figure 2.4. Connection Diagram with DC-DC Converter Used and I/O Powered Separately

Table 3.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current						
Normal Mode[1,2,3,4]—Full speed with code executing from flash, peripheral clocks ON	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	17.5	18.9	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	6.7	7.2	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	1.15	1.4	mA
Normal Mode[1,2,3,4]—Full speed with code executing from flash, peripheral clocks OFF	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	13.3	14.5	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	5.4	5.9	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	980	1.2	µA
Normal Mode[1,2,3,4]—Full speed with code executing from flash, LDOs powered by dc-dc at 1.9 V, peripheral clocks OFF	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz V_{BAT} = 3.3 V	—	9.7	—	mA
		F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz V_{BAT} = 3.8 V	—	8.65	—	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz V_{BAT} = 3.3 V	—	4.15	—	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz V_{BAT} = 3.8 V	—	3.9	—	mA

Notes:

1. Currents are additive. For example, where I_{BAT} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded I_{VIO} is included in all I_{BAT} PM8 production test measurements.

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 1[1,2,3,4]—Full speed with code executing from RAM, peripheral clocks ON	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	13.4	16.6	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	4.7	—	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	810	—	µA
Power Mode 1[1,2,3,4]—Full speed with code executing from RAM, peripheral clocks OFF	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	9.4	12.5	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	3.3	—	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	630	—	µA
Power Mode 1[1,2,3,4]—Full speed with code executing from RAM, LDOs powered by dc-dc at 1.9 V, peripheral clocks OFF	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz V_{BAT} = 3.3 V	—	7.05	—	mA
		F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz V_{BAT} = 3.8 V	—	6.3	—	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz V_{BAT} = 3.3 V	—	2.75	—	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz V_{BAT} = 3.8 V	—	2.6	—	mA
Power Mode 2[1,2,3,4,5]—Core halted with peripheral clocks ON	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	7.6	11.3	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	2.75	—	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	575	—	µA

Notes:

1. Currents are additive. For example, where I_{BAT} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded I_{VIO} is included in all I_{BAT} PM8 production test measurements.

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SARADC0	I_{SARADC}	Sampling at 1 Msps, Internal VREF used	—	1.2	1.6	mA
		Sampling at 250 ksps, lowest power mode settings.	—	390	540	µA
Temperature Sensor	I_{TSENSE}		—	75	110	µA
Internal SAR Reference	I_{REFFS}	Normal Power Mode	—	680	—	µA
		Normal Power Mode	—	160	—	µA
VREF0	I_{REFP}		—	80	—	µA
Comparator 0 (CMP0), Comparator 1 (CMP1)	I_{CMP}	CMPMD = 11	—	0.5	2	µA
		CMPMD = 10	—	3	8	µA
		CMPMD = 01	—	10	16	µA
		CMPMD = 00	—	25	42	µA
IDAC0[8]	I_{IDAC}		—	70	100	µA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	10	22	µA
Flash Current on VBAT						
Write Operation	$I_{FLASH-W}$		—	—	8	mA
Erase Operation	$I_{FLASH-E}$		—	—	15	mA

Notes:

1. Currents are additive. For example, where I_{BAT} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded I_{VIO} is included in all I_{BAT} PM8 production test measurements.

Table 3.3. Power Mode Wake Up Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 2 or 6 Wake Time	t_{PM2}		4	—	5	clocks
Power Mode 3 Fast Wake Time (using LFO as clock source)	t_{PM3FW}		—	425	—	µs
Power Mode 8 Wake Time	t_{PM8}		—	3.8	—	µs

Notes:
1. Wake times are specified as the time from the wake source to the execution phase of the first instruction following WFI. This includes latency to recognize the wake event and fetch the first instruction (assuming wait states = 0).

Table 3.4. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{BAT} High Supply Monitor Threshold (VBATHITHEN = 1)	V_{VBATMH}	Early Warning	—	2.20	—	V
		Reset	1.95	2.05	2.1	V
V_{BAT} Low Supply Monitor Threshold (VBATHITHEN = 0)	V_{VBATML}	Early Warning	—	1.85	—	V
		Reset	1.70	1.75	1.77	V
Power-On Reset (POR) Threshold	V_{POR}	Rising Voltage on V_{BAT}	—	1.4	—	V
		Falling Voltage on V_{BAT}	0.8	1	1.3	V
V_{BAT} Ramp Time	t_{RMP}	Time to $V_{BAT} \geq 1.8$ V	10	—	3000	µs
Reset Delay from POR	t_{POR}	Relative to $V_{BAT} \geq V_{POR}$	3	—	100	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	10	—	µs
$\overline{\text{RESET}}$ Low Time to Generate Reset	t_{RSTL}		50	—	—	ns
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	$F_{AHB} > 1$ MHz	—	0.5	1.5	ms
Missing Clock Detector Trigger Frequency	F_{MCD}		—	2.5	10	kHz
V_{BAT} Supply Monitor Turn-On Time	t_{MON}		—	2	—	µs

Table 3.7. Internal Oscillators (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RTC0 Oscillator (RTC0OSC)						
Missing Clock Detector Trigger Frequency	f_{RTCMCD}		—	8	15	kHz
RTC External Input CMOS Clock Frequency	$f_{RTCEXTCLK}$		0	—	40	kHz
RTC Robust Duty Cycle Range	DC_{RTC}		25	—	55	%

Table 3.8. External Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency	f_{CMOS}		0*	—	50	MHz
External Crystal Frequency	f_{XTAL}		0.01	—	25	MHz
External Input CMOS Clock High Time	t_{CMOSH}		9	—	—	ns
External Input CMOS Clock Low Time	t_{CMOSL}		9	—	—	ns
Low Power Mode Charge Pump Supply Range (input from V_{BAT})	V_{BAT}		2.4	—	3.8	V
***Note:** Minimum of 10 kHz when debugging.						

Table 3.16. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (PB0, PB1, PB3, or PB4)	V_{OH}	Low Drive, I_{OH} = –1 mA	V_{IO} – 0.7	—	—	V
		Low Drive, I_{OH} = –10 µA	V_{IO} – 0.1	—	—	V
		High Drive, I_{OH} = –3 mA	V_{IO} – 0.7	—	—	V
		High Drive, I_{OH} = –10 µA	V_{IO} – 0.1	—	—	V
Output High Voltage (PB2)	V_{OH}	Low Drive, I_{OH} = –1 mA	V_{IORF} – 0.7	—	—	V
		Low Drive, I_{OH} = –10 µA	V_{IORF} – 0.1	—	—	V
		High Drive, I_{OH} = –3 mA	V_{IORF} – 0.7	—	—	V
		High Drive, I_{OH} = –10 µA	V_{IORF} – 0.1	—	—	V
Output Low Voltage (any Port I/O pin or $\overline{\text{RESET}}$[1])	V_{OL}	Low Drive, I_{OL} = 1.4 mA	—	—	0.6	V
		Low Drive, I_{OL} = 10 µA	—	—	0.1	V
		High Drive, I_{OL} = 8.5 mA	—	—	0.6	V
		High Drive, I_{OL} = 10 µA	—	—	0.1	V
Input High Voltage (PB0, PB1, PB3, PB4 or $\overline{\text{RESET}}$)	V_{IH}		V_{IO} – 0.6	—	—	V
Input High Voltage (PB2)	V_{IH}		V_{IORF} – 0.6	—	—	V
Input Low Voltage any Port I/O pin or $\overline{\text{RESET}}$)	V_{IL}		—	—	0.6	V
Weak Pull-Up Current[2] (per pin)	I_{PU}	V_{IO} or V_{IORF} = 1.8	-6	-3.5	-2	µA
		V_{IO} or V_{IORF} = 3.8	-32	-20	-10	µA
Input Leakage (Pullups off or Analog)	I_{LK}	$0 \le V_{IN} \le V_{IO}$ or V_{IORF}	-1	—	1	µA

Notes:

1. Specifications for $\overline{\text{RESET}}$ V_{OL} adhere to the low drive setting.
2. On the SiM3L1x6 and SiM3L1x4 devices, the SWV pin will have double the weak pull-up current specified whenever the device is held in reset.

- Supports synchronizing the regulator switching with the system clock.
- Automatically limits the peak inductor current if the load current rises beyond a safe limit.
- Automatically goes into bypass mode if the battery voltage cannot provide sufficient headroom.
- Sources current, but cannot sink current.

4.1.2. Three Low Dropout LDO Regulators (LDO0)

The SiM3L1xx devices include one LDO0 module with three low dropout regulators. Each of these regulators have independent switches to select the battery voltage or the output of the dc-dc converter as the input to each LDO, and an adjustable output voltage.

The LDOs consume little power and provide flexibility in choosing a power supply for the system. Each regulator can be independently adjusted between 0.8 and 1.9 V output.

4.1.3. Voltage Supply Monitor (VMON0)

The SiM3L1xx devices include a voltage supply monitor that can monitor the main supply voltage. This module includes the following features:

- Main supply “VBAT Low” (VBAT below the early warning threshold) notification.
- Holds the device in reset if the main VBAT supply drops below the VBAT Reset threshold.

The voltage supply monitor allows devices to function in known, safe operating conditions without the need for external hardware.

4.1.4. Power Management Unit (PMU)

The Power Management Unit on the SiM3L1xx manages the power systems of the device. It manages the power-up sequence during power on and the wake up sources for PM8. On power-up, the PMU ensures the core voltages are a proper value before core instruction execution begins.

The VDRV pin powers external circuitry from either the VBAT battery input voltage or the output of the dc-dc converter on VDC. The PMU includes an internal switch to select one of these sources for the VDRV pin.

The PMU has a specialized VBAT-divided-by-2 charge pump that can power some internal modules while in PM8 to save power.

The PMU module includes the following features:

- Provides the enable or disable for the analog power system, including the three LDO regulators.
- Up to 14 pin wake inputs can wake the device from Power Mode 8.
- The Low Power Timer, RTC0 (alarms and oscillator failure), Comparator 0, Advanced Capture Counter, LCD0 VBAT monitor, UART0, low power mode charge pump failure, and the RESET pin can also serve as wake sources for Power Mode 8.
- Controls which 4 kB RAM blocks are retained while in Power Mode 8.
- Provides a PMU_Asleep signal to a pin as an indicator that the device is in PM8.
- Specialized charge pump to reduce power consumption in PM8.

Provides control for the internal switch between VBAT and VDC to power the VDRV pin for external circuitry.

4.1.5. Device Power Modes

The SiM3L1xx devices feature seven low power modes in addition to normal operating mode. Several peripherals provide wake up sources for these low power modes, including the Low Power Timer (LPTIMER0), RTC0 (alarms and oscillator failure notification), Comparator 0 (CMP0), Advanced Capture Counter (ACCTR0), LCD VBAT monitor (LCD0), UART0, low power mode charge pump failure, and PMU Pin Wake.

In addition, all peripherals can have their clocks disabled to reduce power consumption whenever a peripheral is not being used using the clock control (CLKCTRL) registers.

4.1.5.1. Normal Mode (Power Mode 0) and Power Mode 4

Normal Mode and Power Mode 4 are fully operational modes with code executing from flash memory. PM4 is the same as Normal Mode, but with the clocks operating at a lower speed. This enables power to be conserved by reducing the LDO regulator outputs.

4.1.5.6. Power Mode Summary

The power modes described above are summarized in Table 4.1. Table 3.2 and Table 3.3 provide more information on the power consumption and wake up times for each mode.

Table 4.1. SiM3L1xx Power Modes

Mode	Description	Notes
Normal	■ Core operating at full speed ■ Code executing from flash	■ Full device operation
Power Mode 1 (PM1)	■ Core operating at full speed ■ Code executing from RAM	■ Full device operation ■ Higher CPU bandwidth than PM0 (RAM can operate with zero wait states at any frequency)
Power Mode 2 (PM2)	■ Core halted ■ AHB, APB and all peripherals operational at full speed	■ Fast wakeup from any interrupt source
Power Mode 3 (PM3)	■ All clocks to core and peripherals stopped ■ Faster wake enabled by keeping LFOSC0 or RTC0TCLK active	■ Wake on any wake source or reset source defined in the PMU
Power Mode 4 (PM4)	■ Core operating at low speed ■ Code executing from flash	■ Same capabilities as PM0, operating at lower speed ■ Lower clock speed enables lower LDO output settings to save power
Power Mode 5 (PM5)	■ Core operating at low speed ■ Code executing from RAM	■ Same capabilities as PM1, operating at lower speed ■ Lower clock speed enables lower LDO output settings to save power
Power Mode 6 (PM6)	■ Core halted ■ AHB, APB and all peripherals operational at low speed	■ Same capabilities as PM2, operating at lower speed ■ Lower clock speed enables lower LDO output settings to save power ■ When running from LFOSC0, power is similar to PM3, but the device wakes much faster
Power Mode 8 (PM8)	■ Low power sleep ■ LDO regulators are disabled and all active circuitry operates directly from VBAT ■ The following functions are available: ACCTR0, RTC0, UART0 running from RTC0TCLK, LPTIMER0, port match, and the LCD controller ■ Register and RAM state retention	■ Lowest power consumption ■ Wake on any wake source or reset source defined in the PMU

4.1.6. Process/Voltage/Temperature Monitor (TIMER2 and PVTOSC0)

The Process/Voltage/Temperature monitor consists of two modules (TIMER2 and PVTOSC0) designed to monitor the digital circuit performance of the SiM3L1xx device.

The PVT oscillator (PVTOSC0) consists of two oscillators, one operating from the memory LDO and one operating from the digital LDO. These oscillators have two independent speed options and provide the clocks for two 16-bit timers in the TIMER2 module using the EX input. By monitoring the resulting counts of the TIMER2 timers, firmware can monitor the current device performance and increase the scalable LDO regulator (LDO0) output voltages as needed or decrease the output voltages to save power.

The PVT monitor has the following features:

- Two separate oscillators and timers for the memory and digital logic voltage domains.
- Two oscillator output divider settings.
- Provides a method for monitoring digital performance to allow firmware to adjust the scalable LDO regulator output voltages to the lowest level possible, saving power.

4.3.1. PLL (PLL0)

The PLL module consists of a dedicated Digitally-Controlled Oscillator (DCO) that can be used in Free-Running mode without a reference frequency, Frequency-Locked to a reference frequency, or Phase-Locked to a reference frequency. The reference frequency for Frequency-Lock and Phase-Lock modes can use one of multiple sources (including the external oscillator) to provide maximum flexibility for different application needs. Because the PLL module generates its own clock, the DCO can be locked to a particular reference frequency and then moved to Free-Running mode to reduce system power and noise.

The PLL module includes the following features:

- Three output ranges with output frequencies ranging from 23 to 50 MHz.
- Multiple reference frequency inputs, including the RTC0 oscillator, Low Power Oscillator, and external oscillator.
- Three output modes: Free-Running Digitally-Controlled Oscillator, Frequency-Locked, and Phase-Locked.
- Able to sense the rising edge or falling edge of the reference source.
- DCO frequency LSB dithering to provide finer average output frequencies.
- Spectrum spreading to reduce generated system noise.
- Low jitter and fast lock times.\
- All output frequency updates (including dithering and spectrum spreading) can be temporarily suspended using the STALL bit during noise-sensitive measurements.

4.3.2. Low Power Oscillator (LPOSC0)

The Low Power Oscillator is the default AHB oscillator on SiM3L1xx devices and enables or disables automatically, as needed.

The default output frequency of this oscillator is factory calibrated to 20 MHz, and a divided 2.5 MHz version of this clock is also available as an AHB clock source.

The Low Power Oscillator has the following features:

- 20 MHz and divided 2.5 MHz frequencies available for the AHB clock.
- Automatically starts and stops as needed.

4.3.3. Low Frequency Oscillator (LFOSC0)

The low frequency oscillator (LFOSC) provides a low power internal clock source for the RTC0 timer and other peripherals on the device. No external components are required to use the low frequency oscillator, and the RTC1 and RTC2 pins do not need to be shorted together.

The Low Frequency Oscillator has the following features:

- 16.4 kHz output frequency.

4.3.4. External Oscillators (EXTOSC0)

The EXTOSC0 external oscillator circuit may drive an external crystal, ceramic resonator, capacitor, or RC network. A CMOS clock may also provide a clock input. The external oscillator output may be selected as the AHB clock or used to clock other modules independent of the AHB clock selection.

The External Oscillator control has the following features:

- Support for external crystal, resonator, RC, C, or CMOS oscillators.
- Support for external CMOS frequencies from 10 kHz to 50 MHz.
- Support for external crystal frequencies from 10 kHz to 25 MHz.
- Various drive strengths for flexible crystal oscillator support.
- Internal frequency divide-by-two option available.

4.6.3. Real-Time Clock (RTC0)

The RTC module includes a 32-bit timer that allows up to 36 hours of independent time-keeping when used with a 32.768 kHz watch crystal. The RTC provides three alarm events in addition to a missing clock event, which can also function as interrupt, reset, or wakeup sources on SiM3L1xx devices.

The RTC module includes internal loading capacitors that are programmable to 16 discrete levels, allowing compatibility with a wide range of crystals.

The RTC timer clock can be buffered and routed to a port bank pin to provide an accurate, low frequency clock to other devices while the core is in its lowest power down mode. The module also includes a low power internal low frequency oscillator that reduces low power mode current and is available for other modules to use as a clock source.

The RTC module includes the following features:

- 32-bit timer (supports up to 36 hours) with three separate alarms.
- Option for one alarm to automatically reset the RTC timer.
- Missing clock detector.
- Can be used with the internal Low Frequency Oscillator or with an external 32.768 kHz crystal (no additional resistors or capacitors necessary).
- Programmable internal loading capacitors support a wide range of external 32.768 kHz crystals.
- The RTC timer clock (RTC0CLK) can be buffered and routed to an I/O pin to provide an accurate, low frequency clock to other devices while the core is in its lowest power down mode.
- The RTC module can be powered from the low power mode charge pump for lowest possible power consumption while in PM8.

4.6.4. Low Power Timer (LPTIMER0)

The Low Power Timer (LPTIMER) module runs from the RTC timer clock (RTC0CLK), allowing the LPTIMER to operate even if the AHB and APB clocks are disabled. The LPTIMER counter can increment using one of two clock sources: the clock selected by the RTC0 module, or rising or falling edges of an external signal.

The Low Power Timer includes the following features:

- Runs on low-frequency RTC timer clock (RTC0TCLK).
- The LPTIMER counter can increment using one of two clock sources: the RTC0TCLK or rising or falling edges of an external signal.
- Overflow and threshold-match detection.
- Timer reset on threshold-match allows square-wave generation at a variable output frequency.
- Supports PWM with configurable period and duty cycle.
- The LPTIMER module can be powered from the low power mode charge pump for lowest possible power consumption while in PM8.

4.6.5. Watchdog Timer (WDTIMER0)

The WDTIMER module includes a 16-bit timer, a programmable early warning interrupt, and a programmable reset period. The timer registers are protected from inadvertent access by an independent lock and key interface.

The watchdog timer runs from the low frequency oscillator (LFOSC0).

The Watchdog Timer has the following features:

- Programmable timeout interval.
- Optional interrupt to warn when the Watchdog Timer is nearing the reset trip value.
- Lock-out feature to prevent any modification until a system reset.

4.7. Communications Peripherals

4.7.1. USART (USART0)

The USART uses two signals (TX and RX) to communicate serially with an external device. In addition to these signals, the USART module can optionally use a clock (UCLK) or hardware handshaking (RTS and CTS).

The USART module provides the following features:

- Independent transmitter and receiver configurations with separate 16-bit baud rate generators.
- Synchronous or asynchronous transmissions and receptions.
- Clock master or slave operation with programmable polarity and edge controls.
- Up to 5 Mbaud (synchronous or asynchronous, TX or RX, and master or slave) or 1 Mbaud Smartcard (TX or RX).
- Individual enables for generated clocks during start, stop, and idle states.
- Internal transmit and receive FIFOs with flush capability and support for byte, half-word, and word reads and writes.
- Data bit lengths from 5 to 9 bits.
- Programmable inter-packet transmit delays.
- Auto-baud detection with support for the LIN SYNC byte.
- Automatic parity generation (with enable).
- Automatic start and stop generation (with separate enables).
- Transmit and receive hardware flow-control.
- Independent inversion correction for TX, RX, RTS, and CTS signals.
- IrDA modulation and demodulation with programmable pulse widths.
- Smartcard ACK/NACK support.
- Parity error, frame error, overrun, and underrun detection.
- Multi-master and half-duplex support.
- Multiple loop-back modes supported.
- Multi-processor communications support.

4.7.2. UART (UART0)

The low-power UART uses two signals (TX and RX) to communicate serially with an external device.

The UART0 module can operate in PM8 mode by taking the clock directly from the RTC0 time clock (RTC0TCLK) and running from the low power mode charge pump. This will allow the system to conserve power while transmitting or receiving UART traffic. The UART supports standard baud-rates of 9600, 4800, 2400 and 1200 in this low power mode.

The UART0 module provides the following features:

- Independent transmitter and receiver configurations with separate 16-bit baud rate generators.
- Asynchronous transmissions and receptions.
- Up to 5 Mbaud (TX or RX).
- Internal transmit and receive FIFOs with flush capability and support for byte, half-word, and word reads and writes.
- Data bit lengths from 5 to 9 bits.
- Programmable inter-packet transmit delays.
- Auto-baud detection with support for the LIN SYNC byte.
- Automatic parity generation (with enable).
- Automatic start and stop generation (with separate enables).
- Independent inversion correction for TX and RX signals.
- Parity error, frame error, overrun, and underrun detection.
- Half-duplex support.

6. Pin Definitions

6.1. SiM3L1x7 Pin Definitions

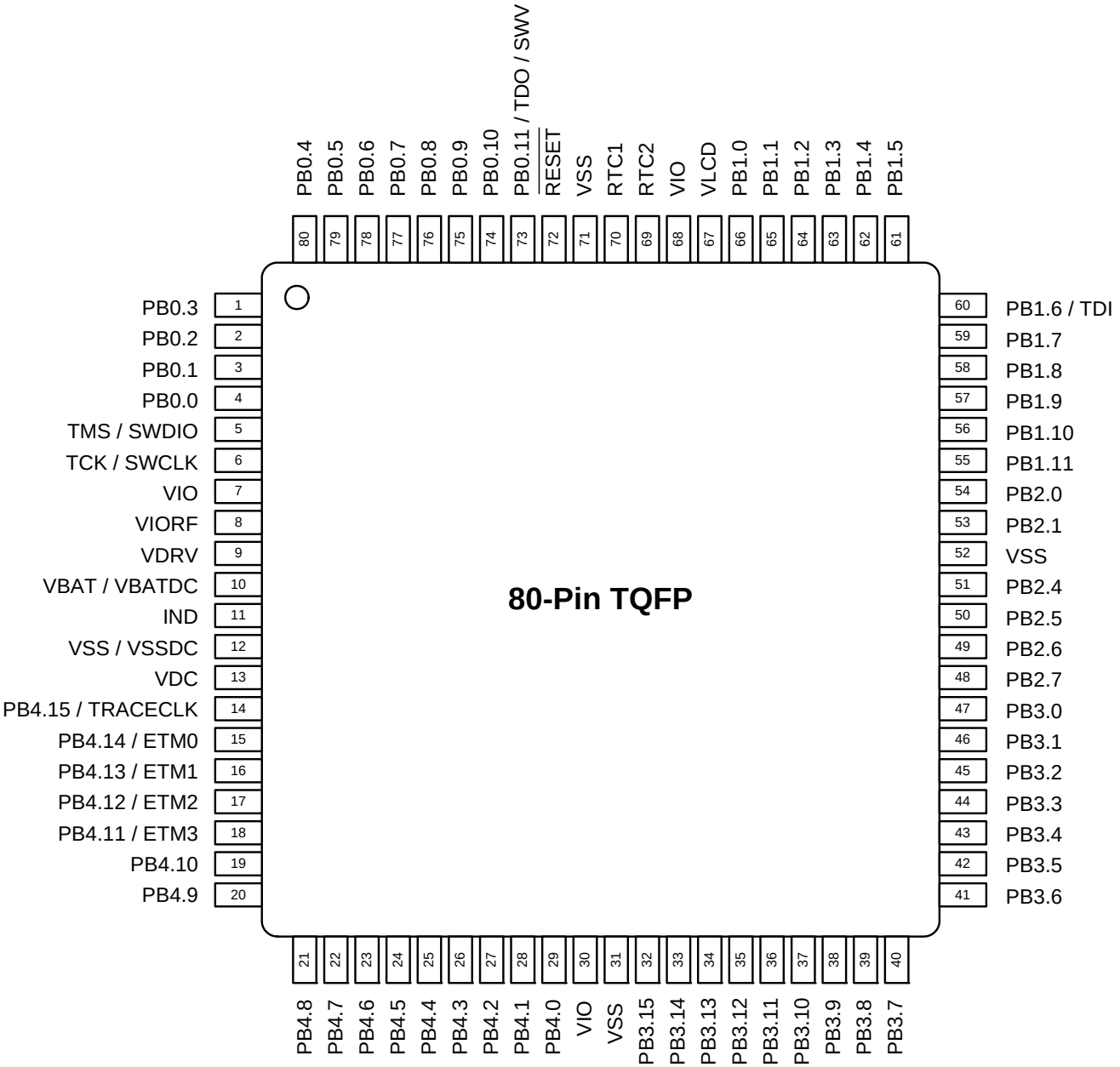

Figure 6.1. SiM3L1x7-GQ Pinout

Table 6.1. Pin Definitions and Alternate Functions for SiM3L1x7

Pin Name	Type	Pin Numbers (TQFP-80)	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
VSS	Ground	12 31 52 71							
VSSDC	Ground (DC-DC)	12							
VIO	Power (I/O)	7 30 68							
VIORF	Power (RF I/O)	8							
VBAT/ VBATDC		10							
VDRV		9							
VDC		13							
VLCD	Power (LCD Charge Pump)	67							
IND	DC-DC Inductor	11							
$\overline{\text{RESET}}$	Active-low Reset	72							
TCK/ SWCLK	JTAG / Serial Wire	6							
TMS/ SWDIO	JTAG / Serial Wire	5							
RTC1	RTC Oscillator Input	70							
RTC2	RTC Oscillator Output	69							

Table 6.1. Pin Definitions and Alternate Functions for SiM3L1x7 (Continued)

Pin Name	Type	Pin Numbers (TQFP-80)	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB0.0	Standard I/O	4	VIO	✓	✓		✓	INT0.0 WAKE.0	ADC0.20 VREF CMP0P.0
PB0.1	Standard I/O	3	VIO	✓	✓		✓	INT0.1 WAKE.1	ADC0.21 VREFGND CMP0N.0
PB0.2	Standard I/O	2	VIO	✓	✓		✓	INT0.2 WAKE.2	ADC0.22 CMP1P.0 XTAL2
PB0.3	Standard I/O	1	VIO	✓	✓		✓	INT0.3 WAKE.3	ADC0.23 CMP1N.0 XTAL1
PB0.4	Standard I/O	80	VIO	✓	✓		✓	INT0.4 WAKE.4	ADC0.0 CMP0P.1 IDAC0
PB0.5	Standard I/O	79	VIO	✓	✓		✓	INT0.5 WAKE.5 ACCTR0_STOP0	ACCTR0_IN0
PB0.6	Standard I/O	78	VIO	✓	✓		✓	INT0.6 WAKE.6 ACCTR0_STOP1	ACCTR0_IN1
PB0.7	Standard I/O	77	VIO	✓	✓		✓	INT0.7 WAKE.7	ACCTR0_LCIN0
PB0.8	Standard I/O	76	VIO	✓	✓		✓	LPT0T0 LPT0OUT0 INT0.8 WAKE.8	ACCTR0_LCIN1

Table 6.2. Pin Definitions and Alternate Functions for SiM3L1x6 (Continued)

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB2.5	Standard I/O	39	VIORF	XBR0	✓			LPT0T13 INT1.5 SPI1_MISO	ADC0.8 CMP0N.5
PB2.6	Standard I/O	38	VIORF	XBR0	✓			LPT0T14 INT1.6 SPI1_MOSI	ADC0.9 CMP1P.5
PB2.7	Standard I/O	37	VIORF	XBR0	✓			INT1.7 SPI1_NSS	ADC0.10 CMP1N.5
PB3.0	Standard I/O	36	VIO	XBR0	✓	LCD0.20		INT1.8	ADC0.11
PB3.1	Standard I/O	35	VIO	XBR0	✓	LCD0.19		INT1.9	ADC0.12
PB3.2	Standard I/O	34	VIO	XBR0	✓	LCD0.18		INT1.10	CMP0P.6
PB3.3	Standard I/O	33	VIO	XBR0	✓	LCD0.17		INT1.11	CMP0N.6
PB3.4	Standard I/O	32	VIO	XBR0	✓	LCD0.16		INT1.12	CMP0P.7
PB3.5	Standard I/O	31	VIO	XBR0	✓	LCD0.15		INT1.13	CMP0N.7
PB3.6	Standard I/O	30	VIO	XBR0	✓	LCD0.14		INT1.14	CMP1P.7
PB3.7	Standard I/O	29	VIO	XBR0	✓	LCD0.13		INT1.15	CMP1N.7
PB3.8	Standard I/O	28	VIO		✓	LCD0.12			ADC0.13
PB3.9	Standard I/O	27	VIO		✓	LCD0.11			ADC0.14
PB3.10	Standard I/O	26	VIO		✓	COM0.3			
PB3.11	Standard I/O	25	VIO		✓	COM0.2			

Table 6.3. Pin Definitions and Alternate Functions for SiM3L1x4

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
VSS	Ground	9 25						
VSSDC	Ground (DC-DC)	9						
VIO	Power (I/O)	5						
VIORF / VDRV	Power (RF I/O)	6						
VBAT / VBATDC		7						
VDC		10						
IND	DC-DC Inductor	8						
$\overline{\text{RESET}}$	Active-low Reset	35						
SWCLK	Serial Wire	4						
SWDIO	Serial Wire	3						
RTC1	RTC Oscillator Input	34						
RTC2	RTC Oscillator Output	33						
PB0.0	Standard I/O	2	VIO	XBR0	✓	✓	INT0.0 WAKE.0	ADC0.20 VREF CMP0P.0
PB0.1	Standard I/O	1	VIO	XBR0	✓	✓	INT0.1 WAKE.2	ADC0.22 CMP0N.0 CMP1P.0 XTAL2

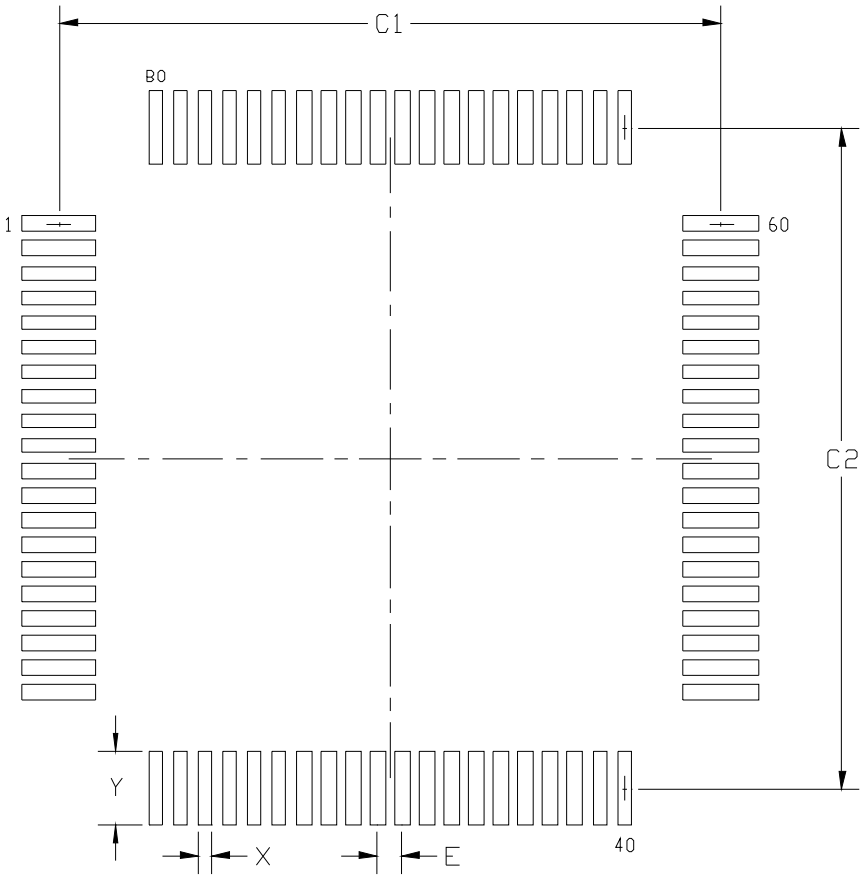

Figure 6.6. TQFP-80 Landing Diagram

Table 6.5. TQFP-80 Landing Diagram Dimensions

Dimension	Min	Max
C1	13.30	13.40
C2	13.30	13.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

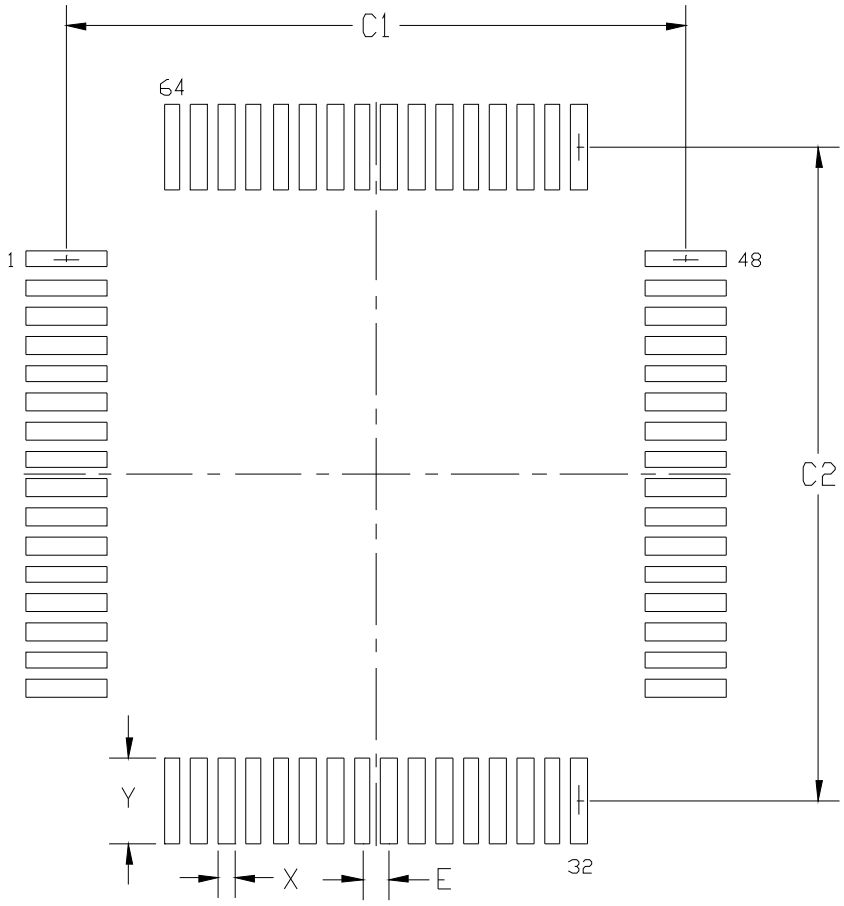

Figure 6.10. TQFP-64 Landing Diagram

Table 6.9. TQFP-64 Landing Diagram Dimensions

Dimension	Min	Max
C1	11.30	11.40
C2	11.30	11.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.