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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 24x10/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TFBGA
Supplier Device Package	80-TFBGA (5.5x5.5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/sim3l167-c-glr

3. Electrical Specifications

3.1. Electrical Characteristics

All electrical parameters in all Tables are specified under the conditions listed in Table 3.1, unless stated otherwise.

Table 3.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VBAT/VBATDC	V_{BAT}		1.8	—	3.8	V
Operating Supply Voltage on VDC	V_{DC}		1.25	—	3.8	V
Operating Supply Voltage on VDRV	V_{DRV}		1.25	—	3.8	V
Operating Supply Voltage on VIO	V_{IO}		1.8	—	V_{BAT}	V
Operation Supply Voltage on VIORF	V_{IORF}		1.8	—	V_{BAT}	V
Operation Supply Voltage on VLCD	V_{LCD}		1.8	—	3.8	V
System Clock Frequency (AHB)	f_{AHB}		0	—	50	MHz
Peripheral Clock Frequency (APB)	f_{APB}		0	—	50	MHz
Operating Ambient Temperature	T_A		–40	—	+85	°C
Operating Junction Temperature	T_J		–40	—	105	°C

Note: All voltages with respect to V_{SS}.

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 2[1,2,3,4,5]—Core halted with only Port I/O clocks on (wake from pin).	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	4	7.2	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	1.47	—	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	430	—	µA
Power Mode 3[1,2,6]—Fast-Wake Mode (PM3CLKEN = 1)	I_{BAT}	V_{BAT} = 3.8 V	—	320	530	µA
		V_{BAT} = 1.8 V	—	225	—	µA
Power Mode 4[1,2,4,6]—Slower clock speed with code executing from flash, peripheral clocks ON	I_{BAT}	F_{AHB} = F_{APB} = 16 kHz, V_{BAT} = 3.8 V	—	385	640	µA
		F_{AHB} = F_{APB} = 16 kHz, V_{BAT} = 1.8 V	—	330	—	µA
Power Mode 5[1,2,4,6]—Slower clock speed with code executing from RAM, peripheral clocks ON	I_{BAT}	F_{AHB} = F_{APB} = 16 kHz, V_{BAT} = 3.8 V	—	320	490	µA
		F_{AHB} = F_{APB} = 16 kHz, V_{BAT} = 1.8 V	—	275	—	µA
Power Mode 6[1,2,4,6]—Core halted with peripheral clocks ON	I_{BAT}	F_{AHB} = F_{APB} = 16 kHz, V_{BAT} = 3.8 V	—	315	490	µA
		F_{AHB} = F_{APB} = 16 kHz, V_{BAT} = 1.8 V	—	270	—	µA
Power Mode 8[1,2]—Low Power Sleep, powered through VBAT, VIO, and VIORF at 2.4 V, 32kB of retention RAM	I_{BAT}	RTC Disabled, T_A = 25 °C	—	75	400	nA
		RTC w/ 16.4 kHz LFO, T_A = 25 °C	—	360	—	nA
		RTC w/ 32.768 kHz Crystal, T_A = 25 °C	—	670	—	nA

Notes:

1. Currents are additive. For example, where I_{BAT} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded I_{VIO} is included in all I_{BAT} PM8 production test measurements.

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SARADC0	I_{SARADC}	Sampling at 1 Msps, Internal VREF used	—	1.2	1.6	mA
		Sampling at 250 ksps, lowest power mode settings.	—	390	540	µA
Temperature Sensor	I_{TSENSE}		—	75	110	µA
Internal SAR Reference	I_{REFFS}	Normal Power Mode	—	680	—	µA
		Normal Power Mode	—	160	—	µA
VREF0	I_{REFP}		—	80	—	µA
Comparator 0 (CMP0), Comparator 1 (CMP1)	I_{CMP}	CMPMD = 11	—	0.5	2	µA
		CMPMD = 10	—	3	8	µA
		CMPMD = 01	—	10	16	µA
		CMPMD = 00	—	25	42	µA
IDAC0[8]	I_{IDAC}		—	70	100	µA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	10	22	µA
Flash Current on VBAT						
Write Operation	$I_{FLASH-W}$		—	—	8	mA
Erase Operation	$I_{FLASH-E}$		—	—	15	mA

Notes:

1. Currents are additive. For example, where I_{BAT} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded I_{VIO} is included in all I_{BAT} PM8 production test measurements.

Table 3.5. On-Chip Regulators (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Memory LDO Output Setting[5]	V_{LDOMEM}	During Programming	1.8	—	1.9	V
		During Normal Operation	1.5	—	1.9	V
Digital LDO Output Setting	V_{LDODIG}	$F_{AHB} \leq 20$ MHz	1.0	—	1.9	V
		$F_{AHB} > 20$ MHz	1.2	—	1.9	V
Analog LDO Output Setting During Normal Operation[6]	V_{LDOANA}		1.8			V

Notes:

1. See reference manual for recommended inductors.
2. Recommended: X7R or X5R ceramic capacitors with low ESR. Example: Murata GRM21BR71C225K with ESR < 10 mΩ (@ frequency > 1 MHz).
3. Input voltage specification accounts for the internal LDO dropout voltage under the maximum load condition to ensure that the LDO output voltage will remain at a valid level as long as V_{LDOIN} is at or above the specified minimum.
4. The memory LDO output should always be set equal to or lower than the output of the analog LDO. When lowering both LDOs (for example to go into PM8 under low supply conditions), first adjust the memory LDO and then the analog LDO. When raising the output of both LDOs, adjust the analog LDO before adjusting the memory LDO.
5. Output range represents the programmable output range, and does not reflect the minimum voltage under all conditions. Dropout when the input supply is close to the output setting is normal, and accounted for.
6. Analog peripheral specifications assume a 1.8 V output on the analog LDO.

Table 3.7. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Phase-Locked Loop (PLL0OSC)						
Calibrated Output Frequency (Free-running output mode, RANGE = 2)	$f_{PLL0OSC}$	Full Temperature and Supply Range	48.3	49	49.7	MHz
Power Supply Sensitivity (Free-running output mode, RANGE = 2)	$PSS_{PLL0OSC}$	T_A = 25 °C, Fout = 49 MHz	—	300	—	ppm/V
Temperature Sensitivity (Free-running output mode, RANGE = 2)	$TS_{PLL0OSC}$	V_{BAT} = 3.3 V, Fout = 49 MHz	—	50	—	ppm/°C
Adjustable Output Frequency Range	$f_{PLL0OSC}$		23	—	50	MHz
Lock Time	$t_{PLL0LOCK}$	f_{REF} = 20 MHz, $f_{PLL0OSC}$ = 50 MHz M=39, N=99, LOCKTH = 0	—	2.75	—	µs
		f_{REF} = 2.5 MHz, $f_{PLL0OSC}$ = 50 MHz M=19, N=399, LOCKTH = 0	—	9.45	—	µs
		f_{REF} = 32.768 kHz, $f_{PLL0OSC}$ = 50 MHz M=0, N=1524, LOCKTH = 0	—	92	—	µs
Low Power Oscillator (LPOSC0)						
Oscillator Frequency	f_{LPOSC}	Full Temperature and Supply Range	19	20	21	MHz
Divided Oscillator Frequency	f_{LPOSCD}	Full Temperature and Supply Range	2.375	2.5	2.625	MHz
Power Supply Sensitivity	PSS_{LPOSC}	T_A = 25 °C	—	0.5	—	%/V
Temperature Sensitivity	TS_{LPOSC}	V_{BAT} = 3.3 V	—	55	—	ppm/°C
Low Frequency Oscillator (LFOSC0)						
Oscillator Frequency	f_{LFOSC}	Full Temperature and Supply Range	13.4	16.4	19.7	kHz
		T_A = 25 °C, V_{BAT} = 3.3 V	15.8	16.4	17.3	kHz
Power Supply Sensitivity	PSS_{LFOSC}	T_A = 25 °C	—	2.4	—	%/V
Temperature Sensitivity	TS_{LFOSC}	V_{BAT} = 3.3 V	—	0.2	—	%/°C

Table 3.9. SAR ADC (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset Temperature Coefficient	TC_{OFF}		—	0.004	—	LSB/°C
Slope Error	E_M		–0.07	–0.02	0.02	%
Dynamic Performance (10 kHz Sine Wave Input 1dB below full scale, Max throughput)						
Signal-to-Noise	SNR	12 Bit Mode	62	66	—	dB
		10 Bit Mode	58	60	—	dB
Signal-to-Noise Plus Distortion	SNDR	12 Bit Mode	62	66	—	dB
		10 Bit Mode	58	60	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD	12 Bit Mode	—	78	—	dB
		10 Bit Mode	—	77	—	dB
Spurious-Free Dynamic Range	SFDR	12 Bit Mode	—	–79	—	dB
		10 Bit Mode	—	–74	—	dB
***Note:** Absolute input pin voltage is limited by the lower of the supply at VBAT and VIO.						

Table 3.11. ACCTR (Advanced Capture Counter)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LC Comparator Response Time, CMPMD = 11 (Highest Speed)	t_{RESP0}	+100 mV Differential	—	100	—	ns
		–100 mV Differential	—	150	—	ns
LC Comparator Response Time, CMPMD = 00 (Lowest Power)	t_{RESP3}	+100 mV Differential	—	1.4	—	µs
		–100 mV Differential	—	3.5	—	µs
LC Comparator Positive Hysteresis Mode 0 (CPMD = 11)	HYS_{CP+}	CMPHYP = 00	—	0.37	—	mV
		CMPHYP = 01	—	7.9	—	mV
		CMPHYP = 10	—	16.7	—	mV
		CMPHYP = 11	—	32.8	—	mV
LC Comparator Negative Hysteresis Mode 0 (CPMD = 11)	HYS_{CP-}	CMPHYN = 00	—	0.37	—	mV
		CMPHYN = 01	—	–7.9	—	mV
		CMPHYN = 10	—	–16.1	—	mV
		CMPHYN = 11	—	–32.7	—	mV
LC Comparator Positive Hysteresis Mode 1 (CPMD = 10)	HYS_{CP+}	CMPHYP = 00	—	0.47	—	mV
		CMPHYP = 01	—	5.85	—	mV
		CMPHYP = 10	—	12	—	mV
		CMPHYP = 11	—	24.4	—	mV
LC Comparator Negative Hysteresis Mode 1 (CPMD = 10)	HYS_{CP-}	CMPHYN = 00	—	0.47	—	mV
		CMPHYN = 01	—	–6.0	—	mV
		CMPHYN = 10	—	–12.1	—	mV
		CMPHYN = 11	—	–24.6	—	mV
LC Comparator Positive Hysteresis Mode 2 (CPMD = 01)	HYS_{CP+}	CMPHYP = 00	—	0.66	—	mV
		CMPHYP = 01	—	4.55	—	mV
		CMPHYP = 10	—	9.3	—	mV
		CMPHYP = 11	—	19	—	mV
LC Comparator Negative Hysteresis Mode 2 (CPMD = 01)	HYS_{CP-}	CMPHYN = 00	—	0.6	—	mV
		CMPHYN = 01	—	–4.5	—	mV
		CMPHYN = 10	—	–9.5	—	mV
		CMPHYN = 11	—	–19	—	mV

Table 3.12. Voltage Reference Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage	V_{REFFS}	–40 to +85 °C, V_{BAT} = 1.8–3.8 V	1.6	1.65	1.7	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{REFFS}		—	—	1.5	µs
Power Supply Rejection	$PSRR_{REFFS}$		—	400	—	ppm/V
Internal Precision Reference						
Valid Supply Range	V_{BAT}	VREF2X = 0	1.8	—	3.8	V
		VREF2X = 1	2.7	—	3.8	V
Output Voltage	V_{REFP}	25 °C ambient, VREF2X = 0	1.17	1.2	1.23	V
		25 °C ambient, VREF2X = 1	2.35	2.4	2.45	V
Short-Circuit Current	I_{SC}		—	—	10	mA
Temperature Coefficient	TC_{VREFP}		—	35	—	ppm/°C
Load Regulation	LR_{VREFP}	Load = 0 to 200 µA to VREFGND	—	4.5	—	ppm/µA
Load Capacitor	C_{VREFP}	Load = 0 to 200 µA to VREFGND	0.1	—	—	µF
Turn-on Time	$t_{VREFPON}$	4.7 µF tantalum, 0.1 µF ceramic bypass	—	3.8	—	ms
		0.1 µF ceramic bypass	—	200	—	µs
Power Supply Rejection	$PSRR_{VREFP}$	VREF2X = 0	—	320	—	ppm/V
		VREF2X = 1	—	560	—	ppm/V
External Reference						
Input Current	I_{EXTREF}	Sample Rate = 250 ksps; VREF = 3.0 V	—	5.25	—	µA

Table 3.13. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	V_{OFF}	T_A = 0 °C	—	760	—	mV
Offset Error*	E_{OFF}	T_A = 0 °C	—	±14	—	mV
Slope	M		—	2.77	—	mV/°C
Slope Error*	E_M		—	±25	—	µV/°C
Linearity			—	1	—	°C
Turn-on Time			—	1.8	—	µs

***Note:** Absolute input pin voltage is limited by the lower of the supply at VBAT and VIO.

3.2. Thermal Conditions

Table 3.17. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance*	θ_{JA}	TQFP-80 Packages	—	40	—	°C/W
		QFN-64 Packages	—	25	—	°C/W
		TQFP-64 Packages	—	30	—	°C/W
		QFN-40 Packages	—	30	—	°C/W
***Note:** Thermal resistance assumes a multi-layer PCB with the exposed pad soldered to a topside PCB pad.						

4.1. Power

The SiM3L1xx devices include a dc-dc buck converter that can take an input from 1.8–3.8 V and create an output from 1.25–3.8 V. In addition, SiM3L1xx devices include three low dropout regulators as part of the LDO0 module: one LDO powers the analog subsystems, one LDO powers the flash and SRAM memory at 1.8 V, and one LDO powers the digital and core circuitry. Each of these regulators can be independently powered from the dc-dc converter or directly from the battery voltage, and their outputs are adjustable to conserve system power. SiM3L1xx devices also include a low power charge pump in the PMU module for use in low power modes (PM8) to further reduce the power consumption of the device.

Figure 4.2 shows the power system configuration of these devices.

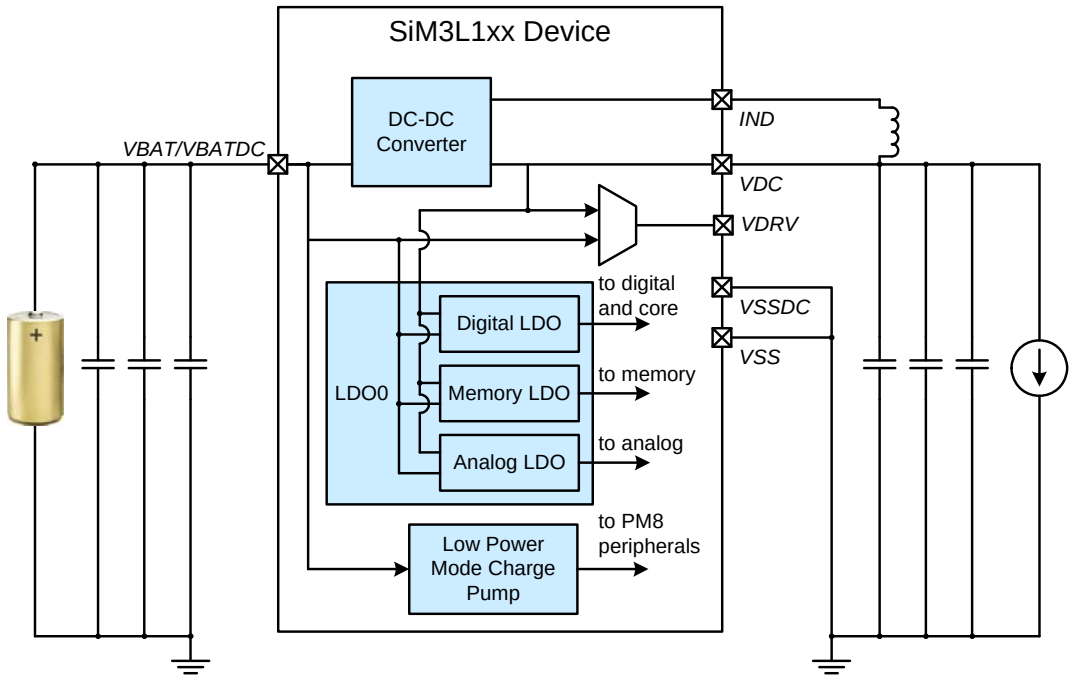

Figure 4.2. SiM3L1xx Power

4.1.1. DC-DC Buck Converter (DCDC0)

SiM3L1xx devices include an on-chip step-down dc-dc converter to efficiently utilize the energy stored in the battery, thus extending the operational life time. The dc-dc converter is a switching buck converter with a programmable output voltage that should be at least 0.45 V lower than the input battery voltage; if this criteria is not met and the converter can no longer operate, the output of the dc-dc converter automatically connects to the battery. The dc-dc converter can supply up to 100 mA and can be used to power the MCU and/or external devices in the system.

The dc-dc converter has a built in voltage reference and oscillator and will automatically limit or turn off the switching activity in case the peak inductor current rises beyond a safe limit or the output voltage rises above the programmed target value. This allows the dc-dc converter output to be safely overdriven by a secondary power source (when available) in order to preserve battery life. When enabled, the dc-dc converter can source current into the output capacitor, but cannot sink current.

The dc-dc converter includes the following features:

- Efficiently utilizes the energy stored in a battery, extending its operational lifetime.
- Input range: 1.8 to 3.8 V.
- Output range: 1.25 to 3.8 V in 50 mV (1.25–1.8 V) or 100 mV (1.8–3.8 V) steps.
- Supplies up to 100 mA.
- Includes a voltage reference and an oscillator.

4.3.1. PLL (PLL0)

The PLL module consists of a dedicated Digitally-Controlled Oscillator (DCO) that can be used in Free-Running mode without a reference frequency, Frequency-Locked to a reference frequency, or Phase-Locked to a reference frequency. The reference frequency for Frequency-Lock and Phase-Lock modes can use one of multiple sources (including the external oscillator) to provide maximum flexibility for different application needs. Because the PLL module generates its own clock, the DCO can be locked to a particular reference frequency and then moved to Free-Running mode to reduce system power and noise.

The PLL module includes the following features:

- Three output ranges with output frequencies ranging from 23 to 50 MHz.
- Multiple reference frequency inputs, including the RTC0 oscillator, Low Power Oscillator, and external oscillator.
- Three output modes: Free-Running Digitally-Controlled Oscillator, Frequency-Locked, and Phase-Locked.
- Able to sense the rising edge or falling edge of the reference source.
- DCO frequency LSB dithering to provide finer average output frequencies.
- Spectrum spreading to reduce generated system noise.
- Low jitter and fast lock times.\
- All output frequency updates (including dithering and spectrum spreading) can be temporarily suspended using the STALL bit during noise-sensitive measurements.

4.3.2. Low Power Oscillator (LPOSC0)

The Low Power Oscillator is the default AHB oscillator on SiM3L1xx devices and enables or disables automatically, as needed.

The default output frequency of this oscillator is factory calibrated to 20 MHz, and a divided 2.5 MHz version of this clock is also available as an AHB clock source.

The Low Power Oscillator has the following features:

- 20 MHz and divided 2.5 MHz frequencies available for the AHB clock.
- Automatically starts and stops as needed.

4.3.3. Low Frequency Oscillator (LFOSC0)

The low frequency oscillator (LFOSC) provides a low power internal clock source for the RTC0 timer and other peripherals on the device. No external components are required to use the low frequency oscillator, and the RTC1 and RTC2 pins do not need to be shorted together.

The Low Frequency Oscillator has the following features:

- 16.4 kHz output frequency.

4.3.4. External Oscillators (EXTOSC0)

The EXTOSC0 external oscillator circuit may drive an external crystal, ceramic resonator, capacitor, or RC network. A CMOS clock may also provide a clock input. The external oscillator output may be selected as the AHB clock or used to clock other modules independent of the AHB clock selection.

The External Oscillator control has the following features:

- Support for external crystal, resonator, RC, C, or CMOS oscillators.
- Support for external CMOS frequencies from 10 kHz to 50 MHz.
- Support for external crystal frequencies from 10 kHz to 25 MHz.
- Various drive strengths for flexible crystal oscillator support.
- Internal frequency divide-by-two option available.

4.4. Integrated LCD Controller (LCD0)

SiM3L1xx devices contain an LCD segment driver and on-chip bias generation that supports static, 2-mux, 3-mux and 4-mux LCDs with 1/2 or 1/3 bias. The on-chip charge pump with programmable output voltage allows software contrast control which is independent of the supply voltage. LCD timing is derived from the RTC timer clock (RTC0TCLK) to allow precise control over the refresh rate.

The SiM3L1xx devices use registers to store the enabled/disabled state of individual LCD segments. All LCD waveforms are generated on-chip based on the contents of these registers with flexible waveform control to reduce power consumption wherever possible. An LCD blinking function is also supported on a subset of LCD segments.

The LCD0 module has the following features:

- Up to 40 segment pins and 4 common pins.
- Supports LCDs with 1/2 or 1/3 bias.
- Includes an on-chip charge pump with programmable output that allows firmware to control the contrast independent of the supply voltage.
- The RTC timer clock (RTC0TCLK) determines the LCD timing and refresh rate.
- All LCD waveforms are generated on-chip based on the contents of the LCD0 registers with flexible waveform control.
- LCD segments can be placed in a discharge state for a configurable number of RTC clock cycles before switching to the next state to reduce power consumption due to display loading.
- Includes a VBAT monitor that can serve as a wakeup source for Power Mode 8.
- Supports four hardware auto-contrast modes: bypass, constant, minimum, and auto-bypass.
- Supports hardware blinking for up to 8 segments.

4.6. Counters/Timers

4.6.1. 32-bit Timer (TIMER0, TIMER1, TIMER2)

Each timer module is independent, and includes the following features:

- Operation as a single 32-bit or two independent 16-bit timers.
- Clocking options include the APB clock, the APB clock scaled using an 8-bit prescaler, the external oscillator, or falling edges on an external input pin (synchronized to the APB clock).
- Auto-reload functionality in both 32-bit and 16-bit modes.

TIMER0 and TIMER1 have the following features:

- Up/Down count capability, controlled by an external input pin.
- Rising and falling edge capture modes.
- Low or high pulse capture modes.
- Period and duty cycle capture mode.
- Square wave output mode, which is capable of toggling an external pin at a given rate with 50% duty cycle.
- 32- or 16-bit pulse-width modulation mode.

TIMER2 does not support the standard input/output features of TIMER0 and TIMER1. The TIMER2 EX signal is internally connected to the outputs of the PVTOSC0 oscillators. TIMER2 can use any of the counting modes that use EX as an input, including up/down mode, edge capture mode, and pulse capture mode. The TIMER2 CT signal is disconnected.

4.6.2. Enhanced Programmable Counter Array (EPCA0)

The Enhanced Programmable Counter Array (EPCA) module is a timer/counter system allowing for complex timing or waveform generation. Multiple modules run from the same main counter, allowing for synchronous output waveforms.

This module includes the following features:

- Three sets of channel pairs (six channels total) capable of generating complementary waveforms.
- Center- and edge-aligned waveform generation.
- Programmable dead times that ensure channel pairs are never active at the same time.
- Programmable clock divisor and multiple options for clock source selection.
- Waveform update scheduling.
- Option to function while the core is inactive.
- Multiple synchronization triggers.
- Pulse-Width Modulation (PWM) waveform generation.

Table 6.2. Pin Definitions and Alternate Functions for SiM3L1x6 (Continued)

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB4.0	Standard I/O	24	VIO		✓	COM0.1			
PB4.1	Standard I/O	23	VIO		✓	COM0.0			
PB4.2	Standard I/O	22	VIO		✓	LCD0.10			ADC0.19
PB4.3	Standard I/O	21	VIO		✓	LCD0.9			
PB4.4	Standard I/O	20	VIO		✓	LCD0.8			
PB4.5	Standard I/O	19	VIO		✓	LCD0.7			
PB4.6	Standard I/O	18	VIO		✓	LCD0.6		PMU_Asleep	
PB4.7	Standard I/O	17	VIO		✓	LCD0.5			
PB4.8/ETM3	Standard I/O / ETM	16	VIO		✓	LCD0.4			
PB4.9/ETM2	Standard I/O / ETM	15	VIO		✓	LCD0.3			
PB4.10/ ETM1	Standard I/O / ETM	14	VIO		✓	LCD0.2			
PB4.11/ ETM0	Standard I/O / ETM	13	VIO		✓	LCD0.1			
PB4.12/ TRACECLK	Standard I/O / ETM	12	VIO		✓	LCD0.0			

Table 6.4. TQFP-80 Package Dimensions

Dimension	Min	Nominal	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.20	0.27
c	0.09	—	0.20
D	14.00 BSC		
D1	12.00 BSC		
e	0.50 BSC		
E	14.00 BSC		
E1	12.00 BSC		
L	0.45	0.60	0.75
L1	1.00 Ref		
Θ	0°	3.5°	7°
aaa	0.20		
bbb	0.20		
ccc	0.08		
ddd	0.08		
eee	0.05		

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant ADD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.4.1. TQFP-80 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.4.2. TQFP-80 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.

6.4.3. TQFP-80 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.6. TQFP-64 Package Specifications

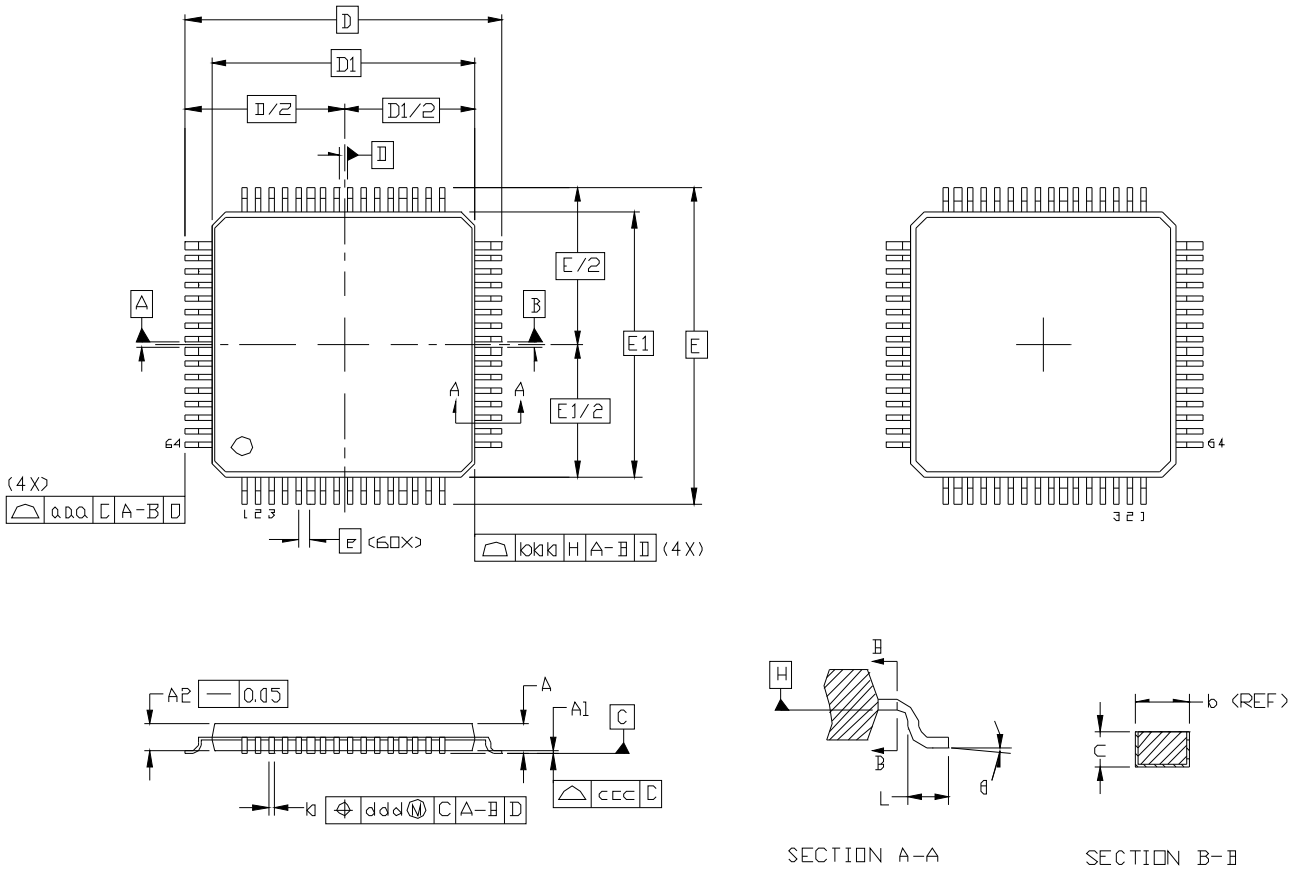

Figure 6.9. TQFP-64 Package Drawing

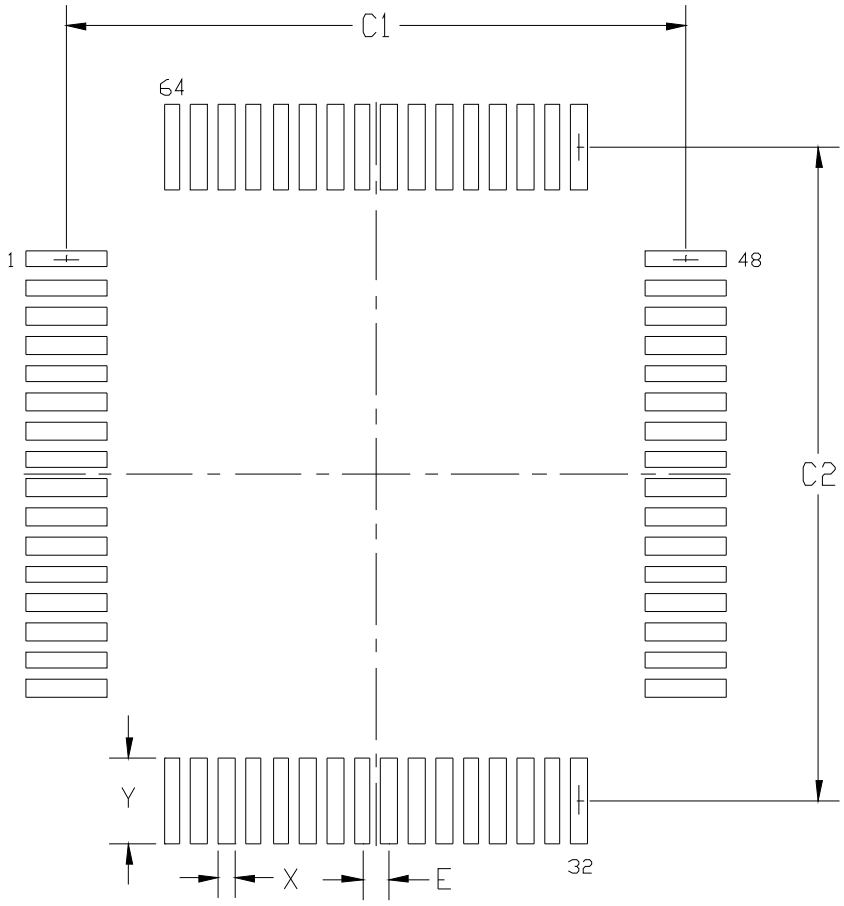

Figure 6.10. TQFP-64 Landing Diagram

Table 6.9. TQFP-64 Landing Diagram Dimensions

Dimension	Min	Max
C1	11.30	11.40
C2	11.30	11.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

6.6.1. TQFP-64 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.6.2. TQFP-64 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.

6.6.3. TQFP-64 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

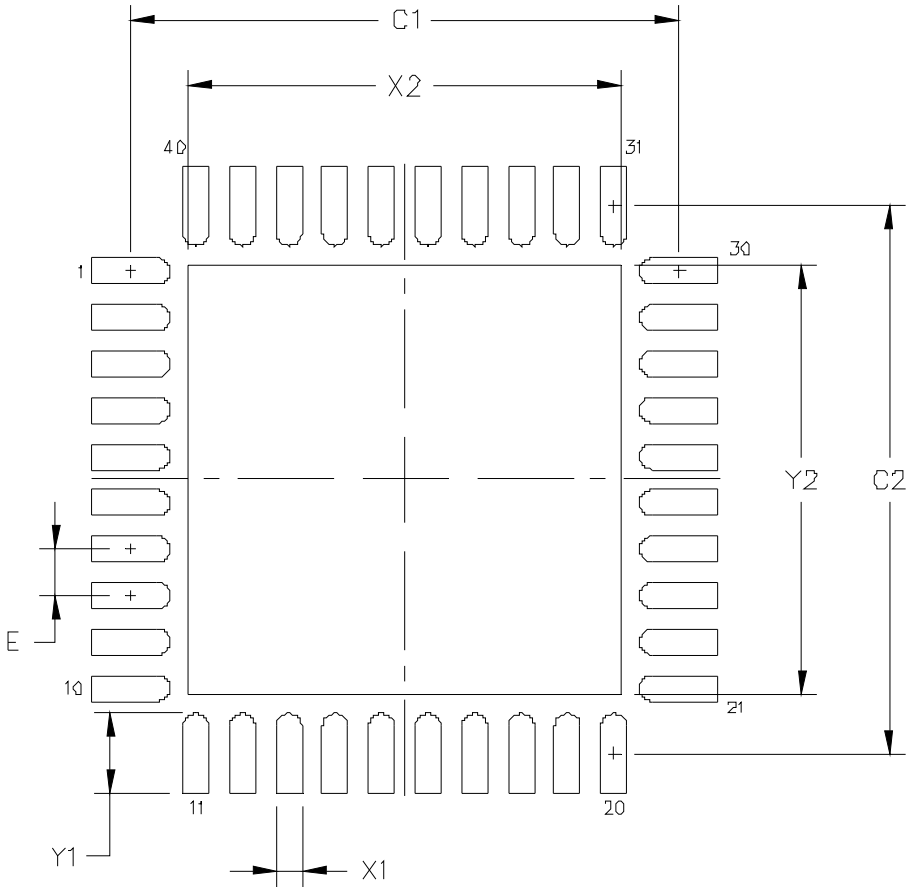

Figure 6.12. QFN-40 Landing Diagram

Table 6.11. QFN-40 Landing Diagram Dimensions

Dimension	mm
C1	5.90
C2	5.90
E	0.50
X1	0.30
Y1	0.85
X2	4.65
Y2	4.65

Notes:
1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.