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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	62
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 24x10/12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/sim3l167-c-gq

1. Related Documents and Conventions

1.1. Related Documents

This data sheet accompanies several documents to provide the complete description of the SiM3L1xx devices.

1.1.1. SiM3L1xx Reference Manual

The Silicon Laboratories SiM3L1xx Reference Manual provides the detailed description for each peripheral on the SiM3L1xx devices.

1.1.2. Hardware Access Layer (HAL) API Description

The Silicon Laboratories Hardware Access Layer (HAL) API provides C-language functions to modify and read each bit in the SiM3L1xx devices. This description can be found in the SiM3xxxx HAL API Reference Manual.

1.1.3. ARM Cortex-M3 Reference Manual

The ARM-specific features like the Nested Vectored Interrupt Controller are described in the ARM Cortex-M3 reference documentation. The online reference manual can be found here:
http://infocenter.arm.com/help/topic/com.arm.doc.subset.cortexm3/index.html#cortexm3.

1.2. Conventions

The block diagrams in this document use the following formatting conventions:

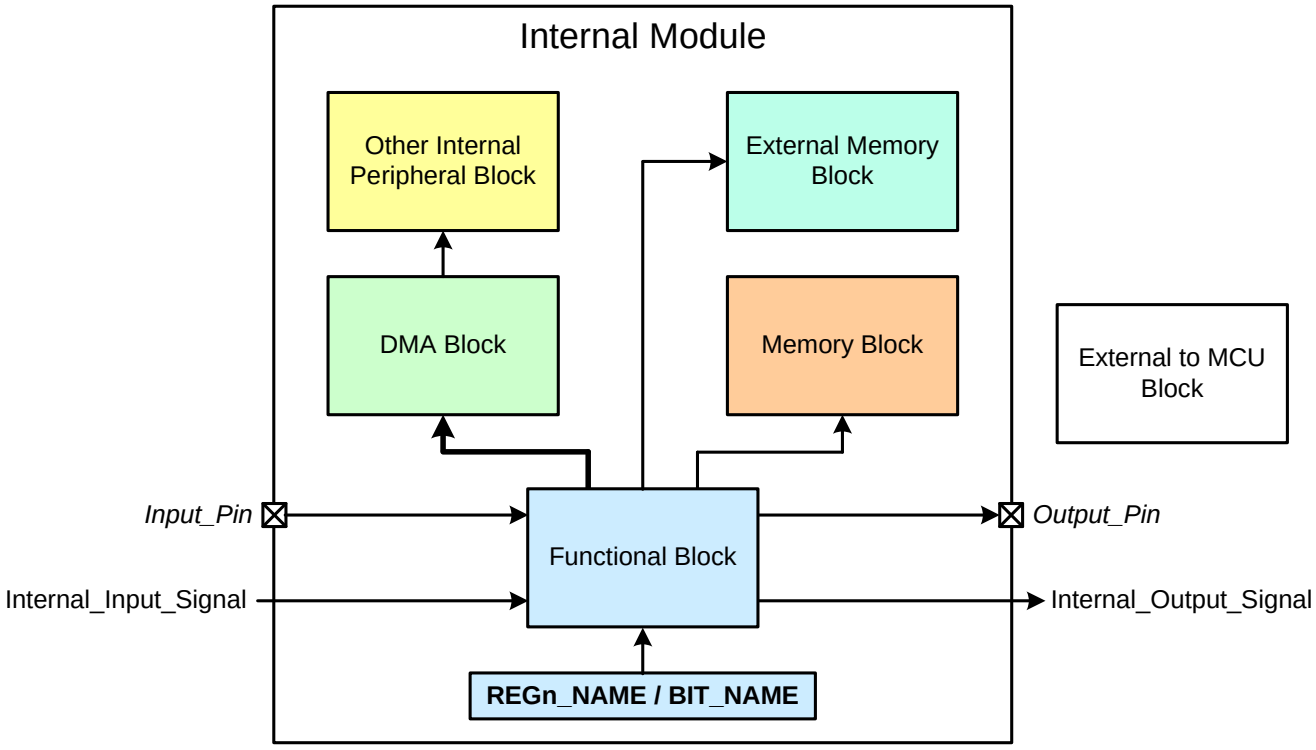

Figure 1.1. Block Diagram Conventions

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 1[1,2,3,4]—Full speed with code executing from RAM, peripheral clocks ON	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	13.4	16.6	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	4.7	—	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	810	—	µA
Power Mode 1[1,2,3,4]—Full speed with code executing from RAM, peripheral clocks OFF	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	9.4	12.5	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	3.3	—	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	630	—	µA
Power Mode 1[1,2,3,4]—Full speed with code executing from RAM, LDOs powered by dc-dc at 1.9 V, peripheral clocks OFF	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz V_{BAT} = 3.3 V	—	7.05	—	mA
		F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz V_{BAT} = 3.8 V	—	6.3	—	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz V_{BAT} = 3.3 V	—	2.75	—	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz V_{BAT} = 3.8 V	—	2.6	—	mA
Power Mode 2[1,2,3,4,5]—Core halted with peripheral clocks ON	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	7.6	11.3	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	2.75	—	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	575	—	µA

Notes:

1. Currents are additive. For example, where I_{BAT} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded I_{VIO} is included in all I_{BAT} PM8 production test measurements.

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Advanced Capture Counter (ACCTR0), LC Dual or Quadrature Mode, Relative to Sampling Frequency[9]	I_{ACCTR}	V_{BAT} = 2.4 V, T_A = 25 °C, CPMD = 01	—	1.39	—	nA/Hz
		V_{BAT} = 3.8 V, T_A = 25 °C, CPMD = 01	—	1.89	—	nA/Hz
		V_{BAT} = 2.4 V, T_A = 25 °C, CPMD = 10	—	2.08	—	nA/Hz
		V_{BAT} = 3.8 V, T_A = 25 °C, CPMD = 10	—	2.59	—	nA/Hz
		V_{BAT} = 2.4 V, T_A = 25 °C, CPMD = 11	—	3.47	—	nA/Hz
		V_{BAT} = 3.8 V, T_A = 25 °C, CPMD = 11	—	4.03	—	nA/Hz
Analog Peripheral Supply Currents						
PLL0 Oscillator (PLL0OSC)	I_{PLLOSC}	Operating at 49 MHz	—	1.4	1.6	mA
Low-Power Oscillator (LPOSC0)	I_{LPOSC}	Operating at 20 MHz	—	25	—	µA
		Operating at 2.5 MHz	—	25	—	µA
Low-Frequency Oscillator (LFOSC0)	I_{LFOSC}	Operating at 16.4 kHz	—	190	310	nA
External Oscillator (EXTOSC0)	I_{EXTOSC}	FREQCN = 111	—	3.8	4.5	mA
		FREQCN = 110	—	840	960	µA
		FREQCN = 101	—	185	230	µA
		FREQCN = 100	—	65	80	µA
		FREQCN = 011	—	25	30	µA
		FREQCN = 010	—	10	13	µA
		FREQCN = 001	—	5	7	µA
		FREQCN = 000	—	3	5	µA

Notes:

1. Currents are additive. For example, where I_{BAT} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded I_{VIO} is included in all I_{BAT} PM8 production test measurements.

Table 3.5. On-Chip Regulators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC-DC Buck Converter						
Input Voltage Range	V_{DCIN}		1.8	—	3.8	V
Input Supply to Output Voltage Differential (for regulation)	V_{DCREG}		0.45	—	—	V
Output Voltage Range	V_{DCOUT}		1.25	—	3.8	V
Output Voltage Accuracy	V_{DCACC}		—	±25	—	mV
Output Current	I_{DCOUT}		—	—	90	mA
Inductor Value[1]	L_{DC}		0.47	0.56	0.68	µH
Inductor Current Rating	I_{LDC}	I_{load} < 50 mA	450	—	—	mA
		I_{load} > 50 mA	550	—	—	mA
Output Capacitor Value	C_{DCOUT}		1	2.2	10	µF
Input Capacitor Value[2]	C_{DCIN}		—	4.7	—	µF
Load Regulation	R_{load}		—	0.03	—	mV/mA
Maximum DC Load Current During Startup	I_{DCMAX}		—	—	5	mA
Switching Clock Frequency	F_{DCCLK}		1.9	2.9	3.8	MHz
Local Oscillator Frequency	F_{DCOSC}		2.4	2.9	3.4	MHz
LDO Regulators						
Input Voltage Range[3]	V_{LDOIN}	Sourced from VBAT	1.8	—	3.8	V
		Sourced from VDC	1.9	—	3.8	V
Output Voltage Range[4]	V_{LDO}		0.8	—	1.9	V
LDO Output Voltage Accuracy	V_{LDOACC}		—	±25	—	mV
Output Settings in PM8 (All LDOs)	V_{LDO}	1.8 V ≤ V_{BAT} ≤ 2.9 V	1.5			V
		1.95 V ≤ V_{BAT} ≤ 3.5 V	1.8			V
		2.0 V ≤ V_{BAT} ≤ 3.8 V	1.9			V

Notes:

1. See reference manual for recommended inductors.
2. Recommended: X7R or X5R ceramic capacitors with low ESR. Example: Murata GRM21BR71C225K with ESR < 10 mΩ (@ frequency > 1 MHz).
3. Input voltage specification accounts for the internal LDO dropout voltage under the maximum load condition to ensure that the LDO output voltage will remain at a valid level as long as V_{LDOIN} is at or above the specified minimum.
4. The memory LDO output should always be set equal to or lower than the output of the analog LDO. When lowering both LDOs (for example to go into PM8 under low supply conditions), first adjust the memory LDO and then the analog LDO. When raising the output of both LDOs, adjust the analog LDO before adjusting the memory LDO.
5. Output range represents the programmable output range, and does not reflect the minimum voltage under all conditions. Dropout when the input supply is close to the output setting is normal, and accounted for.
6. Analog peripheral specifications assume a 1.8 V output on the analog LDO.

Table 3.7. Internal Oscillators (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RTC0 Oscillator (RTC0OSC)						
Missing Clock Detector Trigger Frequency	f_{RTCMCD}		—	8	15	kHz
RTC External Input CMOS Clock Frequency	$f_{RTCEXTCLK}$		0	—	40	kHz
RTC Robust Duty Cycle Range	DC_{RTC}		25	—	55	%

Table 3.8. External Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency	f_{CMOS}		0*	—	50	MHz
External Crystal Frequency	f_{XTAL}		0.01	—	25	MHz
External Input CMOS Clock High Time	t_{CMOSH}		9	—	—	ns
External Input CMOS Clock Low Time	t_{CMOSL}		9	—	—	ns
Low Power Mode Charge Pump Supply Range (input from V_{BAT})	V_{BAT}		2.4	—	3.8	V
***Note:** Minimum of 10 kHz when debugging.						

Table 3.10. IDAC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static Performance						
Resolution	N_{bits}			10		Bits
Integral Nonlinearity	INL		—	±0.5	±2	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL		—	±0.5	±1	LSB
Output Compliance Range	V_{OCR}		—	—	V_{BAT} – 1.0	V
Full Scale Output Current	I_{OUT}	2 mA Range, T_A = 25 °C	1.98	2.046	2.1	mA
		1 mA Range, T_A = 25 °C	0.99	1.023	1.05	mA
		0.5 mA Range, T_A = 25 °C	491	511.5	525	µA
Offset Error	E_{OFF}		—	250	—	nA
Full Scale Error Tempco	TC_{FS}	2 mA Range	—	100	—	ppm/°C
VBAT Power Supply Rejection Ratio		2 mA Range	—	–220	—	ppm/V
Test Load Impedance (to V_{SS})	R_{TEST}		—	1	—	kΩ
Dynamic Performance						
Output Settling Time to 1/2 LSB		min output to max output	—	1.2	—	µs
Startup Time			—	3	—	µs

Table 3.12. Voltage Reference Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage	V_{REFFS}	–40 to +85 °C, V_{BAT} = 1.8–3.8 V	1.6	1.65	1.7	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{REFFS}		—	—	1.5	µs
Power Supply Rejection	$PSRR_{REFFS}$		—	400	—	ppm/V
Internal Precision Reference						
Valid Supply Range	V_{BAT}	VREF2X = 0	1.8	—	3.8	V
		VREF2X = 1	2.7	—	3.8	V
Output Voltage	V_{REFP}	25 °C ambient, VREF2X = 0	1.17	1.2	1.23	V
		25 °C ambient, VREF2X = 1	2.35	2.4	2.45	V
Short-Circuit Current	I_{SC}		—	—	10	mA
Temperature Coefficient	TC_{VREFP}		—	35	—	ppm/°C
Load Regulation	LR_{VREFP}	Load = 0 to 200 µA to VREFGND	—	4.5	—	ppm/µA
Load Capacitor	C_{VREFP}	Load = 0 to 200 µA to VREFGND	0.1	—	—	µF
Turn-on Time	$t_{VREFPON}$	4.7 µF tantalum, 0.1 µF ceramic bypass	—	3.8	—	ms
		0.1 µF ceramic bypass	—	200	—	µs
Power Supply Rejection	$PSRR_{VREFP}$	VREF2X = 0	—	320	—	ppm/V
		VREF2X = 1	—	560	—	ppm/V
External Reference						
Input Current	I_{EXTREF}	Sample Rate = 250 ksps; VREF = 3.0 V	—	5.25	—	µA

Table 3.13. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	V_{OFF}	T_A = 0 °C	—	760	—	mV
Offset Error*	E_{OFF}	T_A = 0 °C	—	±14	—	mV
Slope	M		—	2.77	—	mV/°C
Slope Error*	E_M		—	±25	—	µV/°C
Linearity			—	1	—	°C
Turn-on Time			—	1.8	—	µs

***Note:** Absolute input pin voltage is limited by the lower of the supply at VBAT and VIO.

Table 3.14. Comparator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CMPMD = 00 (Highest Speed)	t_{RESP0}	+100 mV Differential	—	100	—	ns
		–100 mV Differential	—	150	—	ns
Response Time, CMPMD = 11 (Lowest Power)	t_{RESP3}	+100 mV Differential	—	1.4	—	µs
		–100 mV Differential	—	3.5	—	µs
Positive Hysteresis Mode 0 (CPMD = 00)	HYS_{CP+}	CMPHYP = 00	—	0.37	—	mV
		CMPHYP = 01	—	7.9	—	mV
		CMPHYP = 10	—	16.7	—	mV
		CMPHYP = 11	—	32.8	—	mV
Negative Hysteresis Mode 0 (CPMD = 00)	HYS_{CP-}	CMPHYN = 00	—	0.37	—	mV
		CMPHYN = 01	—	–7.9	—	mV
		CMPHYN = 10	—	–16.1	—	mV
		CMPHYN = 11	—	–32.7	—	mV
Positive Hysteresis Mode 1 (CPMD = 01)	HYS_{CP+}	CMPHYP = 00	—	0.47	—	mV
		CMPHYP = 01	—	5.85	—	mV
		CMPHYP = 10	—	12	—	mV
		CMPHYP = 11	—	24.4	—	mV
Negative Hysteresis Mode 1 (CPMD = 01)	HYS_{CP-}	CMPHYN = 00	—	0.47	—	mV
		CMPHYN = 01	—	–6.0	—	mV
		CMPHYN = 10	—	–12.1	—	mV
		CMPHYN = 11	—	–24.6	—	mV
Positive Hysteresis Mode 2 (CPMD = 10)	HYS_{CP+}	CMPHYP = 00	—	0.66	—	mV
		CMPHYP = 01	—	4.55	—	mV
		CMPHYP = 10	—	9.3	—	mV
		CMPHYP = 11	—	19	—	mV
Negative Hysteresis Mode 2 (CPMD = 10)	HYS_{CP-}	CMPHYN = 00	—	0.6	—	mV
		CMPHYN = 01	—	–4.5	—	mV
		CMPHYN = 10	—	–9.5	—	mV
		CMPHYN = 11	—	–19	—	mV

Table 3.16. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (PB0, PB1, PB3, or PB4)	V_{OH}	Low Drive, I_{OH} = –1 mA	V_{IO} – 0.7	—	—	V
		Low Drive, I_{OH} = –10 µA	V_{IO} – 0.1	—	—	V
		High Drive, I_{OH} = –3 mA	V_{IO} – 0.7	—	—	V
		High Drive, I_{OH} = –10 µA	V_{IO} – 0.1	—	—	V
Output High Voltage (PB2)	V_{OH}	Low Drive, I_{OH} = –1 mA	V_{IORF} – 0.7	—	—	V
		Low Drive, I_{OH} = –10 µA	V_{IORF} – 0.1	—	—	V
		High Drive, I_{OH} = –3 mA	V_{IORF} – 0.7	—	—	V
		High Drive, I_{OH} = –10 µA	V_{IORF} – 0.1	—	—	V
Output Low Voltage (any Port I/O pin or $\overline{\text{RESET}}$[1])	V_{OL}	Low Drive, I_{OL} = 1.4 mA	—	—	0.6	V
		Low Drive, I_{OL} = 10 µA	—	—	0.1	V
		High Drive, I_{OL} = 8.5 mA	—	—	0.6	V
		High Drive, I_{OL} = 10 µA	—	—	0.1	V
Input High Voltage (PB0, PB1, PB3, PB4 or $\overline{\text{RESET}}$)	V_{IH}		V_{IO} – 0.6	—	—	V
Input High Voltage (PB2)	V_{IH}		V_{IORF} – 0.6	—	—	V
Input Low Voltage any Port I/O pin or $\overline{\text{RESET}}$)	V_{IL}		—	—	0.6	V
Weak Pull-Up Current[2] (per pin)	I_{PU}	V_{IO} or V_{IORF} = 1.8	-6	-3.5	-2	µA
		V_{IO} or V_{IORF} = 3.8	-32	-20	-10	µA
Input Leakage (Pullups off or Analog)	I_{LK}	$0 \le V_{IN} \le V_{IO}$ or V_{IORF}	-1	—	1	µA

Notes:

1. Specifications for $\overline{\text{RESET}}$ V_{OL} adhere to the low drive setting.
2. On the SiM3L1x6 and SiM3L1x4 devices, the SWV pin will have double the weak pull-up current specified whenever the device is held in reset.

4.3. Clocking

The SiM3L1xx devices have two system clocks: AHB and APB. The AHB clock services memory peripherals and is derived from one of seven sources: the RTC timer clock (RTC0TCLK), the Low Frequency Oscillator, the Low Power Oscillator, the divided Low Power Oscillator, the External Oscillator, the PLL0 Oscillator, and the VIORFCLK pin input. In addition, a divider for the AHB clock provides flexible clock options for the device. The APB clock services data peripherals and is synchronized with the AHB clock. The APB clock can be equal to the AHB clock or set to the AHB clock divided by two.

The Clock Control module on SiM3L1xx devices allows the AHB and APB clocks to be turned off to unused peripherals to save system power. Any registers in a peripheral with disabled clocks will be unable to be accessed until the clocks are enabled. Most peripherals have clocks off by default after a power-on reset.

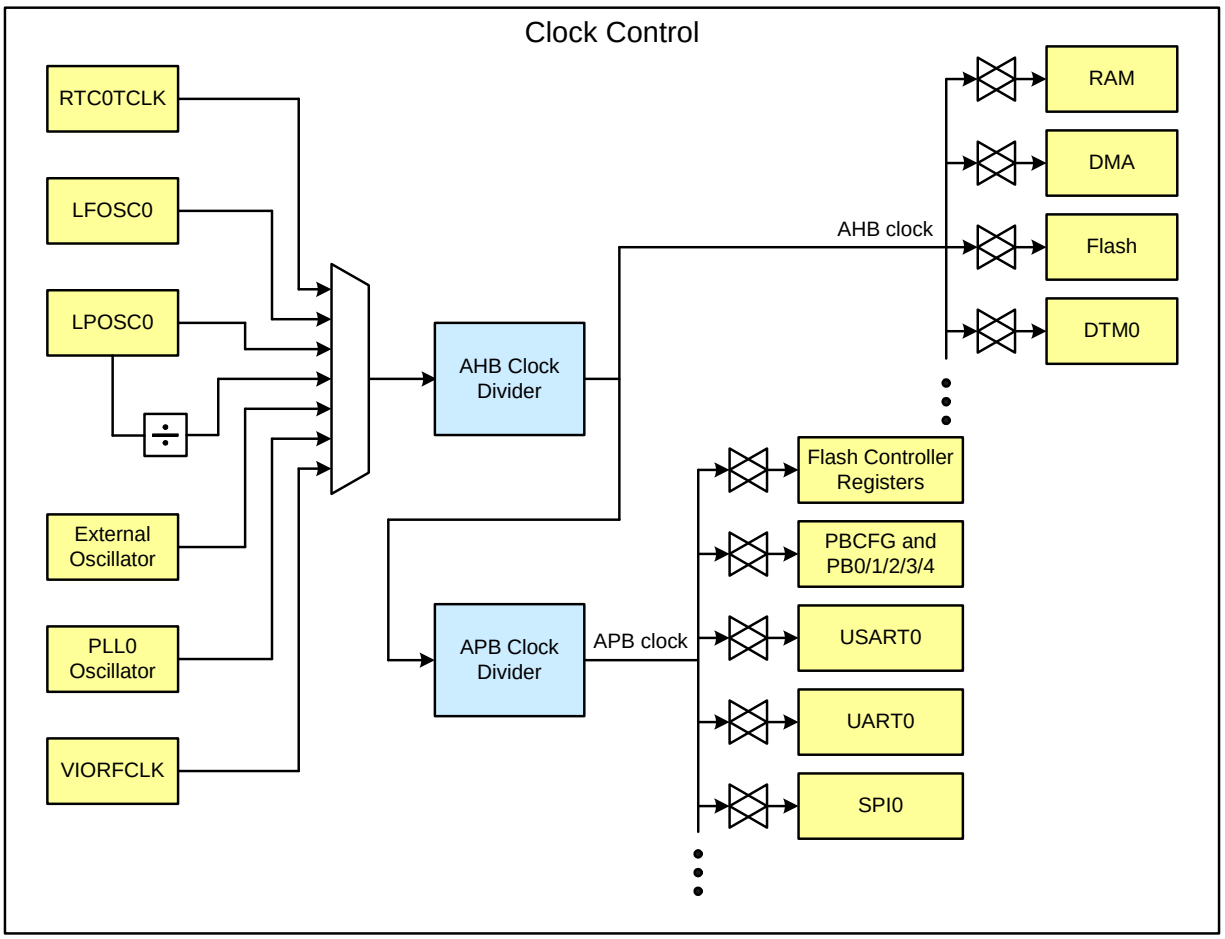

Figure 4.3. SiM3L1xx Clocking

4.4. Integrated LCD Controller (LCD0)

SiM3L1xx devices contain an LCD segment driver and on-chip bias generation that supports static, 2-mux, 3-mux and 4-mux LCDs with 1/2 or 1/3 bias. The on-chip charge pump with programmable output voltage allows software contrast control which is independent of the supply voltage. LCD timing is derived from the RTC timer clock (RTC0TCLK) to allow precise control over the refresh rate.

The SiM3L1xx devices use registers to store the enabled/disabled state of individual LCD segments. All LCD waveforms are generated on-chip based on the contents of these registers with flexible waveform control to reduce power consumption wherever possible. An LCD blinking function is also supported on a subset of LCD segments.

The LCD0 module has the following features:

- Up to 40 segment pins and 4 common pins.
- Supports LCDs with 1/2 or 1/3 bias.
- Includes an on-chip charge pump with programmable output that allows firmware to control the contrast independent of the supply voltage.
- The RTC timer clock (RTC0TCLK) determines the LCD timing and refresh rate.
- All LCD waveforms are generated on-chip based on the contents of the LCD0 registers with flexible waveform control.
- LCD segments can be placed in a discharge state for a configurable number of RTC clock cycles before switching to the next state to reduce power consumption due to display loading.
- Includes a VBAT monitor that can serve as a wakeup source for Power Mode 8.
- Supports four hardware auto-contrast modes: bypass, constant, minimum, and auto-bypass.
- Supports hardware blinking for up to 8 segments.

5. Ordering Information

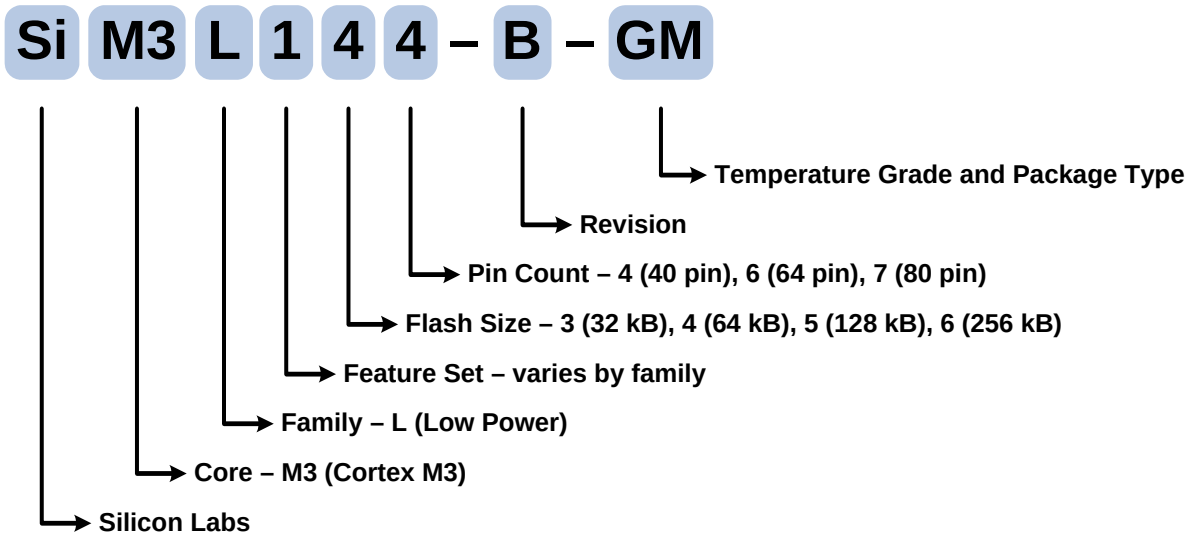

Figure 5.1. SiM3L1xx Part Numbering

All devices in the SiM3L1xx family have the following features:

- **Core:** ARM Cortex-M3 with maximum operating frequency of 50 MHz.
- **PLL.**
- **10-Channel DMA Controller.**
- **128/192/256-bit AES.**
- **16/32-bit CRC.**
- **Encoder/Decoder.**
- **DC-DC Buck Converter.**
- **Timers:** 3 x 32-bit (6 x 16-bit).
- **Real-Time Clock.**
- **Low-Power Timer.**
- **PCA:** 1 x 6 channels (Enhanced)
- **ADC:** 12-bit 250 ksps (10-bit 1 Msps) SAR.
- **DAC:** 10-bit IDAC.
- **Temperature Sensor.**
- **Internal VREF.**
- **Comparator:** 2 x low current.
- **Serial Buses:** 2 x USART, 2 x SPI, 1 x I2C

Additionally, all devices in the SiM3L1xx family include the low power mode advanced capture counter (ACCTR0), though the smaller packages (SiM3L1x4) only support some of the external inputs and outputs.

Table 6.1. Pin Definitions and Alternate Functions for SiM3L1x7

Pin Name	Type	Pin Numbers (TQFP-80)	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
VSS	Ground	12 31 52 71							
VSSDC	Ground (DC-DC)	12							
VIO	Power (I/O)	7 30 68							
VIORF	Power (RF I/O)	8							
VBAT/ VBATDC		10							
VDRV		9							
VDC		13							
VLCD	Power (LCD Charge Pump)	67							
IND	DC-DC Inductor	11							
$\overline{\text{RESET}}$	Active-low Reset	72							
TCK/ SWCLK	JTAG / Serial Wire	6							
TMS/ SWDIO	JTAG / Serial Wire	5							
RTC1	RTC Oscillator Input	70							
RTC2	RTC Oscillator Output	69							

Table 6.1. Pin Definitions and Alternate Functions for SiM3L1x7 (Continued)

Pin Name	Type	Pin Numbers (TQFP-80)	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB0.0	Standard I/O	4	VIO	✓	✓		✓	INT0.0 WAKE.0	ADC0.20 VREF CMP0P.0
PB0.1	Standard I/O	3	VIO	✓	✓		✓	INT0.1 WAKE.1	ADC0.21 VREFGND CMP0N.0
PB0.2	Standard I/O	2	VIO	✓	✓		✓	INT0.2 WAKE.2	ADC0.22 CMP1P.0 XTAL2
PB0.3	Standard I/O	1	VIO	✓	✓		✓	INT0.3 WAKE.3	ADC0.23 CMP1N.0 XTAL1
PB0.4	Standard I/O	80	VIO	✓	✓		✓	INT0.4 WAKE.4	ADC0.0 CMP0P.1 IDAC0
PB0.5	Standard I/O	79	VIO	✓	✓		✓	INT0.5 WAKE.5 ACCTR0_STOP0	ACCTR0_IN0
PB0.6	Standard I/O	78	VIO	✓	✓		✓	INT0.6 WAKE.6 ACCTR0_STOP1	ACCTR0_IN1
PB0.7	Standard I/O	77	VIO	✓	✓		✓	INT0.7 WAKE.7	ACCTR0_LCIN0
PB0.8	Standard I/O	76	VIO	✓	✓		✓	LPT0T0 LPT0OUT0 INT0.8 WAKE.8	ACCTR0_LCIN1

Table 6.1. Pin Definitions and Alternate Functions for SiM3L1x7 (Continued)

Pin Name	Type	Pin Numbers (TQFP-80)	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB3.4	Standard I/O	43	VIO	✓	✓	LCD0.23		INT1.12	CMP0P.6
PB3.5	Standard I/O	42	VIO	✓	✓	LCD0.22		INT1.13	CMP0N.6
PB3.6	Standard I/O	41	VIO	✓	✓	LCD0.21		INT1.14	CMP1P.6
PB3.7	Standard I/O	40	VIO	✓	✓	LCD0.20		INT1.15	CMP1N.6
PB3.8	Standard I/O	39	VIO		✓	LCD0.19			CMP0P.7
PB3.9	Standard I/O	38	VIO		✓	LCD0.18			CMP0N.7
PB3.10	Standard I/O	37	VIO		✓	LCD0.17			CMP1P.7
PB3.11	Standard I/O	36	VIO		✓	LCD0.16			CMP1N.7
PB3.12	Standard I/O	35	VIO		✓	LCD0.15			ADC0.18
PB3.13	Standard I/O	34	VIO		✓	LCD0.14			ADC0.19
PB3.14	Standard I/O	33	VIO		✓	COM0.3			
PB3.15	Standard I/O	32	VIO		✓	COM0.2			
PB4.0	Standard I/O	29	VIO		✓	COM0.1			
PB4.1	Standard I/O	28	VIO		✓	COM0.0			
PB4.2	Standard I/O	27	VIO		✓	LCD0.13			
PB4.3	Standard I/O	26	VIO		✓	LCD0.12			
PB4.4	Standard I/O	25	VIO		✓	LCD0.11			
PB4.5	Standard I/O	24	VIO		✓	LCD0.10			
PB4.6	Standard I/O	23	VIO		✓	LCD0.9		PMU_Asleep	
PB4.7	Standard I/O	22	VIO		✓	LCD0.8			
PB4.8	Standard I/O	21	VIO		✓	LCD0.7			

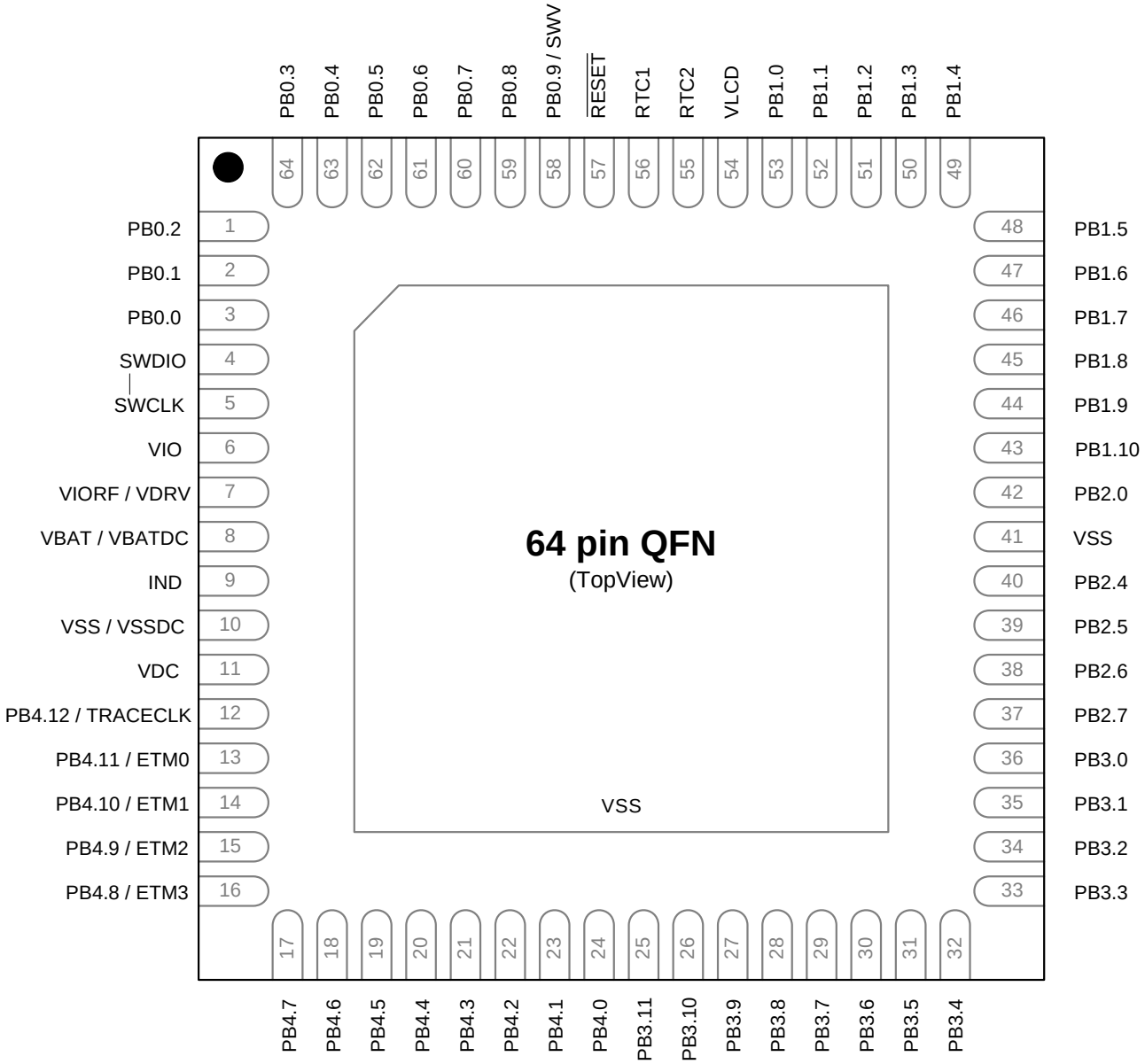

Figure 6.3. SiM3L1x6-GM Pinout

6.3. SiM3L1x4 Pin Definitions

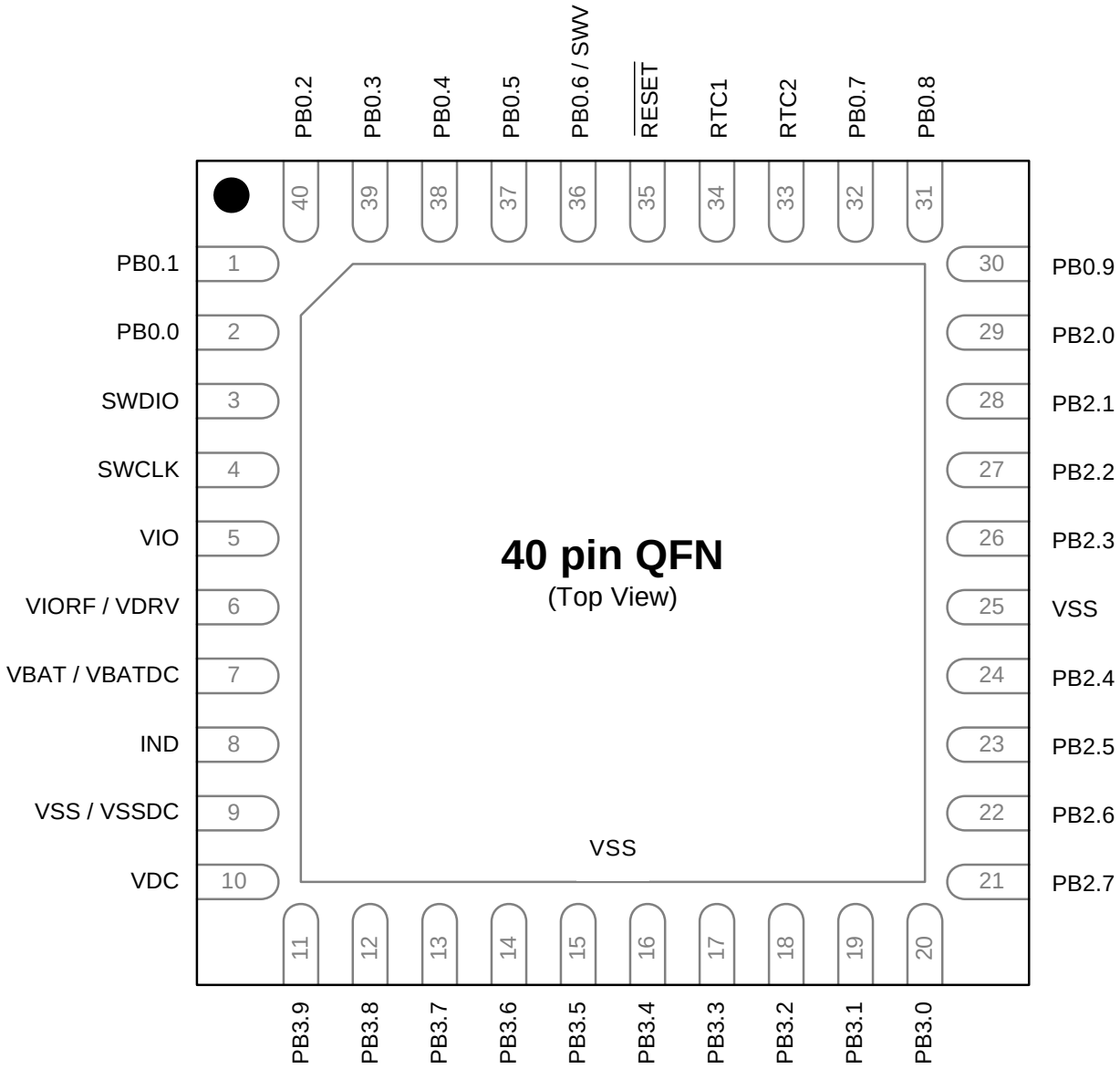

Figure 6.4. SiM3L1x4-GM Pinout

Table 6.3. Pin Definitions and Alternate Functions for SiM3L1x4 (Continued)

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB2.1	Standard I/O	28	VIORF	XBR0	✓		LPT0T9 INT1.1 WAKE.13 VIORFCLK	ADC0.3 CMP0N.4
PB2.2	Standard I/O	27	VIORF	XBR0	✓		LPT0T10 INT1.2 WAKE.14	ADC0.4 CMP1P.4
PB2.3	Standard I/O	26	VIORF	XBR0	✓		LPT0T11 INT1.3 WAKE.15	ADC0.5 CMP1N.4
PB2.4	Standard I/O	24	VIORF	XBR0	✓		LPT0T12 INT1.4 SPI1_SCLK	ADC0.6 CMP0P.5
PB2.5	Standard I/O	23	VIORF	XBR0	✓		LPT0T13 INT1.5 SPI1_MISO	ADC0.7 CMP0N.5
PB2.6	Standard I/O	22	VIORF	XBR0	✓		LPT0T14 INT1.6 SPI1_MOSI	ADC0.8 CMP1P.5
PB2.7	Standard I/O	21	VIORF	XBR0	✓		INT1.7 SPI1_NSS	ADC0.9 CMP1N.5
PB3.0	Standard I/O	20	VIO	XBR0	✓		INT1.8	CMP0N.7
PB3.1	Standard I/O	19	VIO	XBR0	✓		INT1.9	CMP1P.7
PB3.2	Standard I/O	18	VIO	XBR0	✓		INT1.10	CMP1N.7
PB3.3	Standard I/O	17	VIO	XBR0	✓		INT1.11	ADC0.10
PB3.4	Standard I/O	16	VIO	XBR0	✓		INT1.12	ADC0.11
PB3.5	Standard I/O	15	VIO	XBR0	✓		INT1.13	ADC0.12

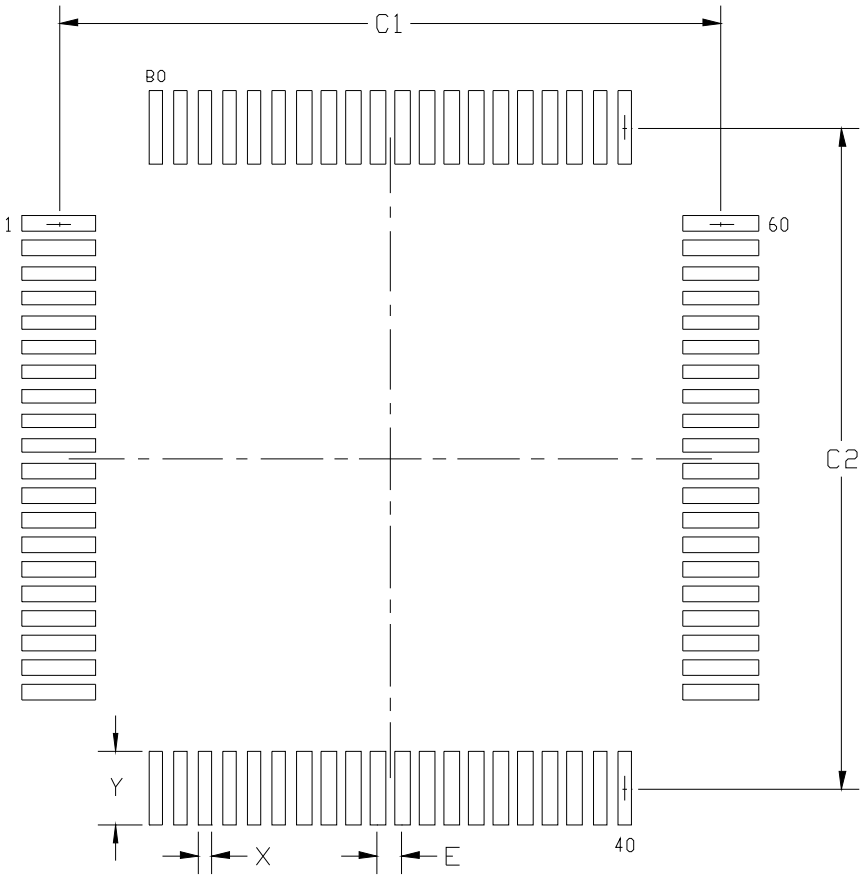

Figure 6.6. TQFP-80 Landing Diagram

Table 6.5. TQFP-80 Landing Diagram Dimensions

Dimension	Min	Max
C1	13.30	13.40
C2	13.30	13.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

6.6.1. TQFP-64 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.6.2. TQFP-64 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.

6.6.3. TQFP-64 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.