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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | I²C, IrDA, SmartCard, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT |
| Number of I/O | 62 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.8V |
| Data Converters | A/D 24x10/12b; D/A 1x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 80-TQFP |
| Supplier Device Package | 80-TQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/sim3l167-c-gqr |

# 2. Typical Connection Diagrams

This section provides typical connection diagrams for SiM3L1xx devices.

## 2.1. Power

Figure 2.1 shows a typical connection diagram for the power pins of the SiM3L1xx devices when the dc-dc buck converter is not used.

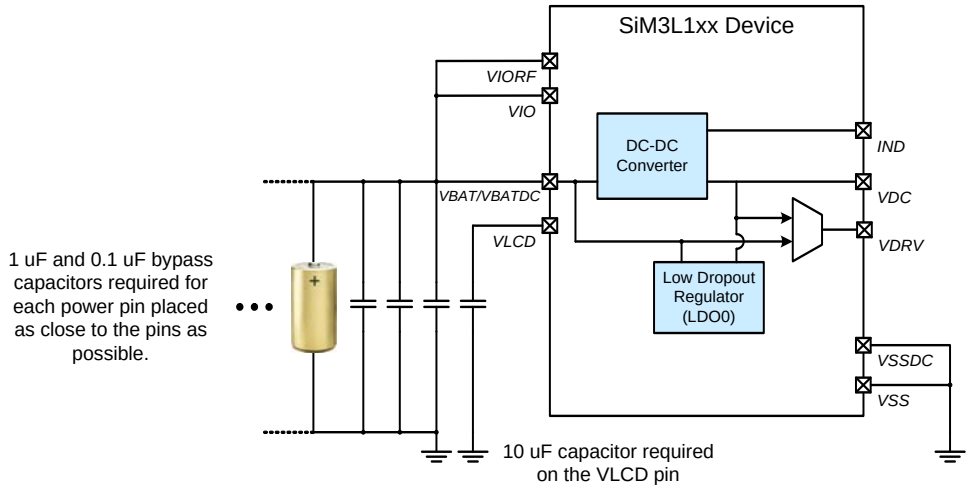


**Figure 2.1. Connection Diagram with DC-DC Converter Unused**

Figure 2.2 shows a typical connection diagram for the power pins of the SiM3L1xx devices when the internal dc-dc buck converter is in use and I/O are powered directly from the battery.

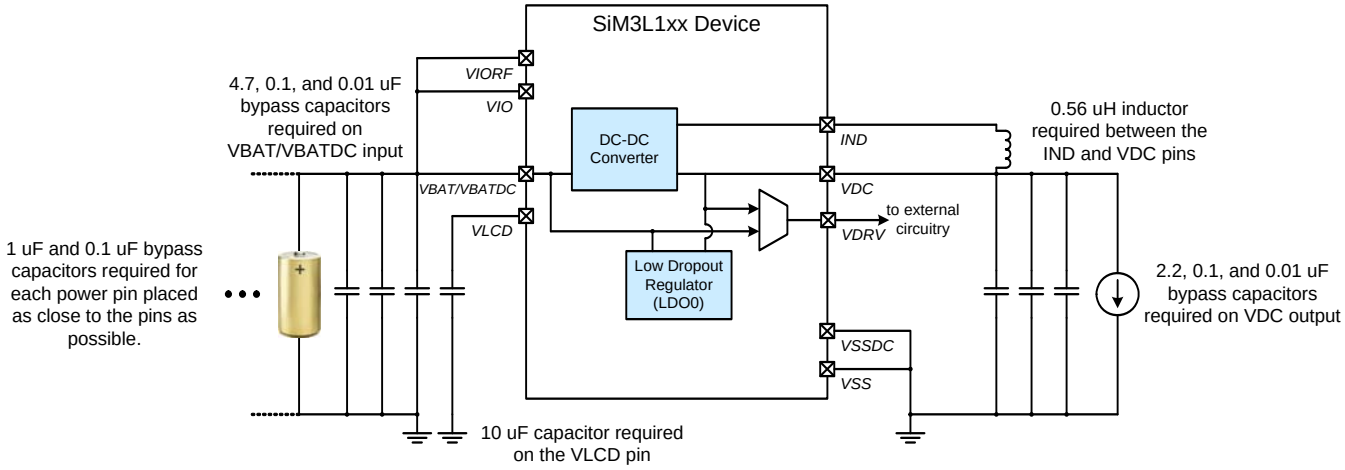


**Figure 2.2. Connection Diagram with DC-DC Converter Used and I/O Powered from Battery**

Figure 2.3 shows a typical connection diagram for the power pins of the SiM3L1xx devices when used with an external radio device like the Silicon Labs EZRadio® or EZRadioPRO® devices.

# 3. Electrical Specifications

## 3.1. Electrical Characteristics

All electrical parameters in all Tables are specified under the conditions listed in Table 3.1, unless stated otherwise.

**Table 3.1. Recommended Operating Conditions**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Supply Voltage on VBAT/VBATDC | $V_{BAT}$ | | 1.8 | — | 3.8 | V |
| Operating Supply Voltage on VDC | $V_{DC}$ | | 1.25 | — | 3.8 | V |
| Operating Supply Voltage on VDRV | $V_{DRV}$ | | 1.25 | — | 3.8 | V |
| Operating Supply Voltage on VIO | $V_{IO}$ | | 1.8 | — | $V_{BAT}$ | V |
| Operation Supply Voltage on VIORF | $V_{IORF}$ | | 1.8 | — | $V_{BAT}$ | V |
| Operation Supply Voltage on VLCD | $V_{LCD}$ | | 1.8 | — | 3.8 | V |
| System Clock Frequency (AHB) | $f_{AHB}$ | | 0 | — | 50 | MHz |
| Peripheral Clock Frequency (APB) | $f_{APB}$ | | 0 | — | 50 | MHz |
| Operating Ambient Temperature | $T_A$ | | –40 | — | +85 | °C |
| Operating Junction Temperature | $T_J$ | | –40 | — | 105 | °C |

**Note:** All voltages with respect to $V_{SS}$.

**Table 3.2. Power Consumption (Continued)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Power Mode 2[1,2,3,4,5]—Core halted with only Port I/O clocks on (wake from pin). | $I_{BAT}$ | $F_{AHB}$ = 49 MHz, $F_{APB}$ = 24.5 MHz | — | 4 | 7.2 | mA |
| | | $F_{AHB}$ = 20 MHz, $F_{APB}$ = 10 MHz | — | 1.47 | — | mA |
| | | $F_{AHB}$ = 2.5 MHz, $F_{APB}$ = 1.25 MHz | — | 430 | — | µA |
| Power Mode 3[1,2,6]—Fast-Wake Mode (PM3CLKEN = 1) | $I_{BAT}$ | $V_{BAT}$ = 3.8 V | — | 320 | 530 | µA |
| | | $V_{BAT}$ = 1.8 V | — | 225 | — | µA |
| Power Mode 4[1,2,4,6]—Slower clock speed with code executing from flash, peripheral clocks ON | $I_{BAT}$ | $F_{AHB}$ = $F_{APB}$ = 16 kHz, $V_{BAT}$ = 3.8 V | — | 385 | 640 | µA |
| | | $F_{AHB}$ = $F_{APB}$ = 16 kHz, $V_{BAT}$ = 1.8 V | — | 330 | — | µA |
| Power Mode 5[1,2,4,6]—Slower clock speed with code executing from RAM, peripheral clocks ON | $I_{BAT}$ | $F_{AHB}$ = $F_{APB}$ = 16 kHz, $V_{BAT}$ = 3.8 V | — | 320 | 490 | µA |
| | | $F_{AHB}$ = $F_{APB}$ = 16 kHz, $V_{BAT}$ = 1.8 V | — | 275 | — | µA |
| Power Mode 6[1,2,4,6]—Core halted with peripheral clocks ON | $I_{BAT}$ | $F_{AHB}$ = $F_{APB}$ = 16 kHz, $V_{BAT}$ = 3.8 V | — | 315 | 490 | µA |
| | | $F_{AHB}$ = $F_{APB}$ = 16 kHz, $V_{BAT}$ = 1.8 V | — | 270 | — | µA |
| Power Mode 8[1,2]—Low Power Sleep, powered through VBAT, VIO, and VIORF at 2.4 V, 32kB of retention RAM | $I_{BAT}$ | RTC Disabled, $T_A$ = 25 °C | — | 75 | 400 | nA |
| | | RTC w/ 16.4 kHz LFO, $T_A$ = 25 °C | — | 360 | — | nA |
| | | RTC w/ 32.768 kHz Crystal, $T_A$ = 25 °C | — | 670 | — | nA |

**Notes:**

1. Currents are additive. For example, where $I_{BAT}$ is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded $I_{VIO}$ is included in all $I_{BAT}$ PM8 production test measurements.

**Table 3.5. On-Chip Regulators**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DC-DC Buck Converter** | | | | | | |
| Input Voltage Range | $V_{DCIN}$ | | 1.8 | — | 3.8 | V |
| Input Supply to Output Voltage Differential (for regulation) | $V_{DCREG}$ | | 0.45 | — | — | V |
| Output Voltage Range | $V_{DCOUT}$ | | 1.25 | — | 3.8 | V |
| Output Voltage Accuracy | $V_{DCACC}$ | | — | ±25 | — | mV |
| Output Current | $I_{DCOUT}$ | | — | — | 90 | mA |
| Inductor Value[1] | $L_{DC}$ | | 0.47 | 0.56 | 0.68 | µH |
| Inductor Current Rating | $I_{LDC}$ | $I_{load}$ < 50 mA | 450 | — | — | mA |
| | | $I_{load}$ > 50 mA | 550 | — | — | mA |
| Output Capacitor Value | $C_{DCOUT}$ | | 1 | 2.2 | 10 | µF |
| Input Capacitor Value[2] | $C_{DCIN}$ | | — | 4.7 | — | µF |
| Load Regulation | $R_{load}$ | | — | 0.03 | — | mV/mA |
| Maximum DC Load Current During Startup | $I_{DCMAX}$ | | — | — | 5 | mA |
| Switching Clock Frequency | $F_{DCCLK}$ | | 1.9 | 2.9 | 3.8 | MHz |
| Local Oscillator Frequency | $F_{DCOSC}$ | | 2.4 | 2.9 | 3.4 | MHz |
| **LDO Regulators** | | | | | | |
| Input Voltage Range[3] | $V_{LDOIN}$ | Sourced from VBAT | 1.8 | — | 3.8 | V |
| | | Sourced from VDC | 1.9 | — | 3.8 | V |
| Output Voltage Range[4] | $V_{LDO}$ | | 0.8 | — | 1.9 | V |
| LDO Output Voltage Accuracy | $V_{LDOACC}$ | | — | ±25 | — | mV |
| Output Settings in PM8 (All LDOs) | $V_{LDO}$ | 1.8 V ≤ $V_{BAT}$ ≤ 2.9 V | 1.5 | | | V |
| | | 1.95 V ≤ $V_{BAT}$ ≤ 3.5 V | 1.8 | | | V |
| | | 2.0 V ≤ $V_{BAT}$ ≤ 3.8 V | 1.9 | | | V |

**Notes:**

1. See reference manual for recommended inductors.
2. Recommended: X7R or X5R ceramic capacitors with low ESR. Example: Murata GRM21BR71C225K with ESR < 10 mΩ (@ frequency > 1 MHz).
3. Input voltage specification accounts for the internal LDO dropout voltage under the maximum load condition to ensure that the LDO output voltage will remain at a valid level as long as $V_{LDOIN}$ is at or above the specified minimum.
4. The memory LDO output should always be set equal to or lower than the output of the analog LDO. When lowering both LDOs (for example to go into PM8 under low supply conditions), first adjust the memory LDO and then the analog LDO. When raising the output of both LDOs, adjust the analog LDO before adjusting the memory LDO.
5. Output range represents the programmable output range, and does not reflect the minimum voltage under all conditions. Dropout when the input supply is close to the output setting is normal, and accounted for.
6. Analog peripheral specifications assume a 1.8 V output on the analog LDO.

**Table 3.9. SAR ADC**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Resolution | $N_{bits}$ | 12 Bit Mode | | 12 | | Bits |
| | | 10 Bit Mode | | 10 | | Bits |
| Supply Voltage Requirements (VBAT) | $V_{ADC}$ | High Speed Mode | 2.2 | — | 3.8 | V |
| | | Low Power Mode | 1.8 | — | 3.8 | V |
| Throughput Rate (High Speed Mode) | $f_S$ | 12 Bit Mode | — | — | 250 | ksps |
| | | 10 Bit Mode | — | — | 1 | Msps |
| Throughput Rate (Low Power Mode) | $f_S$ | 12 Bit Mode | — | — | 62.5 | ksps |
| | | 10 Bit Mode | — | — | 250 | ksps |
| Tracking Time | $t_{TRK}$ | High Speed Mode | 230 | — | — | ns |
| | | Low Power Mode | 450 | — | — | ns |
| SAR Clock Frequency | $f_{SAR}$ | High Speed Mode | — | — | 16.24 | MHz |
| | | Low Power Mode | — | — | 4 | MHz |
| Conversion Time | $t_{CNV}$ | 10-Bit Conversion, SAR Clock = 16 MHz, APB Clock = 40 MHz | | 762.5 | | ns |
| Sample/Hold Capacitor | $C_{SAR}$ | Gain = 1 | — | 5 | — | pF |
| | | Gain = 0.5 | — | 2.5 | — | pF |
| Input Pin Capacitance | $C_{IN}$ | High Quality Inputs | — | 18 | — | pF |
| | | Normal Inputs | — | 20 | — | pF |
| Input Mux Impedance | $R_{MUX}$ | High Quality Inputs | — | 300 | — | Ω |
| | | Normal Inputs | — | 550 | — | Ω |
| Voltage Reference Range | $V_{REF}$ | | 1 | — | $V_{BAT}$ | V |
| Input Voltage Range* | $V_{IN}$ | Gain = 1 | 0 | — | $V_{REF}$ | V |
| | | Gain = 0.5 | 0 | — | $2xV_{REF}$ | V |
| Power Supply Rejection Ratio | $PSRR_{ADC}$ | | — | 70 | — | dB |
| **DC Performance** | | | | | | |
| Integral Nonlinearity | INL | 12 Bit Mode | — | ±1 | ±1.9 | LSB |
| | | 10 Bit Mode | — | ±0.2 | ±0.5 | LSB |
| Differential Nonlinearity (Guaranteed Monotonic) | DNL | 12 Bit Mode | –1 | ±0.7 | 1.8 | LSB |
| | | 10 Bit Mode | — | ±0.2 | ±0.5 | LSB |
| Offset Error (using VREFGND) | $E_{OFF}$ | 12 Bit Mode, VREF = 2.4 V | –2 | 0 | 2 | LSB |
| | | 10 Bit Mode, VREF = 2.4 V | –1 | 0 | 1 | LSB |

**Table 3.11. ACCTR (Advanced Capture Counter)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| LC Comparator Response Time, CMPMD = 11 (Highest Speed) | $t_{RESP0}$ | +100 mV Differential | — | 100 | — | ns |
| | | –100 mV Differential | — | 150 | — | ns |
| LC Comparator Response Time, CMPMD = 00 (Lowest Power) | $t_{RESP3}$ | +100 mV Differential | — | 1.4 | — | µs |
| | | –100 mV Differential | — | 3.5 | — | µs |
| LC Comparator Positive Hysteresis Mode 0 (CPMD = 11) | $HYS_{CP+}$ | CMPHYP = 00 | — | 0.37 | — | mV |
| | | CMPHYP = 01 | — | 7.9 | — | mV |
| | | CMPHYP = 10 | — | 16.7 | — | mV |
| | | CMPHYP = 11 | — | 32.8 | — | mV |
| LC Comparator Negative Hysteresis Mode 0 (CPMD = 11) | $HYS_{CP-}$ | CMPHYN = 00 | — | 0.37 | — | mV |
| | | CMPHYN = 01 | — | –7.9 | — | mV |
| | | CMPHYN = 10 | — | –16.1 | — | mV |
| | | CMPHYN = 11 | — | –32.7 | — | mV |
| LC Comparator Positive Hysteresis Mode 1 (CPMD = 10) | $HYS_{CP+}$ | CMPHYP = 00 | — | 0.47 | — | mV |
| | | CMPHYP = 01 | — | 5.85 | — | mV |
| | | CMPHYP = 10 | — | 12 | — | mV |
| | | CMPHYP = 11 | — | 24.4 | — | mV |
| LC Comparator Negative Hysteresis Mode 1 (CPMD = 10) | $HYS_{CP-}$ | CMPHYN = 00 | — | 0.47 | — | mV |
| | | CMPHYN = 01 | — | –6.0 | — | mV |
| | | CMPHYN = 10 | — | –12.1 | — | mV |
| | | CMPHYN = 11 | — | –24.6 | — | mV |
| LC Comparator Positive Hysteresis Mode 2 (CPMD = 01) | $HYS_{CP+}$ | CMPHYP = 00 | — | 0.66 | — | mV |
| | | CMPHYP = 01 | — | 4.55 | — | mV |
| | | CMPHYP = 10 | — | 9.3 | — | mV |
| | | CMPHYP = 11 | — | 19 | — | mV |
| LC Comparator Negative Hysteresis Mode 2 (CPMD = 01) | $HYS_{CP-}$ | CMPHYN = 00 | — | 0.6 | — | mV |
| | | CMPHYN = 01 | — | –4.5 | — | mV |
| | | CMPHYN = 10 | — | –9.5 | — | mV |
| | | CMPHYN = 11 | — | –19 | — | mV |

peripherals and may individually shut down and gate the clocks of any or all peripherals for power savings.

The on-chip debugging interface (SWJ-DP) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging.

Each device is specified for 1.8 to 3.8 V operation over the industrial temperature range (–40 to +85 °C). The SiM3L1xx devices are available in 40-pin or 64-pin QFN and 64-pin or 80-pin TQFP packages. All package options are lead-free and RoHS compliant. See Table 5.1 for ordering information. A block diagram is included in Figure 4.1.

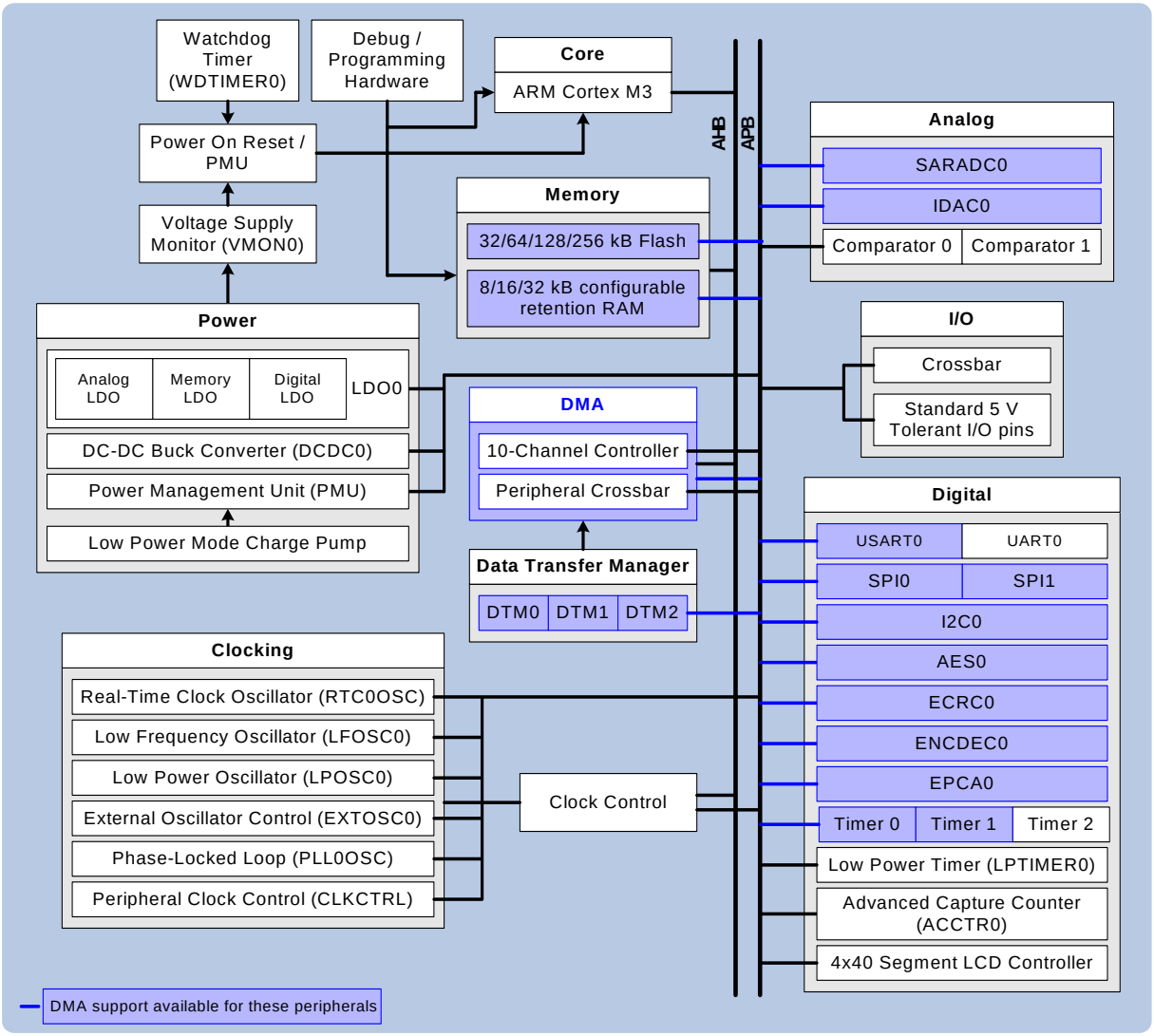


**Figure 4.1. Precision32™ SiM3L1xx Family Block Diagram**

#### 4.1.5.2. Power Mode 1 and Power Mode 5

Power Mode 1 and Power Mode 5 are fully operational modes with code executing from RAM. PM5 is the same as PM1, but with the clocks operating at a lower speed. This enables power to be conserved by reducing the LDO regulator outputs. Compared with the corresponding flash operational mode (Normal or PM4), the active power consumption of the device in these modes is reduced. Additionally, at higher speeds in PM1, the core throughput can also be increased because RAMdoesnot require additional wait states that reduce the instruction fetch speed.

#### 4.1.5.3. Power Mode 2 and Power Mode 6

In Power Mode 2 and Power Mode 6, the core halts and the peripherals continue to run at the selected clock speed. PM6 is the same as PM2, but with the clocks operating at a lower speed. This enables power to be conserved by reducing the LDO regulator outputs. To place the device in PM2 or PM6, the core should execute a wait-for-interrupt (WFI) or wait-for-event (WFE) instruction. If the WFI instruction is called from an interrupt service routine, the interrupt that wakes the device from PM2 or PM6 must be of a sufficient priority to be recognized by the core. It is recommended to perform both a DSB (Data Synchronization Barrier) and an ISB (Instruction Syncronization Barrier) operation prior to the WFI to ensure all bus accesses complete. When operating from the LFOSC0, PM6 can achieve similar power consumption to PM3, but with faster wake times and the ability to wake on any interrupt.

#### 4.1.5.4. Power Mode 3

In Power Mode 3 the core and peripheral clocks are halted. The available sources to wake from PM3 are controlled by the Power Management Unit (PMU). A special Fast Wake option allows the core to wake faster by keeping the LFOSC0 or RTC0 clock active. Because the current consumption of these blocks is minimal, it is recommended to use the fast wake option.

Before entering PM3, the DMA controller should be disabled, and the desired wake source(s) should be configured in the PMU. The SLEEPDEEP bit in the ARM System Control Register should be set, and the PMSEL bit in the CLKCTRL0_CONFIG register should be cleared to indicate that PM3 is the desired power mode. For fast wake, the core clocks (AHB and APB) should be configured to run from the LPOSC, and the PM3 Fast wake option and clock source should be selected in the PM3CN register.

The device will enter PM3 on a WFI or WFE instruction. If the WFI instruction is called from an interrupt service routine, the interrupt that wakes the device from PM3 must be of a sufficient priority to be recognized by the core. It is recommended to perform both a DSB (Data Synchronization Barrier) and an ISB (Instruction Synchronization Barrier) operation prior to the WFI to ensure all bus access is complete.

#### 4.1.5.5. Power Mode 8

In Power Mode 8, the core and most peripherals are completely powered down, but all registers and selected RAM blocks retain their state. The LDO regulators are disabled, so all active circuitry operates directly from VBAT. Alternatively, the PMU has a specialized VBAT-divided-by-2 charge pump that can power some internal modules while in PM8 to save power. The fully operational functions in this mode are: LPTIMER0 , RTC0, UART0 running from RTC0TCLK, PMU Pin Wake, the advanced capture counter, and the LCD controller.

This mode provides the lowest power consumption for the device, but requires an appropriate wake up source or reset to exit. The available wake up or reset sources to wake from PM8 are controlled by the Power Management Unit (PMU). The available wake up sources are: Low Power Timer (LPTIMER0), RTC0 (alarms and oscillator failure notification), Comparator 0 (CMP0), advanced capture counter (ACCTR0), LCD VBAT monitor (LCD0), UART0, low power mode charge pump failure, and PMU Pin Wake. The available reset sources are: RESET pin, VBAT supply monitor, Comparator 0, Comparator 1, low power mode charge pump failure, RTC0 oscillator failure, or a PMU wake event.

Before entering PM8, the desired wake source(s) should be configured in the PMU. The SLEEPDEEP bit in the ARM System Control Register should be set, and the PMSEL bit in the CLKCTRL0_CONFIG register should be set to indicate that PM8 is the desired power mode.

The device will enter PM8 on a WFI or WFE instruction, and remain in PM8 until a reset configured by the PMU occurs. It is recommended to perform both a DSB (Data Synchronization Barrier) and an ISB (Instruction Synchronization Barrier) operation prior to the WFI to ensure all bus access is complete.

### 4.3.1. PLL (PLL0)

The PLL module consists of a dedicated Digitally-Controlled Oscillator (DCO) that can be used in Free-Running mode without a reference frequency, Frequency-Locked to a reference frequency, or Phase-Locked to a reference frequency. The reference frequency for Frequency-Lock and Phase-Lock modes can use one of multiple sources (including the external oscillator) to provide maximum flexibility for different application needs. Because the PLL module generates its own clock, the DCO can be locked to a particular reference frequency and then moved to Free-Running mode to reduce system power and noise.

The PLL module includes the following features:

- Three output ranges with output frequencies ranging from 23 to 50 MHz.
- Multiple reference frequency inputs, including the RTC0 oscillator, Low Power Oscillator, and external oscillator.
- Three output modes: Free-Running Digitally-Controlled Oscillator, Frequency-Locked, and Phase-Locked.
- Able to sense the rising edge or falling edge of the reference source.
- DCO frequency LSB dithering to provide finer average output frequencies.
- Spectrum spreading to reduce generated system noise.
- Low jitter and fast lock times.\
- All output frequency updates (including dithering and spectrum spreading) can be temporarily suspended using the STALL bit during noise-sensitive measurements.

### 4.3.2. Low Power Oscillator (LPOSC0)

The Low Power Oscillator is the default AHB oscillator on SiM3L1xx devices and enables or disables automatically, as needed.

The default output frequency of this oscillator is factory calibrated to 20 MHz, and a divided 2.5 MHz version of this clock is also available as an AHB clock source.

The Low Power Oscillator has the following features:

- 20 MHz and divided 2.5 MHz frequencies available for the AHB clock.
- Automatically starts and stops as needed.

### 4.3.3. Low Frequency Oscillator (LFOSC0)

The low frequency oscillator (LFOSC) provides a low power internal clock source for the RTC0 timer and other peripherals on the device. No external components are required to use the low frequency oscillator, and the RTC1 and RTC2 pins do not need to be shorted together.

The Low Frequency Oscillator has the following features:

- 16.4 kHz output frequency.

### 4.3.4. External Oscillators (EXTOSC0)

The EXTOSC0 external oscillator circuit may drive an external crystal, ceramic resonator, capacitor, or RC network. A CMOS clock may also provide a clock input. The external oscillator output may be selected as the AHB clock or used to clock other modules independent of the AHB clock selection.

The External Oscillator control has the following features:

- Support for external crystal, resonator, RC, C, or CMOS oscillators.
- Support for external CMOS frequencies from 10 kHz to 50 MHz.
- Support for external crystal frequencies from 10 kHz to 25 MHz.
- Various drive strengths for flexible crystal oscillator support.
- Internal frequency divide-by-two option available.

### 4.5.4. 16/32-bit Enhanced CRC (ECRC0)

The ECRC module is designed to provide hardware calculations for flash memory verification and communications protocols. In addition to calculating a result from direct writes from firmware, the ECRC module can automatically snoop the APB bus and calculate a result from data written to or read from a particular peripheral. This allows for an automatic CRC result without directly feeding data through the ECRC module.

The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3). The 16-bit polynomial is fully programmable.

The ECRC module includes the following features:

- Support for a programmable 16-bit polynomial and one fixed 32-bit polynomial.
- Byte-level bit reversal for the CRC input.
- Byte-order reorientation of words for the CRC input.
- Word or half-word bit reversal of the CRC result.
- Ability to configure and seed an operation in a single register write.
- Support for single-cycle parallel (unrolled) CRC computation for 32-, 16-, or 8-bit blocks.
- Capability to CRC 32 bits of data per peripheral bus (APB) clock.
- Automatic APB bus snooping.
- Support for DMA writes using firmware request mode.

### 4.5.5. Encoder / Decoder (ENCDEC0)

The encoder / decoder module supports Manchester and Three-out-of-Six encoding and decoding from either firmware or DMA operations.

This module has the following features:

- Supports Manchester and Three-out-of-Six encoding and decoding.
- Automatic flag clearing when writing the input or reading the output data registers.
- Writing to the input data register automatically initiates an encode or decode operation.
- Optional output in one’s complement format.
- Hardware error detection for invalid input data during decode operations, which helps reduce power consumption and packet turn-around time.
- Flexible byte swapping on the input or output data.

- Multiple loop-back modes supported.
- Multi-processor communications support.
- Operates at 9600, 4800, 2400, or 1200 baud in Power Mode 8.

### 4.7.3. SPI (SPI0, SPI1)

SPI is a 3- or 4-wire communication interface that includes a clock, input data, output data, and an optional select signal.

The SPI0 and SPI1 modules include the following features:

- Supports 3- or 4-wire master or slave modes.
- Supports up to 10 MHz clock in master mode and 5 MHz clock in slave mode.
- Support for all clock phase and slave select (NSS) polarity modes.
- 16-bit programmable clock rate.
- Programmable MSB-first or LSB-first shifting.
- 8-byte FIFO buffers for both transmit and receive data paths to support high speed transfers.
- Support for multiple masters on the same data lines.

In addition, the SPI modules include several features to support autonomous DMA transfers:

- Hardware NSS control.
- Programmable FIFO threshold levels.
- Configurable FIFO data widths.
- Master or slave hardware flow control for the MISO and MOSI signals.

SPI1 is on fixed pins and supports additional flow control options using a fixed input (SPI1CTS). Neither SPI1 nor the flow control input are on the crossbar.

### 4.7.4. I2C (I2C0)

The I2C interface is a two-wire, bi-directional serial bus. The clock and data signals operate in open-drain mode with external pull-ups to support automatic bus arbitration.

Reads and writes to the interface are byte oriented with the I2C interface autonomously controlling the serial transfer of the data. Data can be transferred at up to 1/8th of the APB clock as a master or slave, which can be faster than allowed by the I2C specification, depending on the clock source used. A method of extending the clock-low duration is available to accommodate devices with different speed capabilities on the same bus.

The I2C interface may operate as a master and/or slave, and may function on a bus with multiple masters. The I2C provides control of SDA (serial data), SCL (serial clock) generation and synchronization, arbitration logic, and start/stop control and generation.

The I2C0 module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds.
- Can operate down to APB clock divided by 32768 or up to APB clock divided by 8.
- Support for master, slave, and multi-master modes.
- Hardware synchronization and arbitration for multi-master mode.
- Clock low extending (clock stretching) to interface with faster masters.
- Hardware support for 7-bit slave and general call address recognition.
- Firmware support for 10-bit slave address decoding.
- Ability to disable all slave states.
- Programmable clock high and low period.
- Programmable data setup/hold times.
- Spike suppression up to 2 times the APB period.

# 5. Ordering Information

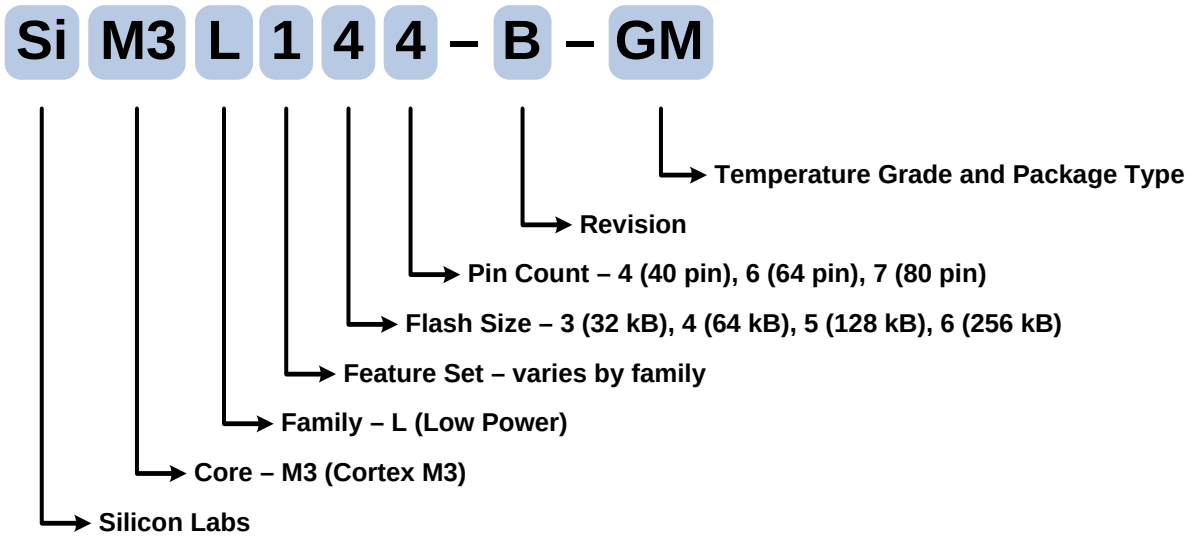


**Figure 5.1. SiM3L1xx Part Numbering**

All devices in the SiM3L1xx family have the following features:

- **Core:** ARM Cortex-M3 with maximum operating frequency of 50 MHz.
- **PLL.**
- **10-Channel DMA Controller.**
- **128/192/256-bit AES.**
- **16/32-bit CRC.**
- **Encoder/Decoder.**
- **DC-DC Buck Converter.**
- **Timers:** 3 x 32-bit (6 x 16-bit).
- **Real-Time Clock.**
- **Low-Power Timer.**
- **PCA:** 1 x 6 channels (Enhanced)
- **ADC:** 12-bit 250 ksps (10-bit 1 Msps) SAR.
- **DAC:** 10-bit IDAC.
- **Temperature Sensor.**
- **Internal VREF.**
- **Comparator:** 2 x low current.
- **Serial Buses:** 2 x USART, 2 x SPI, 1 x I2C

Additionally, all devices in the SiM3L1xx family include the low power mode advanced capture counter (ACCTR0), though the smaller packages (SiM3L1x4) only support some of the external inputs and outputs.

**Table 5.1. Product Selection Guide**

| Ordering Part Number | Flash Memory (kB) | RAM (kB) | LCD Segments | Digital Port I/Os | Digital Port I/Os on the Crossbar | Number of SARADC0 Channels | Number of Comparator 0/1 Inputs (+/-) | Number of PMU Pin Wake Sources | Number of ACCTR0 Inputs and Outputs | JTAG Debugging Interface | ETM Debugging Interface | Serial Wire Debugging Interface | Lead-free (RoHS Compliant) | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SiM3L167-C-GQ | 256 | 32 | 160 (4x40) | 62 | 38 | 24 | 15/15 | 14 | 12 | ✓ | ✓ | ✓ | ✓ | TQFP-80 |
| SiM3L166-C-GM | 256 | 32 | 128 (4x32) | 51 | 34 | 23 | 14/12 | 11 | 12 | | ✓ | ✓ | ✓ | QFN-64 |
| SiM3L166-C-GQ | 256 | 32 | 128 (4x32) | 51 | 34 | 23 | 14/12 | 11 | 12 | | ✓ | ✓ | ✓ | TQFP-64 |
| SiM3L164-C-GM | 256 | 32 | | 28 | 26 | 20 | 9/10 | 11 | 5 | | | ✓ | ✓ | QFN-40 |
| SiM3L157-C-GQ | 128 | 32 | 160 (4x40) | 62 | 38 | 24 | 15/15 | 14 | 12 | ✓ | ✓ | ✓ | ✓ | TQFP-80 |
| SiM3L156-C-GM | 128 | 32 | 128 (4x32) | 51 | 34 | 23 | 14/12 | 11 | 12 | | ✓ | ✓ | ✓ | QFN-64 |
| SiM3L156-C-GQ | 128 | 32 | 128 (4x32) | 51 | 34 | 23 | 14/12 | 11 | 12 | | ✓ | ✓ | ✓ | TQFP-64 |
| SiM3L154-C-GM | 128 | 32 | | 28 | 26 | 20 | 9/10 | 11 | 5 | | | ✓ | ✓ | QFN-40 |
| SiM3L146-C-GM | 64 | 16 | 128 (4x32) | 51 | 34 | 23 | 14/12 | 11 | 12 | | ✓ | ✓ | ✓ | QFN-64 |
| SiM3L146-C-GQ | 64 | 16 | 128 (4x32) | 51 | 34 | 23 | 14/12 | 11 | 12 | | ✓ | ✓ | ✓ | TQFP-64 |
| SiM3L144-C-GM | 64 | 16 | | 28 | 26 | 20 | 9/10 | 11 | 5 | | | ✓ | ✓ | QFN-40 |
| SiM3L136-C-GM | 32 | 8 | 128 (4x32) | 51 | 34 | 23 | 14/12 | 11 | 12 | | ✓ | ✓ | ✓ | QFN-64 |
| SiM3L136-C-GQ | 32 | 8 | 128 (4x32) | 51 | 34 | 23 | 14/12 | 11 | 12 | | ✓ | ✓ | ✓ | TQFP-64 |
| SiM3L134-C-GM | 32 | 8 | | 28 | 26 | 20 | 9/10 | 11 | 5 | | | ✓ | ✓ | QFN-40 |

**Table 6.2. Pin Definitions and Alternate Functions for SiM3L1x6**

| Pin Name | Type | Pin Numbers | I/O Voltage Domain | Crossbar Capability | Port Match | LCD Interface | Output Toggle Logic | External Trigger Inputs / Digital Functions | Analog Functions |
|---|---|---|---|---|---|---|---|---|---|
| VSS | Ground | 10<br>41 | | | | | | | |
| VSSDC | Ground (DC-DC) | 10 | | | | | | | |
| VIO | Power (I/O) | 6 | | | | | | | |
| VIORF / VDRV | Power (RF I/O) | 7 | | | | | | | |
| VBAT / VBATDC | | 8 | | | | | | | |
| VDC | | 11 | | | | | | | |
| VLCD | Power (LCD Charge Pump) | 54 | | | | | | | |
| IND | DC-DC Inductor | 9 | | | | | | | |
| $\overline{\text{RESET}}$ | Active-low Reset | 57 | | | | | | | |
| SWCLK | Serial Wire | 5 | | | | | | | |
| SWDIO | Serial Wire | 4 | | | | | | | |
| RTC1 | RTC Oscillator Input | 56 | | | | | | | |
| RTC2 | RTC Oscillator Output | 55 | | | | | | | |
| PB0.0 | Standard I/O | 3 | VIO | XBR 0 | ✓ | | ✓ | INT0.0<br>WAKE.0 | ADC0.20<br>VREF<br>CMP0P.0 |
| PB0.1 | Standard I/O | 2 | VIO | XBR 0 | ✓ | | ✓ | INT0.1<br>WAKE.2 | ADC0.22<br>CMP0N.0<br>CMP1P.0<br>XTAL2 |

**Table 6.3. Pin Definitions and Alternate Functions for SiM3L1x4 (Continued)**

| Pin Name | Type | Pin Numbers | I/O Voltage Domain | Crossbar Capability | Port Match | Output Toggle Logic | External Trigger Inputs / Digital Functions | Analog Functions |
|---|---|---|---|---|---|---|---|---|
| PB0.2 | Standard I/O | 40 | VIO | XBR0 | ✓ | ✓ | INT0.2<br>WAKE.3 | ADC0.23<br>CMP0N.1<br>CMP1N.0<br>XTAL1 |
| PB0.3 | Standard I/O | 39 | VIO | XBR0 | ✓ | ✓ | INT0.3<br>WAKE.4 | ADC0.0<br>CMP0P.1<br>IDAC0 |
| PB0.4 | Standard I/O | 38 | VIO | XBR0 | ✓ | ✓ | INT0.4<br>WAKE.5 | ACCTR0_IN0 |
| PB0.5 | Standard I/O | 37 | VIO | XBR0 | ✓ | ✓ | INT0.5<br>WAKE.6 | ACCTR0_IN1 |
| PB0.6/SWV | Standard I/O<br>/Serial Wire Viewer | 36 | VIO | XBR0 | ✓ | ✓ | LPT0T0<br>LPT0OUT0<br>INT0.6<br>WAKE.8 | |
| PB0.7 | Standard I/O | 32 | VIO | XBR0 | ✓ | ✓ | LPT0T6<br>INT0.7<br>UART0_TX | CMP1P.2 |
| PB0.8 | Standard I/O | 31 | VIO | XBR0 | ✓ | ✓ | LPT0T7<br>INT0.8<br>UART0_RX | CMP1N.2 |
| PB0.9 | Standard I/O | 30 | VIO | XBR0 | ✓ | ✓ | LPT0T1<br>INT0.9<br>RTC0TCLK_OUT | ADC0.1 |
| PB2.0 | Standard I/O | 29 | VIORF | XBR0 | ✓ | | LPT0T8<br>INT1.0<br>WAKE.12<br>SPI1_CTS | ADC0.2<br>CMP0P.4 |

## 6.4. TQFP-80 Package Specifications

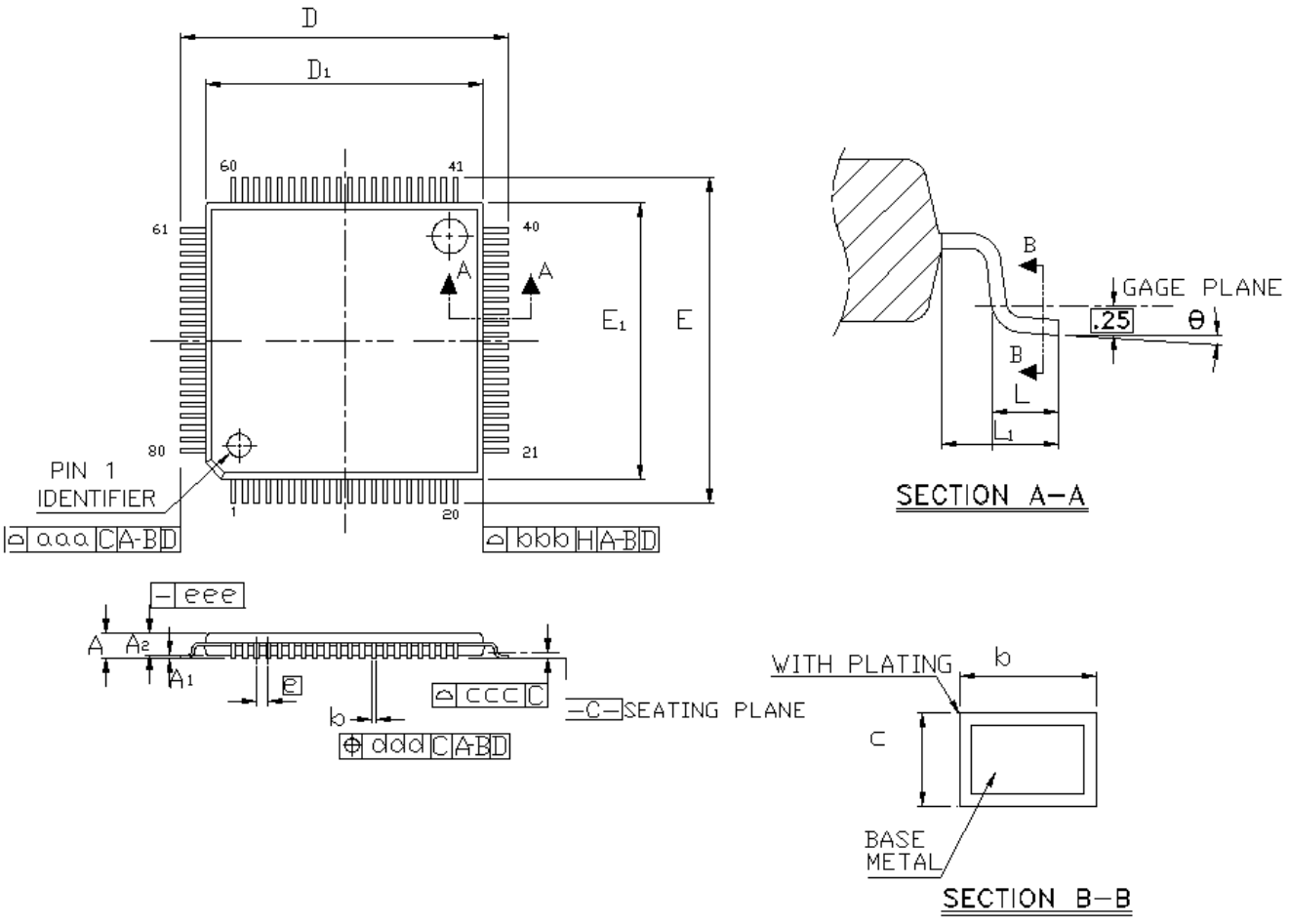


**Figure 6.5. TQFP-80 Package Drawing**

### 6.4.1. TQFP-80 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

### 6.4.2. TQFP-80 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.

### 6.4.3. TQFP-80 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

### 6.7.1. QFN-40 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

### 6.7.2. QFN-40 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 3x3 array of 1.1 mm square openings on a 1.6 mm pitch should be used for the center ground pad.

### 6.7.3. QFN-40 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

# 7. Revision Specific Behavior

This chapter describes any differences between released revisions of the device.

## 7.1. Revision Identification

The Lot ID Code on the top side of the device package can be used for decoding device revision information. Figures 7.1, 7.2, and 7.3 show how to find the Lot ID Code on the top side of the device package.

In addition, firmware can determine the revision of the device by checking the DEVICEID registers.

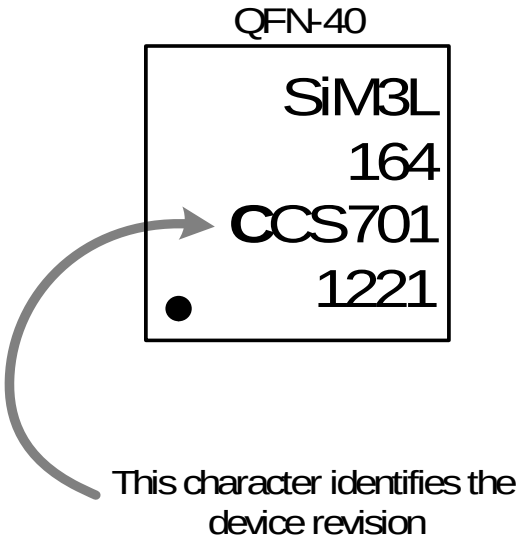


**Figure 7.1. SiM3L1x7-GQ Revision Information**

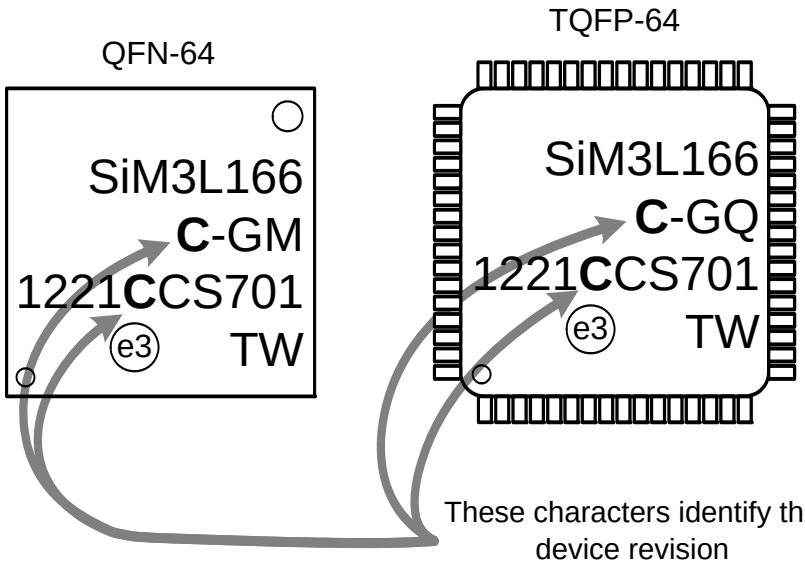


**Figure 7.2. SiM3L1x6-GM and SiM3L1x6-GQ Revision Information**