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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	-
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 38x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-UFBGA, WLCSP
Supplier Device Package	120-WLCSP (5.29x5.28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk60dn512zcab10r

Field	Description	Values
FFF	Program flash memory size	• 32 = 32 KB • 64 = 64 KB • 128 = 128 KB • 256 = 256 KB • 512 = 512 KB • 1M0 = 1 MB • 2M0 = 2 MB
R	Silicon revision	• Z = Initial • (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = –40 to 105 • C = –40 to 85 • (Blank) = 0 to 70
PP	Package identifier	• FM = 32 QFN (5 mm x 5 mm) • FT = 48 QFN (7 mm x 7 mm) • LF = 48 LQFP (7 mm x 7 mm) • LH = 64 LQFP (10 mm x 10 mm) • MP = 64 MAPBGA (5 mm x 5 mm) • LK = 80 LQFP (12 mm x 12 mm) • LL = 100 LQFP (14 mm x 14 mm) • MC = 121 MAPBGA (8 mm x 8 mm) • AB = 120 WLCSP (5.29 mm x 5.28 mm) • LQ = 144 LQFP (20 mm x 20 mm) • MD = 144 MAPBGA (13 mm x 13 mm) • MJ = 256 MAPBGA (17 mm x 17 mm)
CC	Maximum CPU frequency (MHz)	• 5 = 50 MHz • 7 = 72 MHz • 10 = 100 MHz • 12 = 120 MHz • 15 = 150 MHz
N	Packaging type	• R = Tape and reel

2.4 Example

This is an example part number:

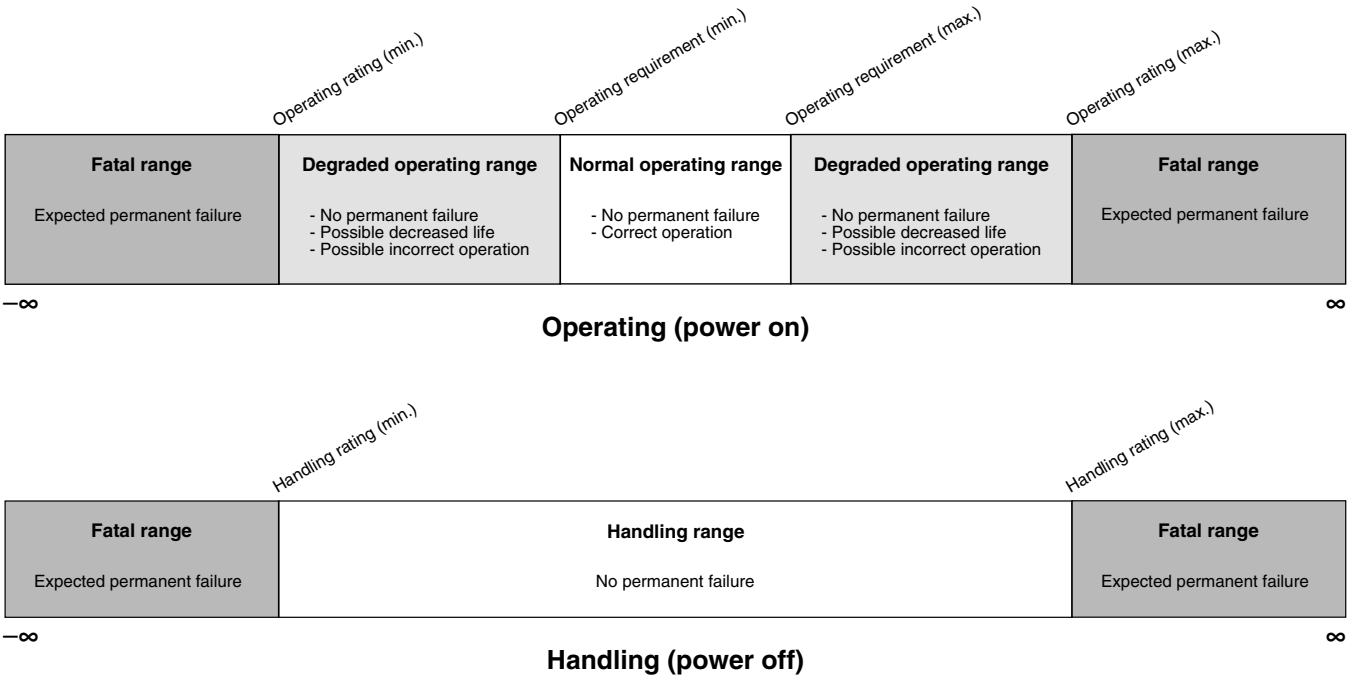
MK60DN512ZVMD10

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.6 Relationship between ratings and operating requirements



3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	N/A	—	mA	6
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	N/A	—	mA	7
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	N/A	—	mA	8
I_{DD_STOP}	Stop mode current at 3.0 V					
	• @ –40 to 25°C	—	0.59	2.5	mA	
	• @ 70°C	—	2.26	7.9	mA	
	• @ 85°C	—	2.5	14.0	mA	
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	• @ –40 to 25°C	—	93	435	µA	
	• @ 70°C	—	520	2000	µA	
	• @ 85°C	—	550	2750	µA	
I_{DD_LLS}	Low leakage stop mode current at 3.0 V					9
	• @ –40 to 25°C	—	4.8	30	µA	
	• @ 70°C	—	28	68	µA	
	• @ 85°C	—	45	115	µA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					9
	• @ –40 to 25°C	—	3.1	8.9	µA	
	• @ 70°C	—	17	35	µA	
	• @ 85°C	—	30	60	µA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					
	• @ –40 to 25°C	—	2.2	5.4	µA	
	• @ 70°C	—	7.1	12.5	µA	
	• @ 85°C	—	13	20	µA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	• @ –40 to 25°C	—	2.1	7.6	µA	
	• @ 70°C	—	6.2	13.5	µA	
	• @ 85°C	—	11	16	µA	
I_{DD_VBAT}	Average current with RTC and 32kHz disabled at 3.0 V					
	• @ –40 to 25°C	—	0.33	0.39	µA	
	• @ 70°C	—	0.60	0.78	µA	
	• @ 85°C	—	1.1	1.70	µA	

Table continues on the next page...

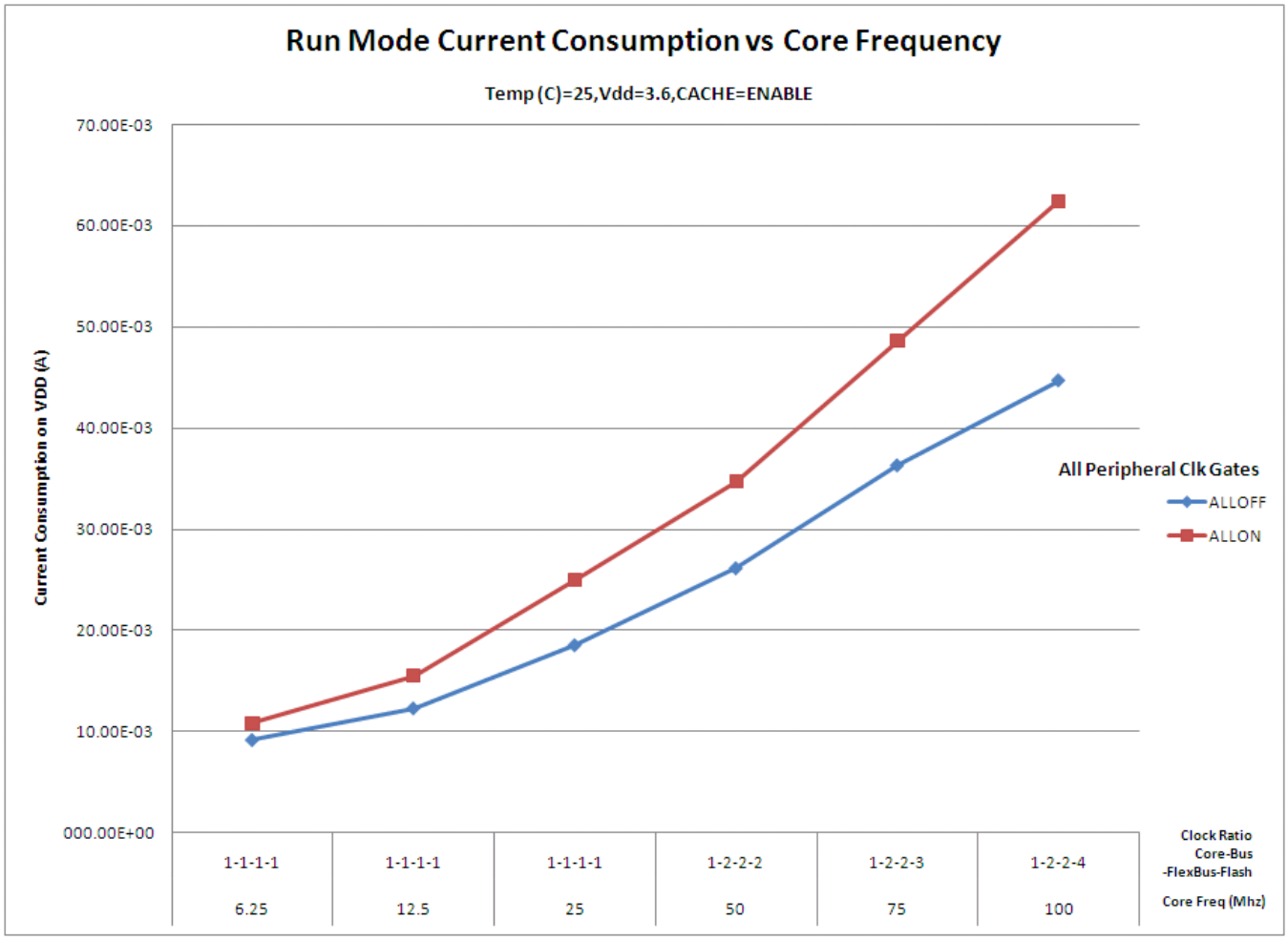


Figure 2. Run mode supply current vs. core frequency

5.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors as measured on 144LQFP and 144MAPBGA packages

Symbol	Description	Frequency band (MHz)	144LQFP	144MAPBGA	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	23	12	dBµV	1 , 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	27	24	dBµV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	28	27	dBµV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	14	11	dBµV	
V_{RE_IEC}	IEC level	0.15–1000	K	K	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2. V_{DD} = 3.3 V, T_A = 25 °C, f_{OSC} = 12 MHz (crystal), f_{SYS} = 96 MHz, f_{BUS} = 48MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for "EMC design."

5.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

5.3 Switching specifications

5.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	100	MHz	
f_{SYS_USB}	System and core clock when Full Speed USB in operation	20	—	MHz	
f_{ENET}	System and core clock when ethernet in operation • 10 Mbps • 100 Mbps	 5 50	 — —	MHz	
f_{BUS}	Bus clock	—	50	MHz	
FB_CLK	FlexBus clock	—	50	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	

5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
MK60DN512ZCAB10R				
T_J	Die junction temperature	–40	95	°C
T_A	Ambient temperature	–40	85	°C
MK60DN512ZAB10R				
T_J	Die junction temperature	0	80	°C
T_A	Ambient temperature	0	70	°C

5.4.2 Thermal attributes

Board type	Symbol	Description	120 WLCSP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	83	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	37	°C/W	1,2, 3
—	$R_{\theta JB}$	Thermal resistance, junction to board	11	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	2.4	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	3	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. Board meets JESD51-9 specification.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal.
4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
5. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.

Table 16. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{pp}[5]	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x,C_y can be provided by using either the integrated capacitors or by using external components.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.2.2 Oscillator frequency specifications

Table 17. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.

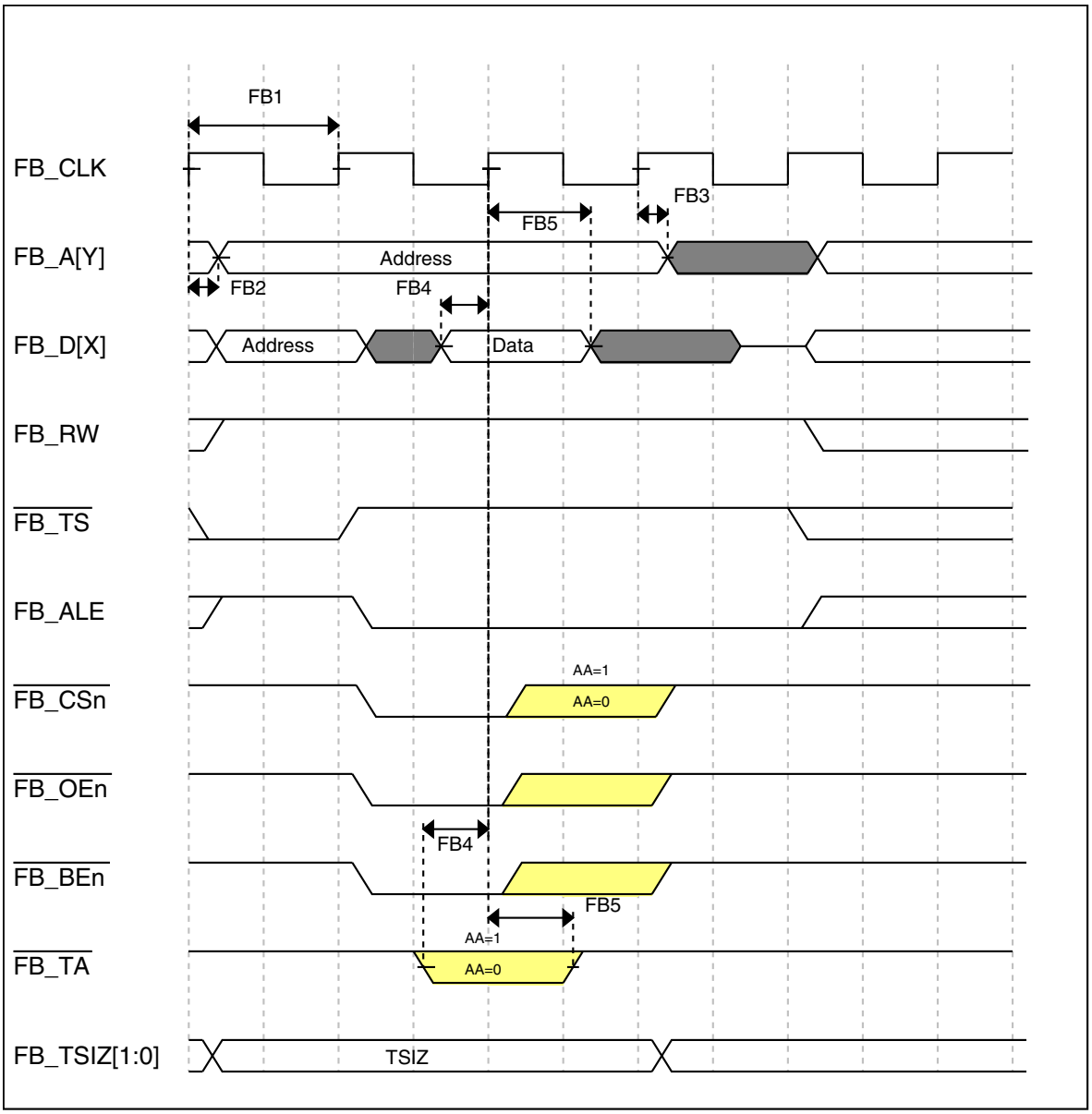


Figure 10. FlexBus read timing diagram

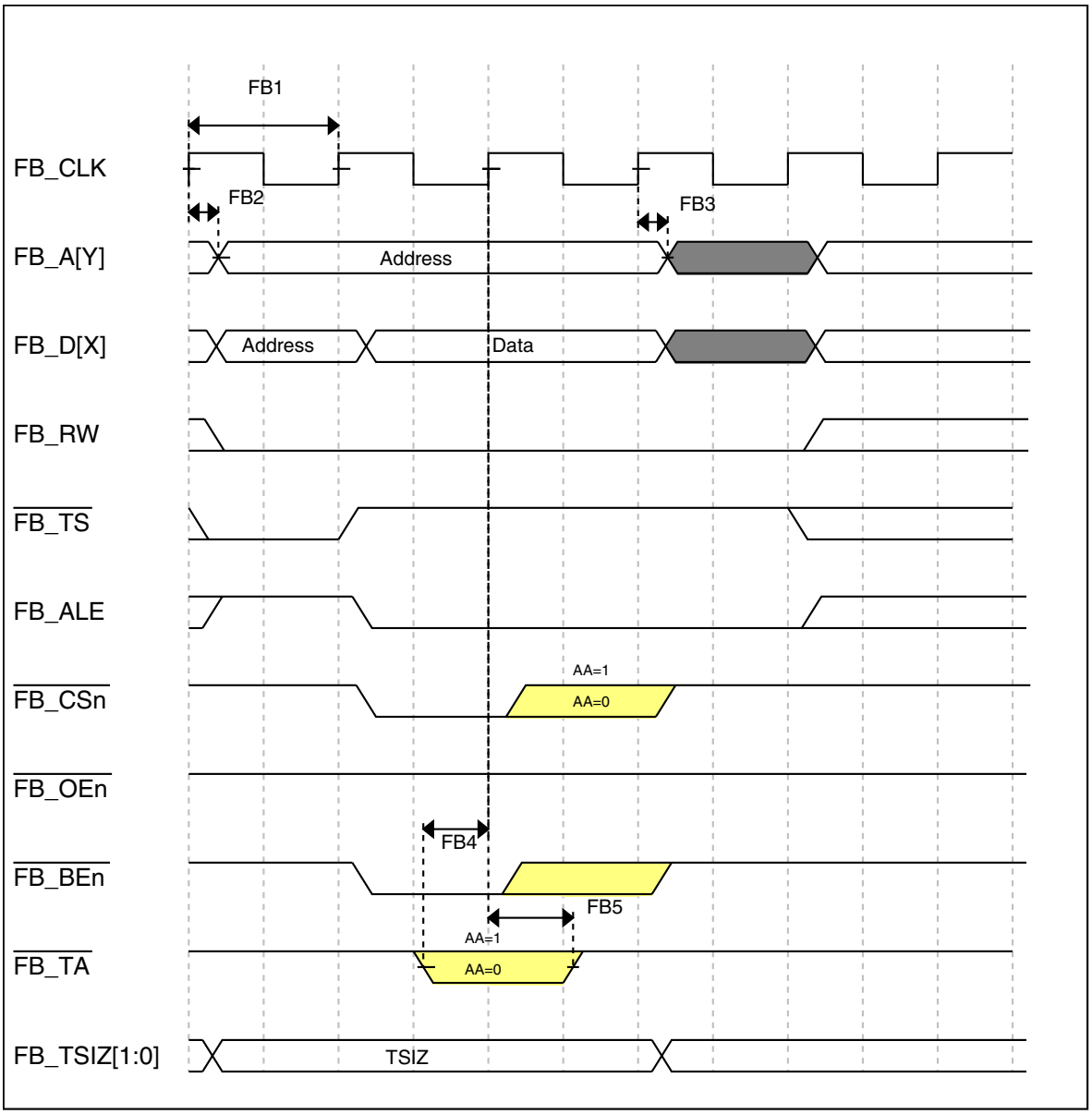


Figure 11. FlexBus write timing diagram

6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

6.6 Analog

Table 28. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0 • ADLPC = 1, ADHSC = 1 • ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	t_{ADACK} = 1/ f_{ADACK}
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB[4]	5
DNL	Differential non-linearity	• 12-bit modes • <12-bit modes	— —	±0.7 ±0.2	-1.1 to +1.9 -0.3 to 0.5	LSB[4]	5
INL	Integral non-linearity	• 12-bit modes • <12-bit modes	— —	±1.0 ±0.5	-2.7 to +1.9 -0.7 to +0.5	LSB[4]	5
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	-4 -1.4	-5.4 -1.8	LSB[4]	V_{ADIN} = V_{DDA} 5
E_Q	Quantization error	• 16-bit modes • ≤13-bit modes	— —	-1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16-bit differential mode • Avg = 32 • Avg = 4 16-bit single-ended mode • Avg = 32 • Avg = 4	 12.8 11.9 12.2 11.4	 14.5 13.8 13.9 13.1	 — — — —	 bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 — —	 –94 -85	 — —	 dB dB	7
SFDR	Spurious free dynamic range	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 82 78	 95 90	 — —	 dB dB	7

Table continues on the next page...

Table 28. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
E_{IL}	Input leakage error			$I_{In} \times R_{AS}$		mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation the ADLPC bit must be set, the HSC bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = (V_{REFH} - V_{REFL})/2^N
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.

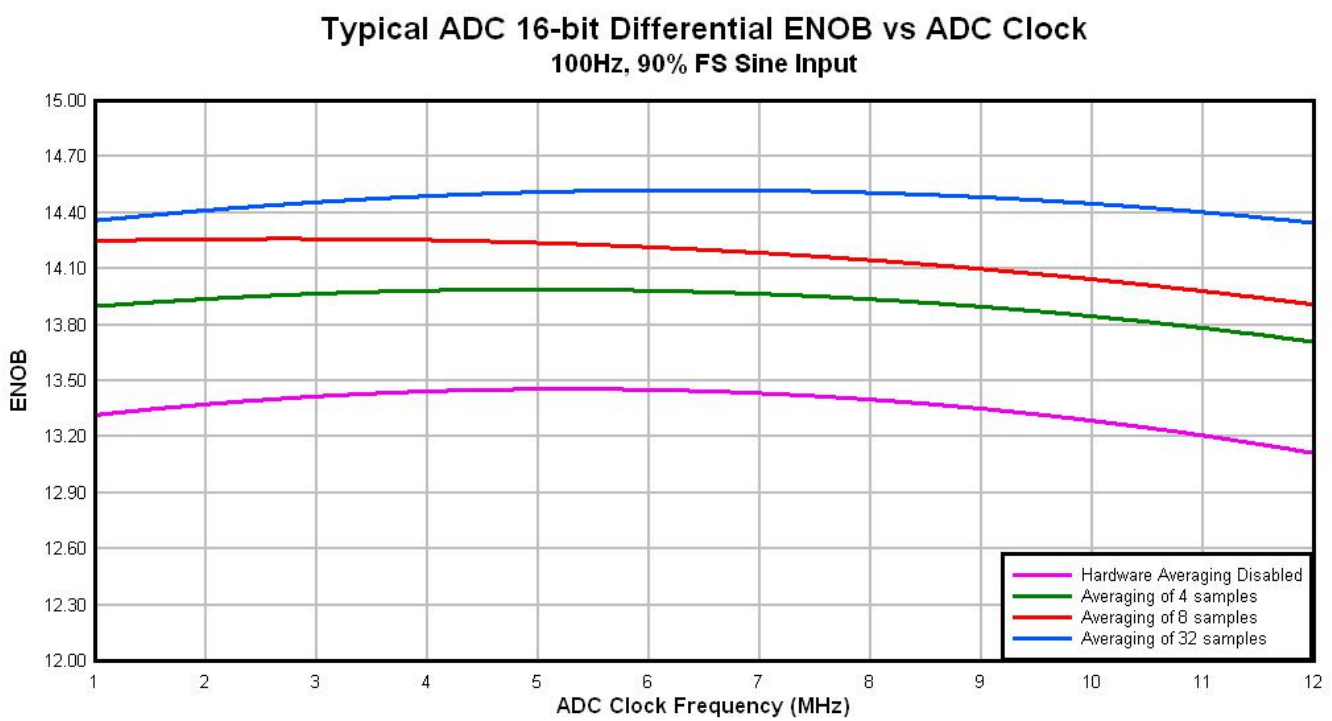


Figure 13. Typical ENOB vs. ADC_CLK for 16-bit differential mode

Table 44. Master mode DSPI timing (full voltage range) (continued)

Num	Description	Min.	Max.	Unit	Notes
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) - 4	($t_{SCK/2}$) + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 4	—	ns	2
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 4	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-4.5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	20.5	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

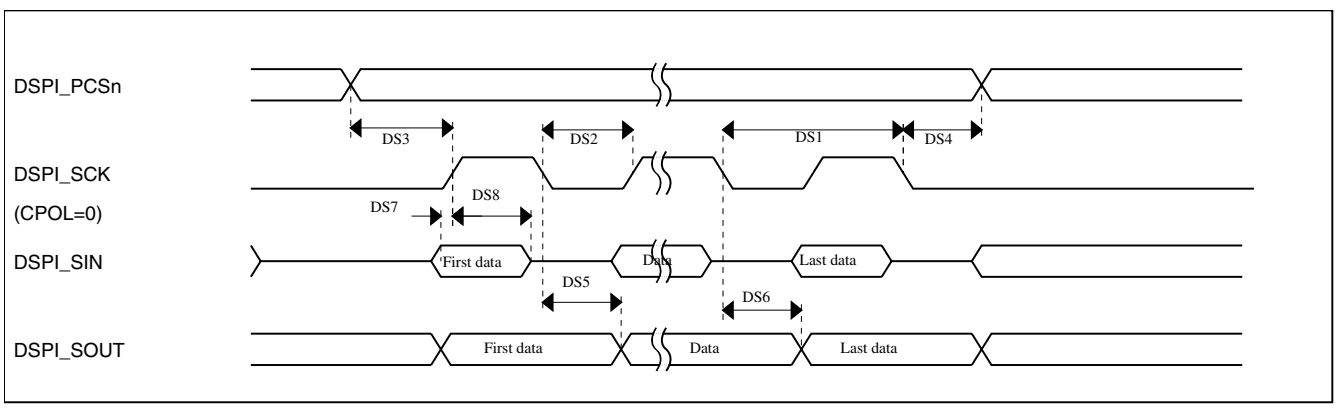


Figure 23. DSPI classic SPI timing — master mode

Table 45. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	6.25	MHz
DS9	DSPI_SCK input cycle time	8 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) - 4	($t_{SCK/2}$) + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	19	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	19	ns

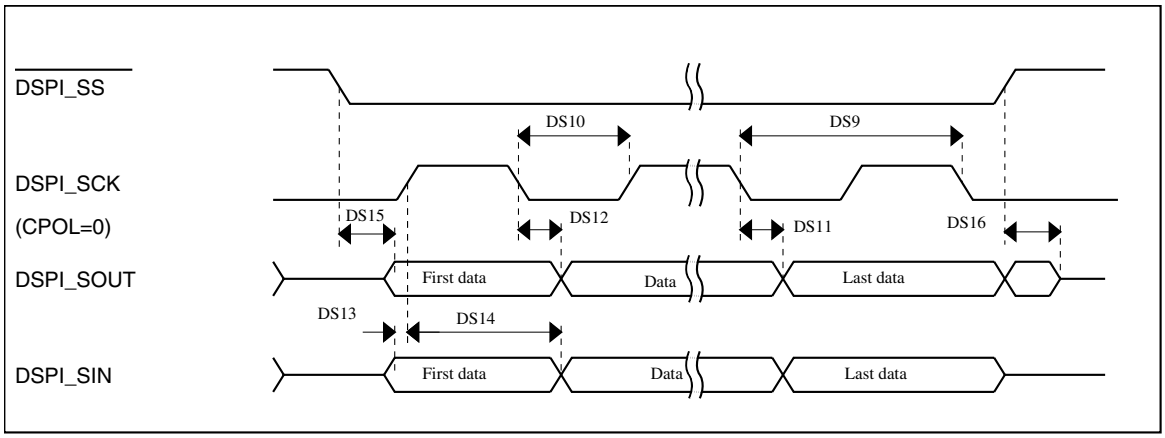


Figure 24. DSPI classic SPI timing — slave mode

6.8.8 Inter-Integrated Circuit Interface (I^2C) timing

Table 46. I^2C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I_2C bus devices	t_{HD}; DAT	0[1]	3.45[2]	0[3]	0.9[1]	µs
Data set-up time	t_{SU}; DAT	250[4]	—	100[2, 5]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[6]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[5]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The master mode I^2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
3. Input signal Slew = 10ns and Output Load = 50pf
4. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
5. A Fast mode I^2C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I^2C bus specification) before the SCL line is released.

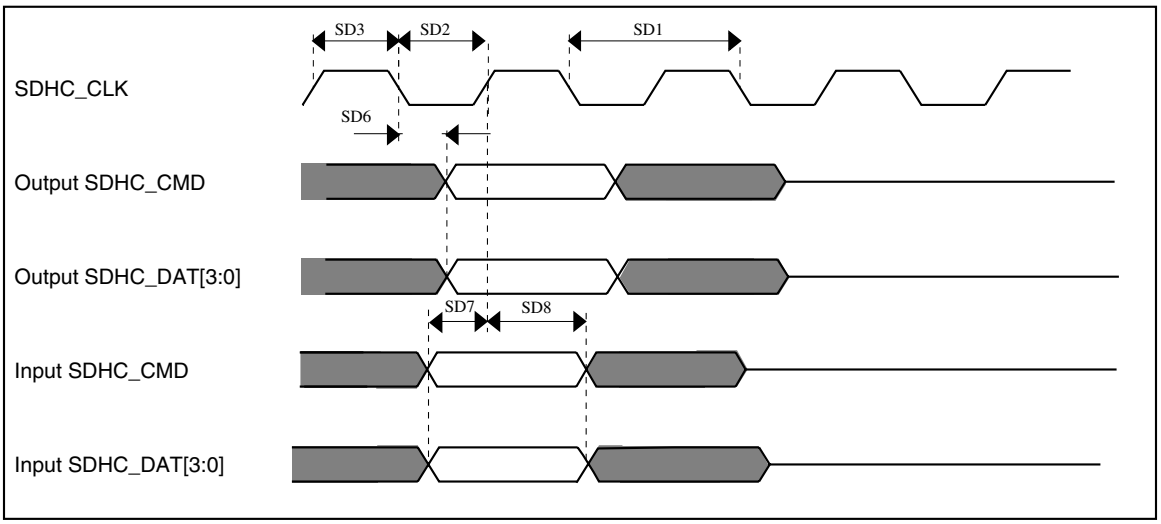


Figure 26. SDHC timing

6.8.11 I²S switching specifications

This section provides the AC timings for the I²S in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (TCR[TSCKP] = 0, RCR[RSCKP] = 0) and a non-inverted frame sync (TCR[TFSI] = 0, RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (I2S_BCLK) and/or the frame sync (I2S_FS) shown in the figures below.

Table 48. I²S master mode timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S1	I2S_MCLK cycle time	2 x t_{SYS}		ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_BCLK cycle time	5 x t_{SYS}	—	ns
S4	I2S_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_BCLK to I2S_FS output valid	—	15	ns
S6	I2S_BCLK to I2S_FS output invalid	-2.5	—	ns
S7	I2S_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_BCLK to I2S_TXD invalid	-3	—	ns
S9	I2S_RXD/I2S_FS input setup before I2S_BCLK	20	—	ns
S10	I2S_RXD/I2S_FS input hold after I2S_BCLK	0	—	ns

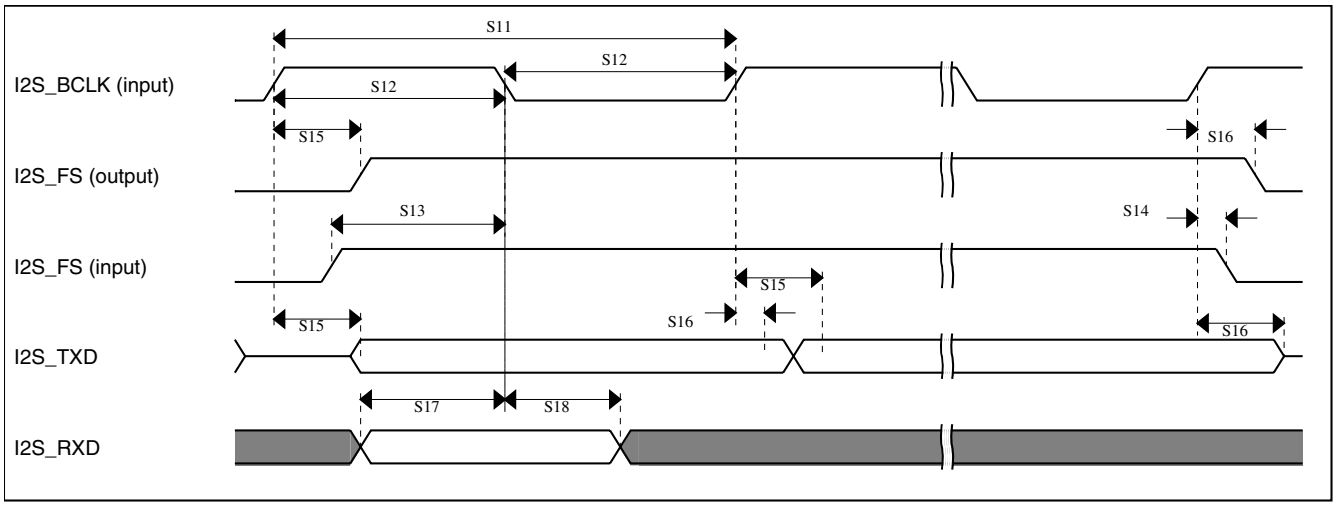


Figure 28. I²S timing — slave modes

Table 50. I²S master mode timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	2 x t_{SYS}		ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_BCLK cycle time	5 x t_{SYS}	—	ns
S4	I2S_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_BCLK to I2S_FS output valid	—	15	ns
S6	I2S_BCLK to I2S_FS output invalid	-4.3	—	ns
S7	I2S_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_BCLK to I2S_TXD invalid	-4.6	—	ns
S9	I2S_RXD/I2S_FS input setup before I2S_BCLK	23.9	—	ns
S10	I2S_RXD/I2S_FS input hold after I2S_BCLK	0	—	ns

Table 51. I²S slave mode timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_BCLK cycle time (input)	8 x t_{SYS}	—	ns
S12	I2S_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_FS input setup before I2S_BCLK	10	—	ns
S14	I2S_FS input hold after I2S_BCLK	3.5	—	ns
S15	I2S_BCLK to I2S_TXD/I2S_FS output valid	—	28.6	ns
S16	I2S_BCLK to I2S_TXD/I2S_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_BCLK	2	—	ns

6.9 Human-machine interfaces (HMI)

6.9.1 TSI electrical specifications

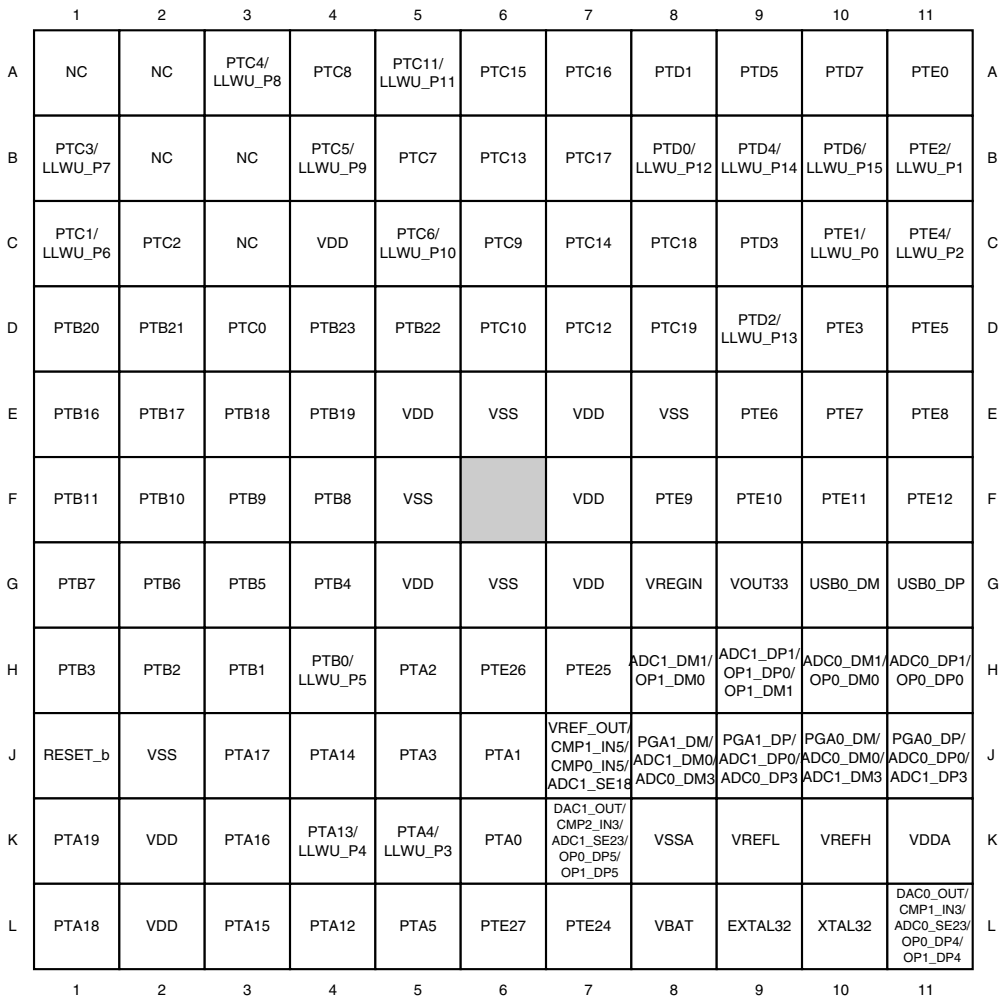
Table 52. TSI electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DDTSI}	Operating voltage	1.71	—	3.6	V	
C_{ELE}	Target electrode capacitance range	1	20	500	pF	1
f_{REFmax}	Reference oscillator frequency	—	5.5	12.7	MHz	2
f_{ELEmax}	Electrode oscillator frequency	—	0.5	4.0	MHz	3
C_{REF}	Internal reference capacitor	0.5	1	1.2	pF	
V_{DELTA}	Oscillator delta voltage	100	600	760	mV	4
I_{REF}	Reference oscillator current source base current • 1uA setting (REFCHRG=0) • 32uA setting (REFCHRG=31)	— —	1.133 36	1.5 50	µA	3 , 5
I_{ELE}	Electrode oscillator current source base current • 1uA setting (EXTCHRG=0) • 32uA setting (EXTCHRG=31)	— —	1.133 36	1.5 50	µA	3 , 6
Pres5	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	7
Pres20	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	8
Pres100	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	9
MaxSens	Maximum sensitivity	0.003	12.5	—	fF/count	10
Res	Resolution	—	—	16	bits	
T_{Con20}	Response time @ 20 pF	8	15	25	µs	11
I_{TSI_RUN}	Current added in run mode	—	55	—	µA	
I_{TSI_LP}	Low power mode current adder	—	1.3	2.5	µA	12

1. The TSI module is functional with capacitance values outside this range. However, optimal performance is not guaranteed.
2. CAPTRM=7, DELVOL=7, and fixed external capacitance of 20 pF.
3. CAPTRM=0, DELVOL=2, and fixed external capacitance of 20 pF.
4. CAPTRM=0, EXTCHRG=9, and fixed external capacitance of 20 pF.
5. The programmable current source value is generated by multiplying the SCANC[REFCHRG] value and the base current.
6. The programmable current source value is generated by multiplying the SCANC[EXTCHRG] value and the base current.
7. Measured with a 5 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 8; Iext = 16.
8. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 2; Iext = 16.
9. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 16, NSCN = 3; Iext = 16.
10. Sensitivity defines the minimum capacitance change when a single count from the TSI module changes, it is equal to (C_{ref} * I_{ext})/(I_{ref} * PS * NSCN). Sensitivity depends on the configuration used. The typical value listed is based on the following configuration: Iext = 5 µA, EXTCHRG = 4, PS = 128, NSCN = 2, $I_{ref} = 16$ µA, REFCHRG = 15, C_{ref} = 1.0 pF. The minimum sensitivity describes the smallest possible capacitance that can be measured by a single count (this is the best sensitivity but is described as a minimum because it's the smallest number). The minimum sensitivity parameter is based on the following configuration: $I_{ext} = 1$ µA, EXTCHRG = 0, PS = 128, NSCN = 32, $I_{ref} = 32$ µA, REFCHRG = 31, C_{ref}= 0.5 pF
11. Time to do one complete measurement of the electrode. Sensitivity resolution of 0.0133 pF, PS = 0, NSCN = 0, 1 electrode, DELVOL = 2, EXTCHRG = 15.
12. CAPTRM=7, DELVOL=2, REFCHRG=0, EXTCHRG=4, PS=7, NSCN=0F, LPSCNITV=F, LPO is selected (1 kHz), and fixed external capacitance of 20 pF. Data is captured with an average of 7 periods window.

120 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
L6	PTE27	DISABLED		PTE27		UART4_RTS_b					
K6	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK	TSI0_CH1	PTA0	UART0_CTS_b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
J6	PTA1	JTAG_TDI/ EZP_DI	TSI0_CH2	PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
H5	PTA2	JTAG_TDO/ TRACE_SWO/ EZP_DO	TSI0_CH3	PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
J5	PTA3	JTAG_TMS/ SWD_DIO	TSI0_CH4	PTA3	UART0_RTS_b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
K5	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b	TSI0_CH5	PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
L5	PTA5	DISABLED		PTA5		FTM0_CH2	RMII0_RXER/ MII0_RXER	CMP2_OUT	I2S0_RX_BCLK	JTAG_TRST	
G5	VDD	VDD	VDD								
F5	VSS	VSS	VSS								
L4	PTA12	CMP2_IN0	CMP2_IN0	PTA12	CAN0_TX	FTM1_CH0	RMII0_RXD1/ MII0_RXD1		I2S0_TXD	FTM1_QD_ PHA	
K4	PTA13/ LLWU_P4	CMP2_IN1	CMP2_IN1	PTA13/ LLWU_P4	CAN0_RX	FTM1_CH1	RMII0_RXD0/ MII0_RXD0		I2S0_TX_FS	FTM1_QD_ PHB	
J4	PTA14	DISABLED		PTA14	SPI0_PCS0	UART0_TX	RMII0_CRS_ DV/ MII0_RXDV		I2S0_TX_BCLK		
L3	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_RX	RMII0_TXEN/ MII0_TXEN		I2S0_RXD		
K3	PTA16	DISABLED		PTA16	SPI0_SOUT	UART0_CTS_b	RMII0_TXD0/ MII0_TXD0		I2S0_RX_FS		
J3	PTA17	ADC1_SE17	ADC1_SE17	PTA17	SPI0_SIN	UART0_RTS_b	RMII0_TXD1/ MII0_TXD1		I2S0_MCLK	I2S0_CLKIN	
L2	VDD	VDD	VDD								
J2	VSS	VSS	VSS								
L1	PTA18	EXTAL	EXTAL	PTA18		FTM0_FLT2	FTM_CLKIN0				
K1	PTA19	XTAL	XTAL	PTA19		FTM1_FLT0	FTM_CLKIN1		LPT0_ALT1		
J1	RESET_b	RESET_b	RESET_b								
H4	PTB0/ LLWU_P5	ADC0_SE8/ ADC1_SE8/ TSI0_CH0	ADC0_SE8/ ADC1_SE8/ TSI0_CH0	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0	RMII0_MDIO/ MII0_MDIO		FTM1_QD_ PHA		
H3	PTB1	ADC0_SE9/ ADC1_SE9/ TSI0_CH6	ADC0_SE9/ ADC1_SE9/ TSI0_CH6	PTB1	I2C0_SDA	FTM1_CH1	RMII0_MDC/ MII0_MDC		FTM1_QD_ PHB		
H2	PTB2	ADC0_SE12/ TSI0_CH7	ADC0_SE12/ TSI0_CH7	PTB2	I2C0_SCL	UART0_RTS_b	ENET0_1588_ TMR0		FTM0_FLT3		
H1	PTB3	ADC0_SE13/ TSI0_CH8	ADC0_SE13/ TSI0_CH8	PTB3	I2C0_SDA	UART0_CTS_b	ENET0_1588_ TMR1		FTM0_FLT0		
G4	PTB4	ADC1_SE10	ADC1_SE10	PTB4			ENET0_1588_ TMR2		FTM1_FLT0		

120 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
G3	PTB5	ADC1_SE11	ADC1_SE11	PTB5			ENET0_1588_TMR3		FTM2_FLT0		
G2	PTB6	ADC1_SE12	ADC1_SE12	PTB6				FB_AD23			
G1	PTB7	ADC1_SE13	ADC1_SE13	PTB7				FB_AD22			
F4	PTB8			PTB8		UART3_RTS_b		FB_AD21			
F3	PTB9			PTB9	SPI1_PCS1	UART3_CTS_b		FB_AD20			
F2	PTB10	ADC1_SE14	ADC1_SE14	PTB10	SPI1_PCS0	UART3_RX		FB_AD19	FTM0_FLT1		
F1	PTB11	ADC1_SE15	ADC1_SE15	PTB11	SPI1_SCK	UART3_TX		FB_AD18	FTM0_FLT2		
G6	VSS	VSS	VSS								
E5	VDD	VDD	VDD								
E1	PTB16	TSI0_CH9	TSI0_CH9	PTB16	SPI1_SOUT	UART0_RX		FB_AD17	EWM_IN		
E2	PTB17	TSI0_CH10	TSI0_CH10	PTB17	SPI1_SIN	UART0_TX		FB_AD16	EWM_OUT_b		
E3	PTB18	TSI0_CH11	TSI0_CH11	PTB18	CAN0_TX	FTM2_CH0	I2S0_TX_BCLK	FB_AD15	FTM2_QD_PHA		
E4	PTB19	TSI0_CH12	TSI0_CH12	PTB19	CAN0_RX	FTM2_CH1	I2S0_TX_FS	FB_OE_b	FTM2_QD_PHB		
D1	PTB20			PTB20	SPI2_PCS0			FB_AD31	CMP0_OUT		
D2	PTB21			PTB21	SPI2_SCK			FB_AD30	CMP1_OUT		
D5	PTB22			PTB22	SPI2_SOUT			FB_AD29	CMP2_OUT		
D4	PTB23			PTB23	SPI2_SIN	SPI0_PCS5		FB_AD28			
D3	PTC0	ADC0_SE14/TSI0_CH13	ADC0_SE14/TSI0_CH13	PTC0	SPI0_PCS4	PDB0_EXTRG	I2S0_TXD	FB_AD14			
C1	PTC1/LLWU_P6	ADC0_SE15/TSI0_CH14	ADC0_SE15/TSI0_CH14	PTC1/LLWU_P6	SPI0_PCS3	UART1_RTS_b	FTM0_CH0	FB_AD13			
C2	PTC2	ADC0_SE4b/CMP1_IN0/TSI0_CH15	ADC0_SE4b/CMP1_IN0/TSI0_CH15	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1	FB_AD12			
B1	PTC3/LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	FB_CLKOUT			
G7	VDD	VDD	VDD								
A3	PTC4/LLWU_P8			PTC4/LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3	FB_AD11	CMP1_OUT		
B4	PTC5/LLWU_P9			PTC5/LLWU_P9	SPI0_SCK		LPT0_ALT2	FB_AD10	CMP0_OUT		
C5	PTC6/LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/LLWU_P10	SPI0_SOUT	PDB0_EXTRG		FB_AD9			
B5	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN			FB_AD8			
A4	PTC8	ADC1_SE4b/CMP0_IN2	ADC1_SE4b/CMP0_IN2	PTC8		I2S0_MCLK	I2S0_CLKIN	FB_AD7			
C6	PTC9	ADC1_SE5b/CMP0_IN3	ADC1_SE5b/CMP0_IN3	PTC9			I2S0_RX_BCLK	FB_AD6	FTM2_FLT0		
D6	PTC10	ADC1_SE6b/CMP0_IN4	ADC1_SE6b/CMP0_IN4	PTC10	I2C1_SCL		I2S0_RX_FS	FB_AD5			
A5	PTC11/LLWU_P11	ADC1_SE7b	ADC1_SE7b	PTC11/LLWU_P11	I2C1_SDA		I2S0_RXD	FB_RW_b			



	1	2	3	4	5	6	7	8	9	10	11	
A	NC	NC	PTC4/ LLWU_P8	PTC8	PTC11/ LLWU_P11	PTC15	PTC16	PTD1	PTD5	PTD7	PTE0	A
B	PTC3/ LLWU_P7	NC	NC	PTC5/ LLWU_P9	PTC7	PTC13	PTC17	PTD0/ LLWU_P12	PTD4/ LLWU_P14	PTD6/ LLWU_P15	PTE2/ LLWU_P1	B
C	PTC1/ LLWU_P6	PTC2	NC	VDD	PTC6/ LLWU_P10	PTC9	PTC14	PTC18	PTD3	PTE1/ LLWU_P0	PTE4/ LLWU_P2	C
D	PTB20	PTB21	PTC0	PTB23	PTB22	PTC10	PTC12	PTC19	PTD2/ LLWU_P13	PTE3	PTE5	D
E	PTB16	PTB17	PTB18	PTB19	VDD	VSS	VDD	VSS	PTE6	PTE7	PTE8	E
F	PTB11	PTB10	PTB9	PTB8	VSS		VDD	PTE9	PTE10	PTE11	PTE12	F
G	PTB7	PTB6	PTB5	PTB4	VDD	VSS	VDD	VREGIN	VOUT33	USB0_DM	USB0_DP	G
H	PTB3	PTB2	PTB1	PTB0/ LLWU_P5	PTA2	PTE26	PTE25	ADC1_DM1/ OP1_DM0	ADC1_DP1/ OP1_DP0/ OP1_DM1	ADC0_DM1/ OP0_DM0	ADC0_DP1/ OP0_DP0	H
J	RESET_b	VSS	PTA17	PTA14	PTA3	PTA1	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DP/ ADC0_DP0/ ADC1_DP3	J
K	PTA19	VDD	PTA16	PTA13/ LLWU_P4	PTA4/ LLWU_P3	PTA0	DAC1_OUT/ CMP2_IN3/ ADC1_SE23/ OP0_DP5/ OP1_DP5	VSSA	VREFL	VREFH	VDDA	K
L	PTA18	VDD	PTA15	PTA12	PTA5	PTE27	PTE24	VBAT	EXTAL32	XTAL32	DAC0_OUT/ CMP1_IN3/ ADC0_SE23/ OP0_DP4/ OP1_DP4	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 29. K60 120 WLCSP Pinout Diagram

9 Revision History

The following table provides a revision history for this document.

Table 53. Revision History

Rev. No.	Date	Substantial Changes
6.1	08/2012	Initial public release

Table continues on the next page...