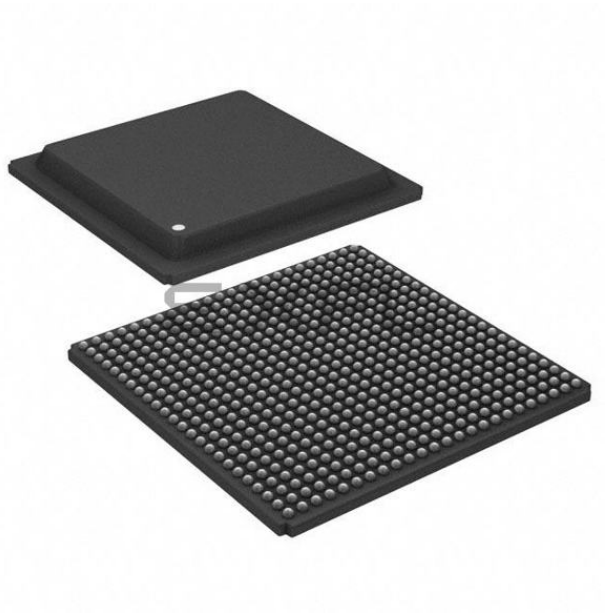

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed/Floating Point
Interface	Host Interface, Link Port, Multi-Processor
Clock Rate	500MHz
Non-Volatile Memory	External
On-Chip RAM	1.5MB
Voltage - I/O	2.50V
Voltage - Core	1.05V
Operating Temperature	-40°C ~ 85°C (TC)
Mounting Type	Surface Mount
Package / Case	576-BBGA
Supplier Device Package	576-BGA-ED (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-ts202sabpz050

GENERAL DESCRIPTION

The ADSP-TS202S TigerSHARC processor is an ultrahigh performance, static superscalar processor optimized for large signal processing tasks and communications infrastructure. The DSP combines very wide memory widths with dual computation blocks—supporting floating-point (IEEE 32-bit and extended precision 40-bit) and fixed-point (8-, 16-, 32-, and 64-bit) processing—to set a new standard of performance for digital signal processors. The TigerSHARC static superscalar architecture lets the DSP execute up to four instructions each cycle, performing 24 fixed-point (16-bit) operations or six floating-point operations.

Four independent 128-bit wide internal data buses, each connecting to the six 2M bit memory banks, enable quad-word data, instruction, and I/O accesses and provide 28G bytes per second of internal memory bandwidth. Operating at 500 MHz, the ADSP-TS202S processor's core has a 2.0 ns instruction cycle time. Using its single-instruction, multiple-data (SIMD) features, the ADSP-TS202S processor can perform four billion 40-bit MACS or one billion 80-bit MACS per second. Table 1 shows the DSP's performance benchmarks.

Table 1. General-Purpose Algorithm Benchmarks at 500 MHz

Benchmark	Speed	Clock Cycles
32-bit algorithm, 1 billion MACS/s peak performance		
1K point complex FFT[1] (Radix 2)	18.8 µs	9419
64K point complex FFT[1] (Radix 2)	2.8 ms	1397544
FIR filter (per real tap)	1 ns	0.5
[8 × 8][8 × 8] matrix multiply (complex, floating-point)	2.8 µs	1399
16-bit algorithm, 4 billion MACS/s peak performance		
256 point complex FFT[1] (Radix 2)	1.9 µs	928
I/O DMA transfer rate		
External port	1G bytes/s	n/a
Link ports (each)	1G bytes/s	n/a

[1] Cache preloaded.

The ADSP-TS202S processor is code-compatible with the other TigerSHARC processors.

The Functional Block Diagram on Page 1 shows the ADSP-TS202S processor's architectural blocks. These blocks include

- Dual compute blocks, each consisting of an ALU, multiplier, 64-bit shifter, and 32-word register file and associated data alignment buffers (DABs)
- Dual integer ALUs (IALUs), each with its own 31-word register file for data addressing and a status register
- A program sequencer with instruction alignment buffer (IAB) and branch target buffer (BTB)
- An interrupt controller that supports hardware and software interrupts, supports level- or edge-triggers, and supports prioritized, nested interrupts
- Four 128-bit internal data buses, each connecting to the six 2M-bit memory banks
- On-chip DRAM (12M-bit)
- An external port that provides the interface to host processors, multiprocessing space (DSPs), off-chip memory-mapped peripherals, and external SRAM and SDRAM
- A 14-channel DMA controller
- Four full-duplex LVDS link ports
- Two 64-bit interval timers and timer expired pin
- An 1149.1 IEEE compliant JTAG test access port for on-chip emulation

Figure 2 shows a typical single-processor system with external SRAM and SDRAM. Figure 4 on Page 8 shows a typical multiprocessor system.

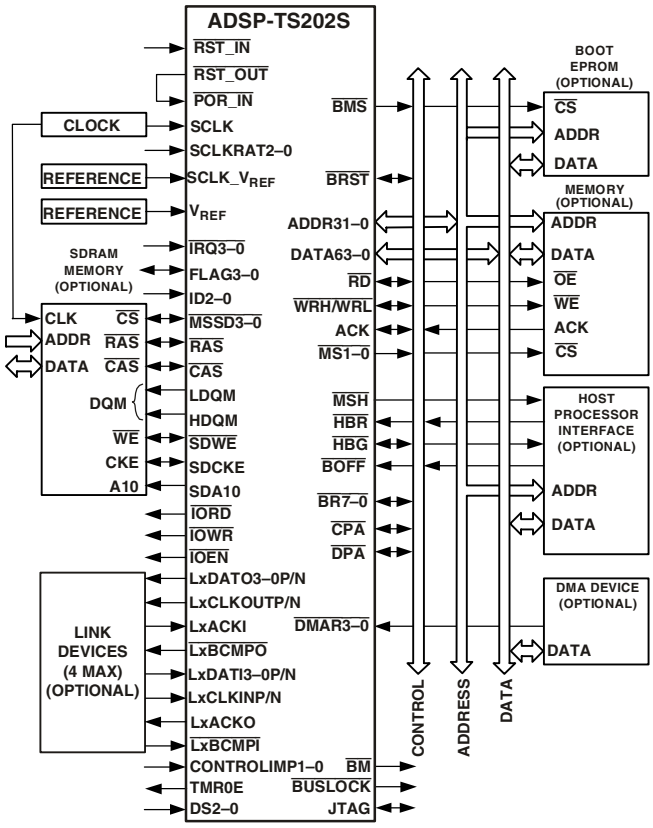

Figure 2. ADSP-TS202S Single-Processor System with External SDRAM

ADSP-TS202S processor accesses of the host as slave or pipelined for host accesses of the ADSP-TS202S processor as slave. Each protocol has programmable transmission parameters, such as idle cycles, pipe depth, and internal wait cycles.

The host interface supports burst transactions initiated by a host processor. After the host issues the starting address of the burst and asserts the $\overline{\text{BRST}}$ signal, the DSP increments the address internally while the host continues to assert $\overline{\text{BRST}}$.

The host interface provides a deadlock recovery mechanism that enables a host to recover from deadlock situations involving the DSP. The $\overline{\text{BOFF}}$ signal provides the deadlock recovery mechanism. When the host asserts $\overline{\text{BOFF}}$, the DSP backs off the current transaction and asserts $\overline{\text{HBG}}$ and relinquishes the external bus.

The host can directly read or write the internal memory of the ADSP-TS202S processor, and it can access most of the DSP registers, including DMA control (TCB) registers. Vector interrupts support efficient execution of host commands.

Multiprocessor Interface

The ADSP-TS202S processor offers powerful features tailored to multiprocessing DSP systems through the external port and link ports. This multiprocessing capability provides highest bandwidth for interprocessor communication, including

- Up to eight DSPs on a common bus
- On-chip arbitration for glueless multiprocessing
- Link ports for point-to-point communication

The external port and link ports provide integrated, glueless multiprocessing support.

The external port supports a unified address space (see Figure 3) that enables direct interprocessor accesses of each ADSP-TS202S processor's internal memory and registers. The DSP's on-chip distributed bus arbitration logic provides simple, glueless connection for systems containing up to eight ADSP-TS202S processors and a host processor. Bus arbitration has a rotating priority. Bus lock supports indivisible read-modify-write sequences for semaphores. A bus fairness feature prevents one DSP from holding the external bus too long.

The DSP's four link ports provide a second path for interprocessor communications with throughput of 4G bytes per second. The cluster bus provides 1G bytes per second throughput—with a total of 4G bytes per second interprocessor bandwidth (limited by SOC bandwidth).

SDRAM Controller

The SDRAM controller controls the ADSP-TS202S processor's transfers of data to and from external synchronous DRAM (SDRAM) at a throughput of 32 bits or 64 bits per SCLK cycle using the external port and SDRAM control pins.

The SDRAM interface provides a glueless interface with standard SDRAMs—16M bits, 64M bits, 128M bits, 256M bits, and 512M bits. The DSP supports directly a maximum of four banks of 64M words × 32 bits of SDRAM. The SDRAM interface is mapped in external memory in each DSP's unified memory map.

EPROM Interface

The ADSP-TS202S processor can be configured to boot from an external 8-bit EPROM at reset through the external port. An automatic process (which follows reset) loads a program from the EPROM into internal memory. This process uses 16 wait cycles for each read access. During booting, the $\overline{\text{BMS}}$ pin functions as the EPROM chip select signal. The EPROM boot procedure uses DMA Channel 0, which packs the bytes into 32-bit instructions. Applications can also access the EPROM (write flash memories) during normal operation through DMA.

The EPROM or flash memory interface is not mapped in the DSP's unified memory map. It is a byte address space limited to a maximum of 16M bytes (24 address bits). The EPROM or flash memory interface can be used after boot via a DMA.

DMA CONTROLLER

The ADSP-TS202S processor's on-chip DMA controller, with 14 DMA channels, provides zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to the DSP's core, enabling DMA operations to occur while the DSP's core continues to execute program instructions.

The DMA controller performs DMA transfers between internal memory and external memory and memory-mapped peripherals, the internal memory of other DSPs on a common bus, a host processor, or link port I/O; between external memory and external peripherals or link port I/O; and between an external bus master and internal memory or link port I/O. The DMA controller performs the following DMA operations:

- External port block transfers. Four dedicated bidirectional DMA channels transfer blocks of data between the DSP's internal memory and any external memory or memory-mapped peripheral on the external bus. These transfers support master mode and handshake mode protocols.
- Link port transfers. Eight dedicated DMA channels (four transmit and four receive) transfer quad-word data only between link ports and between a link port and internal or external memory. These transfers only use handshake mode protocol. DMA priority rotates between the four receive channels.
- AutoDMA transfers. Two dedicated unidirectional DMA channels transfer data received from an external bus master to internal memory or link port I/O. These transfers only use slave mode protocol, and an external bus master must initiate the transfer.

The DMA controller provides these additional features:

- Flyby transfers. Flyby operations only occur through the external port (DMA channel 0) and do not involve the DSP's core. The DMA controller acts as a conduit to transfer data from an external I/O device and external SDRAM memory. During a transaction, the DSP relinquishes the

LINK PORTS (LVDS)

The DSP's four full-duplex link ports each provide additional four-bit receive and four-bit transmit I/O capability, using low voltage, differential-signal (LVDS) technology. With the ability to operate at a double data rate—latching data on both the rising and falling edges of the clock—running at 500 MHz, each link port can support up to 500M bytes per second per direction, for a combined maximum throughput of 4G bytes per second.

The link ports provide an optional communications channel that is useful in multiprocessor systems for implementing point-to-point interprocessor communications. Applications can also use the link ports for booting.

Each link port has its own triple-buffered quad-word input and double-buffered quad-word output registers. The DSP's core can write directly to a link port's transmit register and read from a receive register, or the DMA controller can perform DMA transfers through eight (four transmit and four receive) dedicated link port DMA channels.

Each link port direction has three signals that control its operation. For the transmitter, LxCLKOUT is the output transmit clock, LxACKI is the handshake input to control the data flow, and the $\overline{\text{LxBCMPO}}$ output indicates that the block transfer is complete. For the receiver, LxCLKIN is the input receive clock, LxACKO is the handshake output to control the data flow, and the $\overline{\text{LxBCMPI}}$ input indicates that the block transfer is complete. The LxDATO3–0 pins are the data output bus for the transmitter and the LxDATI3–0 pins are the input data bus for the receiver.

Applications can program separate error detection mechanisms for transmit and receive operations (applications can use the checksum mechanism to implement consecutive link port transfers), the size of data packets, and the speed at which bytes are transmitted.

TIMER AND GENERAL-PURPOSE I/O

The ADSP-TS202S processor has a timer pin (TMR0E) that generates output when a programmed timer counter has expired and four programmable general-purpose I/O pins (FLAG3–0) that can function as either single-bit input or output. As outputs, these pins can signal peripheral devices; as inputs, they can provide the test for conditional branching.

RESET AND BOOTING

The ADSP-TS202S processor has three levels of reset:

- Power-up reset—after power-up of the system (SCLK, all static inputs, and strap pins are stable), the $\overline{\text{RST\_IN}}$ pin must be asserted (low).
- Normal reset—for any chip reset following the power-up reset, the $\overline{\text{RST\_IN}}$ pin must be asserted (low).
- DSP-core reset—when setting the SWRST bit in EMUCTL, the DSP core is reset, but not the external port or I/O.

For normal operations, tie the $\overline{\text{RST\_OUT}}$ pin to the $\overline{\text{POR\_IN}}$ pin.

After reset, the ADSP-TS202S processor has four boot options for beginning operation:

- Boot from EPROM.
- Boot by an external master (host or another ADSP-TS202S processor).
- Boot by link port.
- No boot—start running from memory address selected with one of the $\overline{\text{IRQ3–0}}$ interrupt signals. See Table 2.

Using the "no boot" option, the ADSP-TS202S processor must start running from memory when one of the interrupts is asserted.

Table 2. No Boot, Run from Memory Addresses

Interrupt	Address
$\overline{\text{IRQ0}}$	0x3000 0000 (External Memory)
$\overline{\text{IRQ1}}$	0x3800 0000 (External Memory)
$\overline{\text{IRQ2}}$	0x8000 0000 (External Memory)
$\overline{\text{IRQ3}}$	0x0000 0000 (Internal Memory)

The ADSP-TS202S processor core always exits from reset in the idle state and waits for an interrupt. Some of the interrupts in the interrupt vector table are initialized and enabled after reset.

For more information on boot options, see the *EE-200: ADSP-TS20x TigerSHARC Processor Boot Loader Kernels Operation* on the Analog Devices website (www.analog.com).

CLOCK DOMAINS

The DSP uses calculated ratios of the SCLK clock to operate as shown in Figure 5. The instruction execution rate is equal to CCLK. A PLL from SCLK generates CCLK, which is phase-locked. The SCLKRATx pins define the clock multiplication of SCLK to CCLK (see Table 4 on Page 12). The link port clock is generated from CCLK via a software programmable divisor, and the SOC bus operates at 1/2 CCLK. Memory transfers to external, and link port buffers operate at the SOCCLK rate. SCLK also provides clock input for the external bus interface and defines the ac specification reference for the external bus signals. The external bus interface runs at the SCLK frequency. The maximum SCLK frequency is one quarter the internal DSP clock (CCLK) frequency.

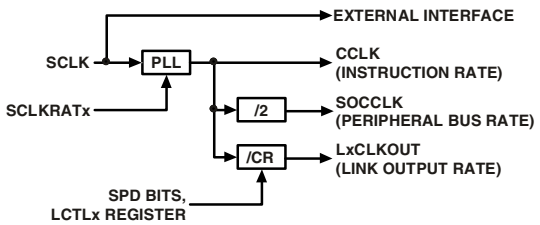

Figure 5. Clock Domains

Table 6. Pin Definitions—External Port Arbitration

Signal	Type	Term	Description
$\overline{BR7–0}$	I/O	V_{DD_IO}[1]	Multiprocessing Bus Request Pins. Used by the DSPs in a multiprocessor system to arbitrate for bus mastership. Each DSP drives its own $\overline{BRx}$ line (corresponding to the value of its ID2–0 inputs) and monitors all others. In systems with fewer than eight DSPs, set the unused $\overline{BRx}$ pins high (V_{DD_IO}).
ID2–0	I (pd)	na	Multiprocessor ID. Indicates the DSP's ID, from which the DSP determines its order in a multiprocessor system. These pins also indicate to the DSP which bus request ($\overline{BR0}$–$\overline{BR7}$) to assert when requesting the bus: 000 = $\overline{BR0}$, 001 = $\overline{BR1}$, 010 = $\overline{BR2}$, 011 = $\overline{BR3}$, 100 = $\overline{BR4}$, 101 = $\overline{BR5}$, 110 = $\overline{BR6}$, or 111 = $\overline{BR7}$. ID2–0 must have a constant value during system operation and can change during reset only.
$\overline{BM}$	O	na	Bus Master. The current bus master DSP asserts $\overline{BM}$. For debugging only. At reset this is a strap pin. For more information, see Table 16 on Page 20.
$\overline{BOFF}$	I	epu	Back Off. A deadlock situation can occur when the host and a DSP try to read from each other's bus at the same time. When deadlock occurs, the host can assert $\overline{BOFF}$ to force the DSP to relinquish the bus before completing its outstanding transaction.
$\overline{BUSLOCK}$	O/T (pu_0)	na	Bus Lock Indication. Provides an indication that the current bus master has locked the bus. At reset, this is a strap pin. For more information, see Table 16 on Page 20.
$\overline{HBR}$	I	epu	Host Bus Request. A host must assert $\overline{HBR}$ to request control of the DSP's external bus. When $\overline{HBR}$ is asserted in a multiprocessing system, the bus master relinquishes the bus and asserts $\overline{HBG}$ once the outstanding transaction is finished.
$\overline{HBG}$	I/O/T (pu_0)	epu[2]	Host Bus Grant. Acknowledges $\overline{HBR}$ and indicates that the host can take control of the external bus. When relinquishing the bus, the master DSP three-states the ADDR31–0, DATA63–0, $\overline{MSH}$, $\overline{MSSD3–0}$, $\overline{MS1–0}$, $\overline{RD}$, $\overline{WRL}$, $\overline{WRH}$, $\overline{BMS}$, $\overline{BRST}$, $\overline{IORD}$, $\overline{IOWR}$, $\overline{IOEN}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, SDA10, SDCKE, LDQM, and HDQM pins, and the DSP puts the SDRAM in self-refresh mode. The DSP asserts $\overline{HBG}$ until the host deasserts $\overline{HBR}$. In multiprocessor systems, the current bus master DSP drives $\overline{HBG}$, and all slave DSPs monitor it.
$\overline{CPA}$	I/O/OD (pu_od_0)	epu[2]	Core Priority Access. Asserted while the DSP's core accesses external memory. This pin enables a slave DSP to interrupt a master DSP's background DMA transfers and gain control of the external bus for core-initiated transactions. $\overline{CPA}$ is an open-drain output, connected to all DSPs in the system. If not required in the system, leave $\overline{CPA}$ unconnected (external pull-ups will be required for DSP ID = 1 through ID = 7).
$\overline{DPA}$	I/O/OD (pu_od_0)	epu[2]	DMA Priority Access. Asserted while a high priority DSP DMA channel accesses external memory. This pin enables a high priority DMA channel on a slave DSP to interrupt transfers of a normal priority DMA channel on a master DSP and gain control of the external bus for DMA-initiated transactions. $\overline{DPA}$ is an open-drain output, connected to all DSPs in the system. If not required in the system, leave $\overline{DPA}$ unconnected (external pull-ups will be required for DSP ID = 1 through ID = 7).

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on DSP ID = 0; **pu_0** = internal pull-up 5 kΩ on DSP ID = 0; **pu_od_0** = internal pull-up 500 Ω on DSP ID = 0; **pd_m** = internal pull-down 5 kΩ on DSP bus master; **pu_m** = internal pull-up 5 kΩ on DSP bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 22.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

[1] The $\overline{BRx}$ pin matching the ID2–0 input selection for the processor should be left nc if unused. For example, the processor with ID = 000 has $\overline{BR0}$ = nc and $\overline{BR7–1}$ = V_{DD_IO}.
[2] This external pull-up resistor may be omitted for the ID = 000 TigerSHARC processor.

Table 8. Pin Definitions—External Port SDRAM Controller (Continued)

Signal	Type	Term	Description
SDA10	O/T (pu_0)	nc	SDRAM Address Bit 10. Separate A10 signals enable SDRAM refresh operation while the DSP executes non-SDRAM transactions.
SDCKE	I/O/T (pu_m/ pd_m)	nc	SDRAM Clock Enable. Activates the SDRAM clock for SDRAM self-refresh or suspend modes. A slave DSP in a multiprocessor system does not have the pull-up or pull-down. A master DSP (or ID = 0 in a single processor system) has a pull-up before granting the bus to the host, except when the SDRAM is put in self refresh mode. In self refresh mode, the master has a pull-down before granting the bus to the host.
$\overline{\text{SDWE}}$	I/O/T (pu_0)	nc	SDRAM Write Enable. When sampled low while $\overline{\text{CAS}}$ is active, $\overline{\text{SDWE}}$ indicates an SDRAM write access. When sampled high while $\overline{\text{CAS}}$ is active, $\overline{\text{SDWE}}$ indicates an SDRAM read access. In other SDRAM accesses, $\overline{\text{SDWE}}$ defines the type of operation to execute according to SDRAM specification.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on DSP ID = 0; **pu_0** = internal pull-up 5 kΩ on DSP ID = 0; **pu_od_0** = internal pull-up 500 Ω on DSP ID = 0; **pd_m** = internal pull-down 5 kΩ on DSP bus master; **pu_m** = internal pull-up 5 kΩ on DSP bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 22.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

Table 9. Pin Definitions—JTAG Port

Signal	Type	Term	Description
$\overline{\text{EMU}}$	O/OD	nc[1]	Emulation. Connected to the DSP's JTAG emulator target board connector only.
TCK	I	epd or epu[1]	Test Clock (JTAG). Provides an asynchronous clock for JTAG scan.
TDI	I (pu_ad)	nc[1]	Test Data Input (JTAG). A serial data input of the scan path.
TDO	O/T	nc[1]	Test Data Output (JTAG). A serial data output of the scan path.
TMS	I (pu_ad)	nc[1]	Test Mode Select (JTAG). Used to control the test state machine.
$\overline{\text{TRST}}$	I/A (pu_ad)	na	Test Reset (JTAG). Resets the test state machine. $\overline{\text{TRST}}$ must be asserted or pulsed low after power-up for proper device operation. For more information, see Reset and Booting on Page 9.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on DSP ID = 0; **pu_0** = internal pull-up 5 kΩ on DSP ID = 0; **pu_od_0** = internal pull-up 500 Ω on DSP ID = 0; **pd_m** = internal pull-down 5 kΩ on DSP bus master; **pu_m** = internal pull-up 5 kΩ on DSP bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 22.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

[1] See the reference on Page 11 to the JTAG emulation technical reference EE-68.

Table 10. Pin Definitions—Flags, Interrupts, and Timer

Signal	Type	Term	Description
FLAG3–0	I/O/A (pu)	nc	FLAG pins. Bidirectional input/output pins can be used as program conditions. Each pin can be configured individually for input or for output. FLAG3–0 are inputs after power-up and reset.
$\overline{\text{IRQ3–0}}$	I/A (pu)	nc	Interrupt Request. When asserted, the DSP generates an interrupt. Each of the $\overline{\text{IRQ3–0}}$ pins can be independently set for edge-triggered or level-sensitive operation. After reset, these pins are disabled unless the $\overline{\text{IRQ3–0}}$ strap option and interrupt vectors are initialized for booting.
TMR0E	O	na	Timer 0 expires. This output pulses whenever timer 0 expires. At reset, this is a strap pin. For more information, see Table 16 on Page 20.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on DSP ID = 0; **pu_0** = internal pull-up 5 kΩ on DSP ID = 0; **pu_od_0** = internal pull-up 500 Ω on DSP ID = 0; **pd_m** = internal pull-down 5 kΩ on DSP bus master; **pu_m** = internal pull-up 5 kΩ on DSP bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 22.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

Table 11. Pin Definitions—Link Ports

Signal	Type	Term	Description
LxDATO3–0P	O	nc	Link Ports 3–0 Data 3–0 Transmit LVDS P
LxDATO3–0N	O	nc	Link Ports 3–0 Data 3–0 Transmit LVDS N
LxCLKOUTP	O	nc	Link Ports 3–0 Transmit Clock LVDS P
LxCLKOUTN	O	nc	Link Ports 3–0 Transmit Clock LVDS N
LxACKI	I (pd)	nc	Link Ports 3–0 Receive Acknowledge. Using this signal, the receiver indicates to the transmitter that it may continue the transmission.
$\overline{\text{LxBCMPO}}$	O (pu)	nc	Link Ports 3–0 Block Completion. When the transmission is executed using DMA, this signal indicates to the receiver that the transmitted block is completed. The pull-up resistor is present on $\overline{\text{L0BCMPO}}$ only. At reset, the $\overline{\text{L1BCMPO}}$, $\overline{\text{L2BCMPO}}$, and $\overline{\text{L3BCMPO}}$ pins are strap pins. For more information, see Table 16 on Page 20.
LxDATI3–0P	I	V_{DD_IO}	Link Ports 3–0 Data 3–0 Receive LVDS P
LxDATI3–0N	I	V_{DD_IO}	Link Ports 3–0 Data 3–0 Receive LVDS N
LxCLKINP	I/A	V_{DD_IO}	Link Ports 3–0 Receive Clock LVDS P
LxCLKINN	I/A	V_{DD_IO}	Link Ports 3–0 Receive Clock LVDS N
LxACKO	O	nc	Link Ports 3–0 Transmit Acknowledge. Using this signal, the receiver indicates to the transmitter that it may continue the transmission.
$\overline{\text{LxBCMPI}}$	I (pd_l)	V_{SS}	Link Ports 3–0 Block Completion. When the reception is executed using DMA, this signal indicates to the receiver that the transmitted block is completed.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on DSP ID = 0; **pu_0** = internal pull-up 5 kΩ on DSP ID = 0; **pu_od_0** = internal pull-up 500 Ω on DSP ID = 0; **pd_m** = internal pull-down 5 kΩ on DSP bus master; **pu_m** = internal pull-up 5 kΩ on DSP bus master; **pu_ad** = internal pull-up 40 kΩ; **pd_l** = internal pull-down 50 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 22.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

Table 15. Pin Definitions—Power, Ground, and Reference

Signal	Type	Term	Description
V_{DD}	P	na	V_{DD} Pins for Internal Logic
V_{DD_A}	P	na	V_{DD} Pins for Analog Circuits. Pay critical attention to bypassing this supply.
V_{DD_IO}	P	na	V_{DD} Pins for I/O Buffers
V_{DD_DRAM}	P	na	V_{DD} Pins for Internal DRAM
V_{REF}	I	na	Reference voltage defines the trip point for all input buffers, except SCLK, $\overline{RST\_IN}$, $\overline{POR\_IN}$, $\overline{IRQ3–0}$, FLAG3–0, $\overline{DMAR3–0}$, ID2–0, CONTROLIMP1–0, LxDATO3–0P/N, LxCLKOUTP/N, LxDATI3–0P/N, LxCLKINP/N, TCK, TDI, TMS, and $\overline{TRST}$. V_{REF} can be connected to a power supply or set by a voltage divider circuit as shown in Figure 6. For more information, see Filtering Reference Voltage and Clocks on Page 10.
$SCLK\_V_{REF}$	I	na	System Clock Reference. Connect this pin to a reference voltage as shown in Figure 7. For more information, see Filtering Reference Voltage and Clocks on Page 10.
V_{SS}	G	na	Ground Pins
NC	—	nc	No Connect. Do not connect these pins to anything (not to any supply, signal, or each other). These pins are reserved and must be left unconnected.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on DSP ID = 0; **pu_0** = internal pull-up 5 kΩ on DSP ID = 0; **pu_od_0** = internal pull-up 500 Ω on DSP ID = 0; **pd_m** = internal pull-down 5 kΩ on DSP bus master; **pu_m** = internal pull-up 5 kΩ on DSP bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 22.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

STRAP PIN FUNCTION DESCRIPTIONS

Some pins have alternate functions at reset. Strap options set DSP operating modes. During reset, the DSP samples the strap option pins. Strap pins have an internal pull-up or pull-down for the default value. If a strap pin is not connected to an overdriving external pull-up, pull-down, or logic load, the DSP samples the default value during reset. If strap pins are connected to logic inputs, a stronger external pull-up or pull-down may be required to ensure default value depending on leakage and/or low level input current of the logic load. To set a mode other than the default mode, connect the strap pin to a sufficiently stronger external pull-up or pull-down. Table 16 lists and describes each of the DSP's strap pins.

Table 16. Pin Definitions—I/O Strap Pins

Signal	Type (at Reset)	On Pin …	Description
EBOOT	I (pd_0)	$\overline{\text{BMS}}$	EPROM Boot 0 = boot from EPROM immediately after reset (default) 1 = idle after reset and wait for an external device to boot DSP through the external port or a link port
IRQEN	I (pd)	$\overline{\text{BM}}$	Interrupt Enable 0 = disable and set $\overline{\text{IRQ3–0}}$ interrupts to edge-sensitive after reset (default) 1 = enable and set $\overline{\text{IRQ3–0}}$ interrupts to level-sensitive immediately after reset
LINK_DWIDTH	I (pd)	TMR0E	Link Port Input Default Data Width 0 = 1-bit (default) 1 = 4-bit
SYS_REG_WE	I (pd_0)	$\overline{\text{BUSLOCK}}$	SYSCON and SDRCON Write Enable 0 = one-time writable after reset (default) 1 = always writable
TM1	I (pu)	$\overline{\text{L1BCMPO}}$	Test Mode 1. Do not overdrive default value during reset.
TM2	I (pu)	$\overline{\text{L2BCMPO}}$	Test Mode 2. Do not overdrive default value during reset.
TM3	I (pu)	$\overline{\text{L3BCMPO}}$	Test Mode 3. Do not overdrive default value during reset.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on DSP ID = 0; **pu_0** = internal pull-up 5 kΩ on DSP ID = 0; **pu_od_0** = internal pull-up 500 Ω on DSP ID = 0; **pd_m** = internal pull-down 5 kΩ on DSP bus master; **pu_m** = internal pull-up 5 kΩ on DSP bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 22.

When default configuration is used, no external resistor is needed on the strap pins. To apply other configurations, a 500 Ω resistor connected to V_{DD_IO} is required. If providing external pull-downs, do not strap these pins directly to V_{SS}; the strap pins require 500 Ω resistor straps.

All strap pins are sampled on the rising edge of $\overline{\text{RST\_IN}}$ (deassertion edge). Each pin latches the strapped pin state (state of the strap pin at the rising edge of $\overline{\text{RST\_IN}}$). Shortly after deassertion of $\overline{\text{RST\_IN}}$, these pins are reconfigured to their normal functionality.

These strap pins have an internal pull-down resistor, pull-up resistor, or no-resistor (three-state) on each pin. The resistor type, which is connected to the I/O pad, depends on whether $\overline{\text{RST\_IN}}$ is active (low) or if $\overline{\text{RST\_IN}}$ is deasserted (high). Table 17 shows the resistors that are enabled during active reset and during normal operation.

Table 17. Strap Pin Internal Resistors—Active Reset ($\overline{\text{RST\_IN}}$ = 0) vs. Normal Operation ($\overline{\text{RST\_IN}}$ = 1)

Pin	$\overline{\text{RST\_IN}}$ = 0	$\overline{\text{RST\_IN}}$ = 1
$\overline{\text{BMS}}$	(pd_0)	(pu_0)
$\overline{\text{BM}}$	(pd)	Driven
TMR0E	(pd)	Driven
$\overline{\text{BUSLOCK}}$	(pd_0)	(pu_0)
$\overline{\text{L1BCMPO}}$	(pu)	Driven
$\overline{\text{L2BCMPO}}$	(pu)	Driven
$\overline{\text{L3BCMPO}}$	(pu)	Driven

pd = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ;
pd_0 = internal pull-down 5 kΩ on DSP ID = 0;
pu_0 = internal pull-up 5 kΩ on DSP ID = 0

Table 18. Maximum Duty Cycle for Input Transient Voltage

V_{IN} Max (V)[1]	V_{IN} Min (V)[1]	Maximum Duty Cycle[2]
+3.63	–0.33	100%
+3.64	–0.34	90%
+3.70	–0.40	50%
+3.78	–0.48	30%
+3.86	–0.56	17%
+3.93	–0.63	10%

[1] The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the voltages specified and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.

[2] Duty cycle refers to the percentage of time the signal exceeds the value for the 100% case. This is equivalent to the measured duration of a single instance of overshoot or undershoot as a percentage of the period of occurrence. The practical worst case for period of occurrence for either overshoot or undershoot is $2 \times t_{SCLK}$.

ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}	High Level Output Voltage[1]	@ V_{DD_IO} = Min, I_{OH} = –2 mA	2.18		V
V_{OL}	Low Level Output Voltage[1]	@ V_{DD_IO} = Min, I_{OL} = 4 mA		0.4	V
I_{IH}	High Level Input Current	@ V_{DD_IO} = Max, V_{IN} = V_{IH} Max		20	µA
I_{IH_PU}	High Level Input Current	@ V_{DD_IO} = Max, V_{IN} = V_{IH} Max		20	µA
I_{IH_PD}	High Level Input Current	@ V_{DD_IO} = Max, V_{IN} = V_{DD_IO} Max	0.3	0.76	mA
$I_{IH\_PD\_L}$	High Level Input Current	@ V_{DD_IO} = Max, V_{IN} = V_{IH} Max	30	76	µA
I_{IL}	Low Level Input Current	@ V_{DD_IO} = Max, V_{IN} = 0 V		20	µA
I_{IL_PU}	Low Level Input Current	@ V_{DD_IO} = Max, V_{IN} = 0 V	0.3	0.76	mA
$I_{IL\_PU\_AD}$	Low Level Input Current	@ V_{DD_IO} = Max, V_{IN} = 0 V	30	100	µA
I_{OZH}	Three-State Leakage Current High	@ V_{DD_IO} = Max, V_{IN} = V_{IH} Max		50	µA
I_{OZH_PD}	Three-State Leakage Current High	@ V_{DD_IO} = Max, V_{IN} = V_{DD_IO} Max	0.3	0.76	mA
I_{OZL}	Three-State Leakage Current Low	@ V_{DD_IO} = Max, V_{IN} = 0 V		20	µA
I_{OZL_PU}	Three-State Leakage Current Low	@ V_{DD_IO} = Max, V_{IN} = 0 V	0.3	0.76	mA
$I_{OZL\_PU\_AD}$	Three-State Leakage Current Low	@ V_{DD_IO} = Max, V_{IN} = 0 V	30	100	µA
I_{OZL_OD}	Three-State Leakage Current Low	@ V_{DD_IO} = Max, V_{IN} = 0 V	4	7.6	mA
C_{IN}	Input Capacitance[2, 3]	@ f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		3	pF

Parameter name suffix conventions: no suffix = applies to pins without pull-up or pull-down resistors; **_PD** = applies to pin types (pd) or (pd_0); **_PU** = applies to pin types (pu) or (pu_0); **_PU_AD** = applies to pin types (pu_ad); **_OD** = applies to pin types OD; **_PD_L** = applies to pin types (pd_l).

[1] Applies to output and bidirectional pins.

[2] Applies to all signals.

[3] Guaranteed but not tested.

Table 23. Reference Clocks—System Clock (SCLK) Cycle Time

Parameter	Description	SCLKRAT = 4×, 6×, 8×, 10×, 12×		SCLKRAT = 5×, 7×		Unit
		Min	Max	Min	Max	
t_{SCLK}[1, 2, 3]	System Clock Cycle Time	8	50	8	50	ns
t_{SCLKH}	System Clock Cycle High Time	$0.40 \times t_{SCLK}$	$0.60 \times t_{SCLK}$	$0.45 \times t_{SCLK}$	$0.55 \times t_{SCLK}$	ns
t_{SCLKL}	System Clock Cycle Low Time	$0.40 \times t_{SCLK}$	$0.60 \times t_{SCLK}$	$0.45 \times t_{SCLK}$	$0.55 \times t_{SCLK}$	ns
t_{SCLKF}	System Clock Transition Time—Falling Edge[4]		1.5		1.5	ns
t_{SCLKR}	System Clock Transition Time—Rising Edge		1.5		1.5	ns
t_{SCLKJ}[5, 6]	System Clock Jitter Tolerance		500		500	ps

[1] For more information, see Table 3 on Page 12.
[2] For more information, see Clock Domains on Page 9.
[3] The value of (t_{SCLK} / SCLKRAT2-0) must not violate the specification for t_{CCLK}.
[4] System clock transition times apply to minimum SCLK cycle time (t_{SCLK}) only.
[5] Actual input jitter should be combined with ac specifications for accurate timing analysis.
[6] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

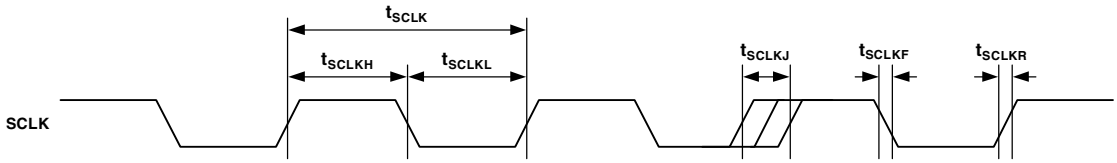

Figure 10. Reference Clocks—System Clock (SCLK) Cycle Time

Table 24. Reference Clocks—JTAG Test Clock (TCK) Cycle Time

Parameter	Description	Min	Max	Unit
t_{TCK}	Test Clock (JTAG) Cycle Time	Greater of 30 or $t_{CCLK} \times 4$		ns
t_{TCKH}	Test Clock (JTAG) Cycle High Time	12		ns
t_{TCKL}	Test Clock (JTAG) Cycle Low Time	12		ns

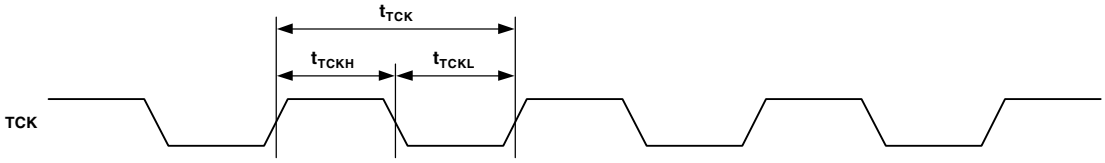

Figure 11. Reference Clocks—JTAG Test Clock (TCK) Cycle Time

Table 29. AC Signal Specifications (Continued)

(All values in this table are in nanoseconds.)

Name	Description	Input Setup (Min)	Input Hold (Min)	Output Valid (Max)	Output Hold (Min)	Output Enable (Min)[1]	Output Disable (Max)[1]	Reference Clock
DS2–0[8]	Static Pins—Must Be Constant	—	—	—	—	—	—	—
SCLKRAT2–0[8]	Static Pins—Must Be Constant	—	—	—	—	—	—	—
ENEDREG	Static Pins—Must Be Connected to V_{SS}	—	—	—	—	—	—	—
STRAP SYS[9, 10]	Strap Pins	1.5	0.5	—	—	—	—	SCLK
JTAG SYS[11, 12]	JTAG System Pins	+2.5	+10.0	+12.0	–1.0	—	—	TCK

[1] The external port protocols employ bus IDLE cycles for bus mastership transitions as well as slave address boundary crossings to avoid any potential bus contention. The apparent driver overlap, due to output disables being larger than output enables, is not actual.
[2] For input specifications on FLAG3–0 pins, see Table 21.
[3] These input pins are asynchronous and therefore do not need to be synchronized to a clock reference.
[4] For additional requirement details, see Reset and Booting on Page 9.
[5] $\overline{\text{RST\_IN}}$ clock reference is the falling edge of SCLK.
[6] TDO output clock reference is the falling edge of TCK.
[7] Reference clock depends on function.
[8] These pins may change only during reset; recommend connecting it to V_{DD_IO}/V_{SS}.
[9] STRAP pins include: $\overline{\text{BMS}}$, $\overline{\text{BM}}$, $\overline{\text{BUSLOCK}}$, TMR0E, $\overline{\text{L1BCMPO}}$, $\overline{\text{L2BCMPO}}$, and $\overline{\text{L3BCMPO}}$.
[10] Specifications applicable during reset only.
[11] JTAG system pins include: $\overline{\text{RST\_IN}}$, $\overline{\text{RST\_OUT}}$, $\overline{\text{POR\_IN}}$, $\overline{\text{IRQ3–0}}$, $\overline{\text{DMAR3–0}}$, $\overline{\text{HBR}}$, $\overline{\text{BOFF}}$, $\overline{\text{MS1–0}}$, $\overline{\text{MSH}}$, SDCKE, LDQM, HDQM, $\overline{\text{BMS}}$, $\overline{\text{IOWR}}$, $\overline{\text{IORD}}$, $\overline{\text{BM}}$, $\overline{\text{EMU}}$, SDA10, $\overline{\text{IOEN}}$, $\overline{\text{BUSLOCK}}$, TMR0E, DATA63–0, ADDR31–0, $\overline{\text{RD}}$, $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, $\overline{\text{BRST}}$, $\overline{\text{MSSD3–0}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{SDWE}}$, $\overline{\text{HBG}}$, $\overline{\text{BR7–0}}$, FLAG3–0, L0DATOP3–0, L0DATON3–0, L1DATOP3–0, L1DATON3–0, L2DATOP3–0, L2DATON3–0, L3DATOP3–0, L3DATON3–0, L0CLKOUTP, L0CLKOUTN, L1CLKOUTP, L1CLKOUTN, L2CLKOUTP, L2CLKOUTN, L3CLKOUTP, L3CLKOUTN, L0ACKI, L1ACKI, L2ACKI, L3ACKI, L0DATIP3–0, L0DATIN3–0, L1DATIP3–0, L1DATIN3–0, L2DATIP3–0, L2DATIN3–0, L3DATIP3–0, L3DATIN3–0, L0CLKINP, L0CLKINN, L1CLKINP, L1CLKINN, L2CLKINP, L2CLKINN, L3CLKINP, L3CLKINN, L0ACKO, L1ACKO, L2ACKO, L3ACKO, ACK, $\overline{\text{CPA}}$, $\overline{\text{DPA}}$, $\overline{\text{L0BCMPO}}$, $\overline{\text{L1BCMPO}}$, $\overline{\text{L2BCMPO}}$, $\overline{\text{L3BCMPO}}$, $\overline{\text{L0BCMPI}}$, $\overline{\text{L1BCMPI}}$, $\overline{\text{L2BCMPI}}$, $\overline{\text{L3BCMPI}}$, ID2–0, CTRL_IMPD1–0, SCLKRAT2–0, DS2–0, ENEDREG.
[12] JTAG system output timing clock reference is the falling edge of TCK.

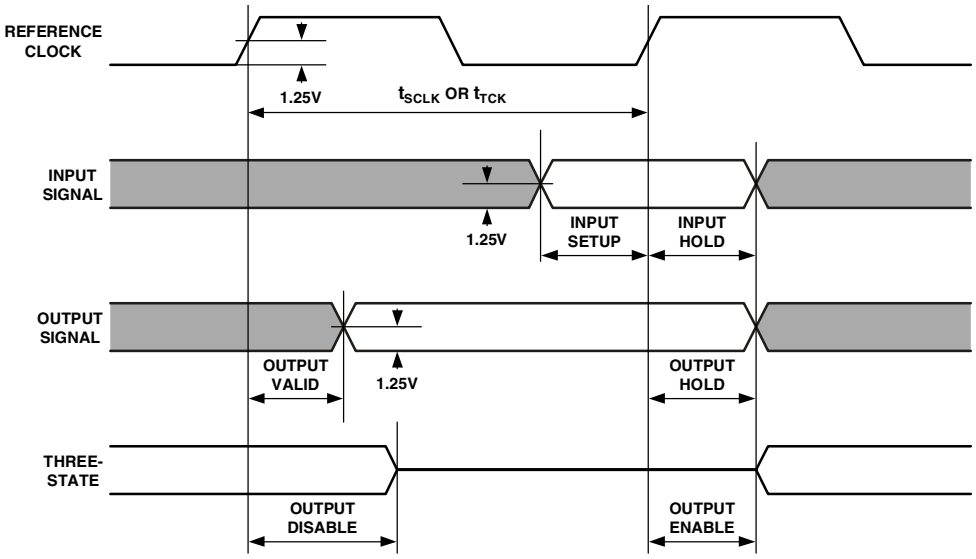

Figure 15. General AC Parameters Timing

Link Port Low Voltage, Differential-Signal (LVDS) Electrical Characteristics, and Timing

Table 30 and Table 31 with Figure 16 provide the electrical characteristics for the LVDS link ports. The LVDS link port signal definitions represent all differential signals with a V_{OD} = 0 V level and use signal naming without N (negative) and P (positive) suffixes (see Figure 16).

Table 30. Link Port LVDS Transmit Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}	Output Voltage High, V_{O_P} or V_{O_N}	R_L = 100 Ω		1.85	V
V_{OL}	Output Voltage Low, V_{O_P} or V_{O_N}	R_L = 100 Ω	0.92		V
$\|V_{OD}\|$	Output Differential Voltage	R_L = 100 Ω	300	650	mV
I_{OS}	Short-Circuit Output Current	V_{O_P} or V_{O_N} = 0 V		+5/–55	mA
		V_{OD} = 0 V		±10	mA
V_{OCM}	Common-Mode Output Voltage		1.20	1.50	V

Table 31. Link Port LVDS Receive Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
$\|V_{ID}\|$	Differential Input Voltage	$t_{LDIS}/t_{LDIH} \geq 0.20$ ns	250	850	mV
		$t_{LDIS}/t_{LDIH} \geq 0.25$ ns	217	850	mV
		$t_{LDIS}/t_{LDIH} \geq 0.30$ ns	206	850	mV
		$t_{LDIS}/t_{LDIH} \geq 0.35$ ns	195	850	mV
V_{ICM}	Common-Mode Input Voltage		0.6	1.57	V

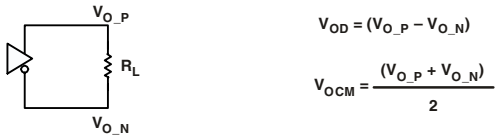

Figure 16. Link Ports—Transmit Electrical Characteristics

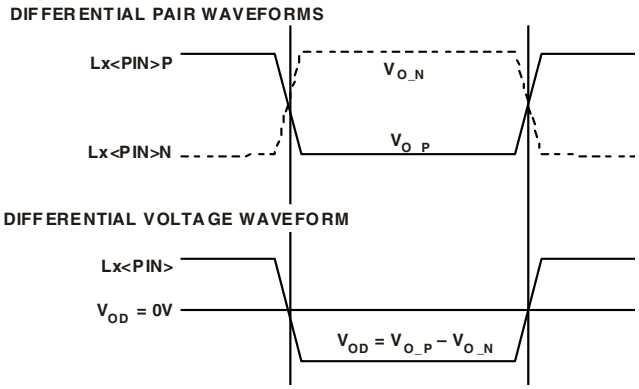

Figure 17. Link Ports—Signals Definition

Link Port—Data Out Timing

Table 32 with Figure 19, Figure 18, Figure 20, Figure 21, Figure 22, and Figure 23 provide the data out timing for the LVDS link ports.

Table 32. Link Port—Data Out Timing

Parameter	Description	Min	Max	Unit
Outputs				
t_{REO}	Rising Edge (Figure 19)		350	ps
t_{FEO}	Falling Edge (Figure 19)		350	ps
t_{LCLKOP}	LxCLKOUT Period (Figure 18)	Greater of 2.0 or $0.9 \times LCR \times t_{CCLK}$ [1, 2, 3]	Smaller of 12.5 or $1.1 \times LCR \times t_{CCLK}$ [1, 2, 3]	ns
t_{LCLKOH}	LxCLKOUT High (Figure 18)	$0.4 \times t_{LCLKOP}$ [1]	$0.6 \times t_{LCLKOP}$ [1]	ns
t_{LCLKOL}	LxCLKOUT Low (Figure 18)	$0.4 \times t_{LCLKOP}$ [1]	$0.6 \times t_{LCLKOP}$ [1]	ns
t_{COJT}	LxCLKOUT Jitter (Figure 18)		±150 [4, 5, 6]	ps
			±250 [7]	ps
t_{LDOS}	LxDATO Output Setup (Figure 20)	$0.25 \times LCR \times t_{CCLK} - 0.10 \times t_{CCLK}$ [1, 4, 8]		ns
		$0.25 \times LCR \times t_{CCLK} - 0.15 \times t_{CCLK}$ [1, 5, 6, 8]		ns
		$0.25 \times LCR \times t_{CCLK} - 0.30 \times t_{CCLK}$ [1, 7, 8]		ns
t_{LDOH}	LxDATO Output Hold (Figure 20)	$0.25 \times LCR \times t_{CCLK} - 0.10 \times t_{CCLK}$ [1, 4, 8]		ns
		$0.25 \times LCR \times t_{CCLK} - 0.15 \times t_{CCLK}$ [1, 5, 6, 8]		ns
		$0.25 \times LCR \times t_{CCLK} - 0.30 \times t_{CCLK}$ [1, 7, 8]		ns
t_{LACKID}	Delay from LxACKI Rising Edge to First Transmission Clock Edge (Figure 21)		$16 \times LCR \times t_{CCLK}$ [1, 2]	ns
t_{BCMPOV}	$\overline{\text{LxBCMPO}}$ Valid (Figure 21)		$2 \times LCR \times t_{CCLK}$ [1, 2]	ns
t_{BCMPOH}	$\overline{\text{LxBCMPO}}$ Hold (Figure 22)	$3 \times TSW - 0.5$ [1, 9]		ns
Inputs				
t_{LACKIS}	LxACKI Low Setup to Guarantee that the Transmitter Stops Transmitting (Figure 22) LxACKI High Setup to Guarantee that the Transmitter Continues its Transmission Without Any Interruption (Figure 23)	$16 \times LCR \times t_{CCLK}$ [1, 2]		ns
t_{LACKIH}	LxACKI High Hold Time (Figure 23)	0.51		ns

[1] Timing is relative to the 0 differential voltage ($V_{OD} = 0$).
[2] LCR (link port clock ratio) = 1, 1.5, 2, or 4. t_{CCLK} is the core period.
[3] For the cases of t_{LCLKOP} = 2.0 ns and t_{LCLKOP} = 12.5 ns, the effect of t_{COJT} specification on output period must be considered.
[4] LCR= 1.
[5] LCR= 1.5.
[6] LCR= 2.
[7] LCR= 4.
[8] The t_{LDOS} and t_{LDOH} values include LCLKOUT jitter.
[9] TSW is a short-word transmission period. For a 4-bit link, it is $2 \times LCR \times t_{CCLK}$. For a 1-bit link, it is $8 \times LCR \times t_{CCLK}$ ns.

OUTPUT DRIVE CURRENTS

Figure 26 through Figure 33 show typical I–V characteristics for the output drivers of the ADSP-TS202S processor. The curves in these diagrams represent the current drive capability of the output drivers as a function of output voltage over the range of drive strengths. For complete output driver characteristics, refer to the DSP's IBIS models, available on the Analog Devices website (www.analog.com).

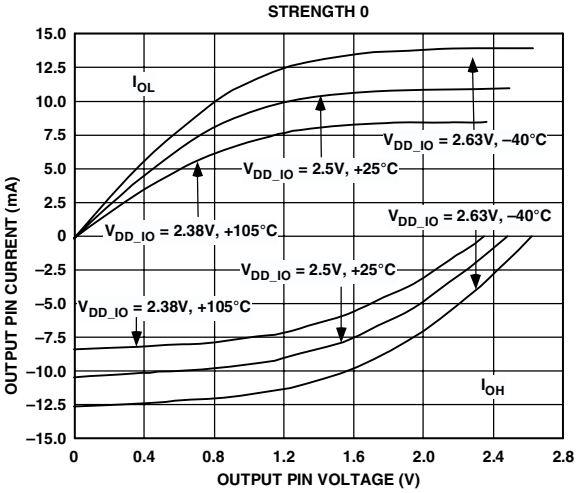

Figure 26. Typical Drive Currents at Strength 0

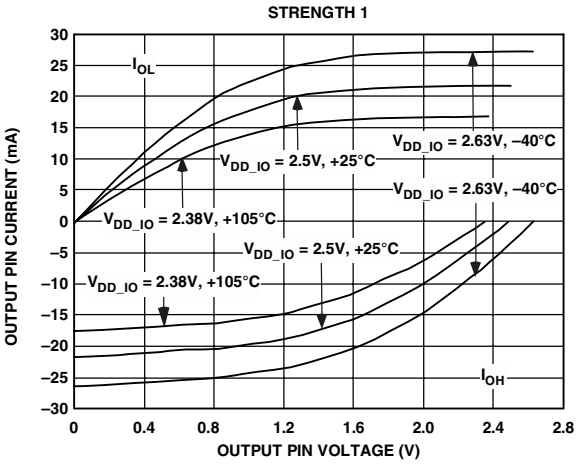

Figure 27. Typical Drive Currents at Strength 1

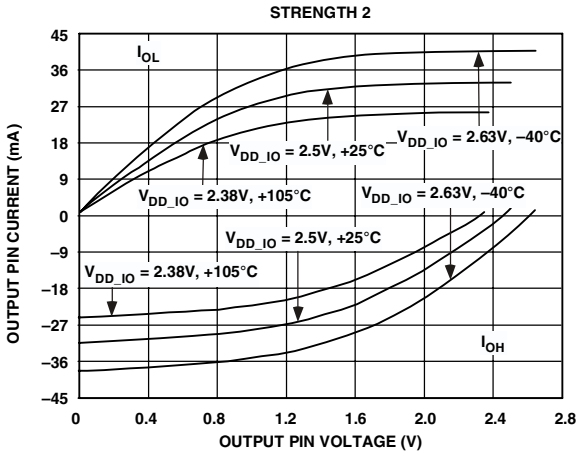

Figure 28. Typical Drive Currents at Strength 2

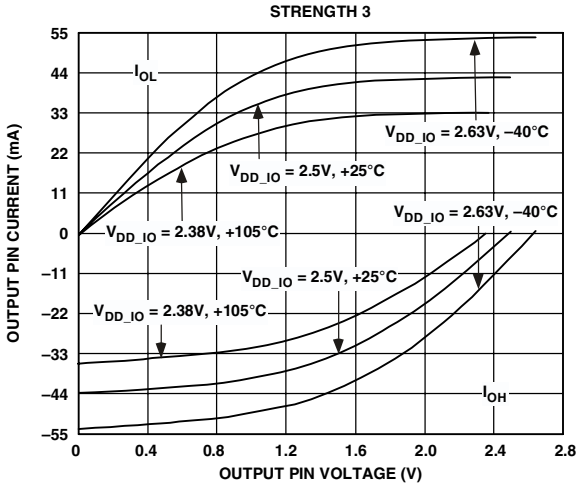

Figure 29. Typical Drive Currents at Strength 3

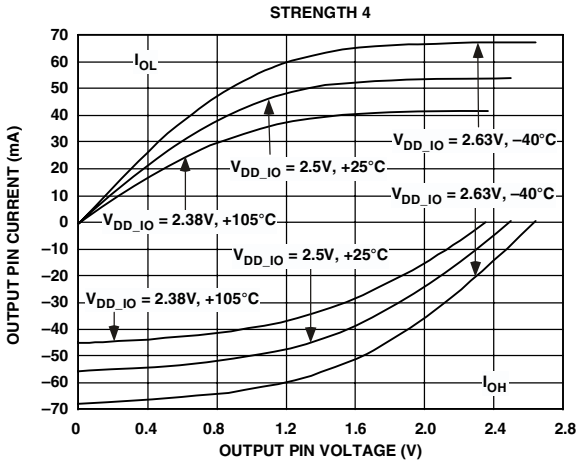

Figure 30. Typical Drive Currents at Strength 4

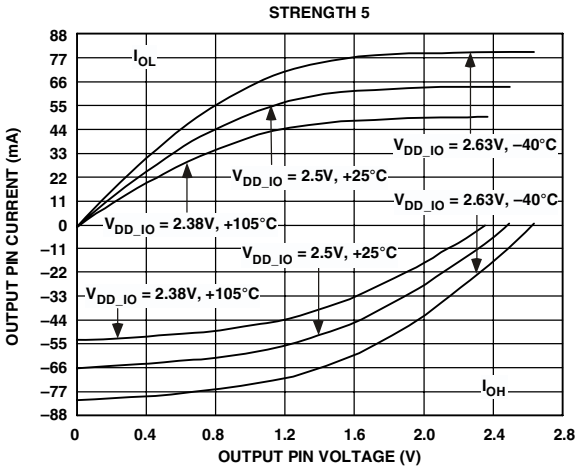

Figure 31. Typical Drive Currents at Strength 5

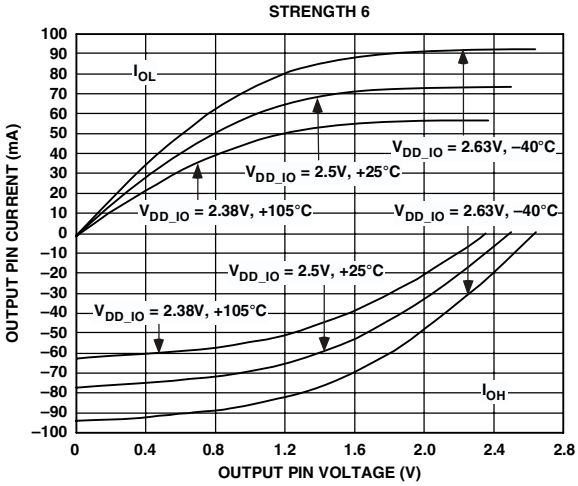

Figure 32. Typical Drive Currents at Strength 6

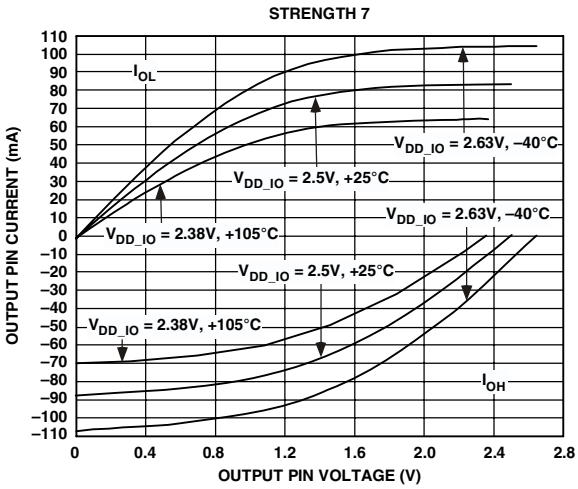

Figure 33. Typical Drive Currents at Strength 7

TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 29 on Page 28. These include output disable time, output enable time, and capacitive loading. The timing specifications for the DSP apply for the voltage reference levels in Figure 34.

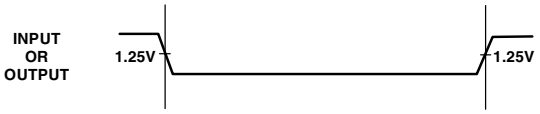

Figure 34. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L and the load current, I_L. This decay time can be approximated by the following equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The output disable time t_{DIS} is the difference between $t_{MEASURED\_DIS}$ and t_{DECAY} as shown in Figure 35. The time $t_{MEASURED\_DIS}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.4 V.

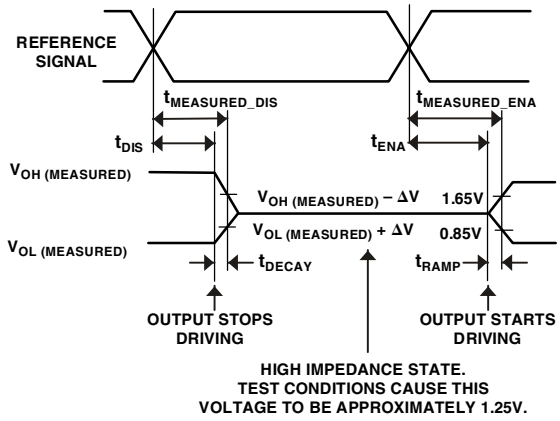

Figure 35. Output Enable/Disable

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The time for the voltage on the bus to ramp by ΔV is dependent on the capacitive load, C_L, and the drive current, I_D. This ramp time can be approximated by the following equation:

$$t_{RAMP} = (C_L \Delta V)/I_D$$

The output enable time t_{ENA} is the difference between $t_{MEASURED\_ENA}$ and t_{RAMP} as shown in Figure 35. The time $t_{MEASURED\_ENA}$ is the interval from when the reference signal switches to when the output voltage ramps ΔV from the measured three-stated output level. t_{RAMP} is calculated with test load C_L, drive current I_D, and with ΔV equal to 0.4 V.

Capacitive Loading

Output valid and hold are based on standard capacitive loads: 30 pF on all pins (see Figure 36). The delay and hold specifications given should be derated by a drive strength related factor for loads other than the nominal value of 30 pF. Figure 37 through Figure 44 show how output rise time varies with capacitance. Figure 45 graphically shows how output valid varies with load capacitance. (Note that this graph or derating does not apply to output disable delays; see Output Disable Time on Page 37.) The graphs of Figure 37 through Figure 45 may not be linear outside the ranges shown.

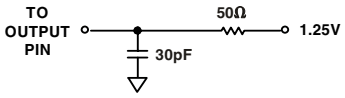

Figure 36. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

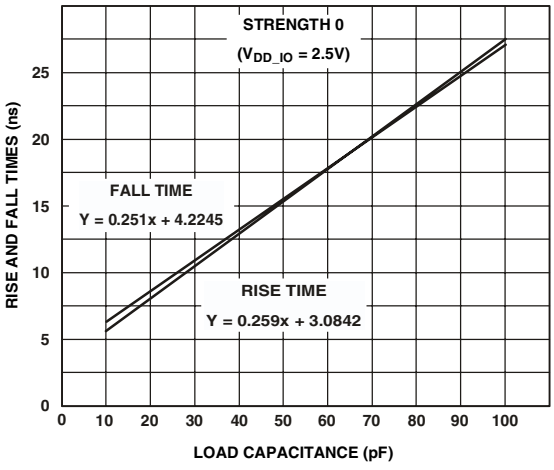

Figure 37. Typical Output Rise and Fall Time (10% to 90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 0

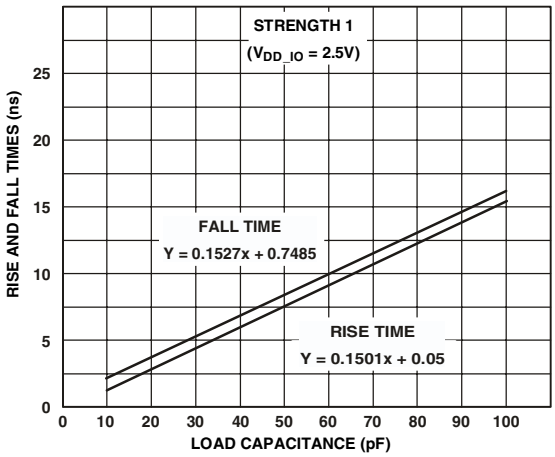

Figure 38. Typical Output Rise and Fall Time (10% to 90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 1

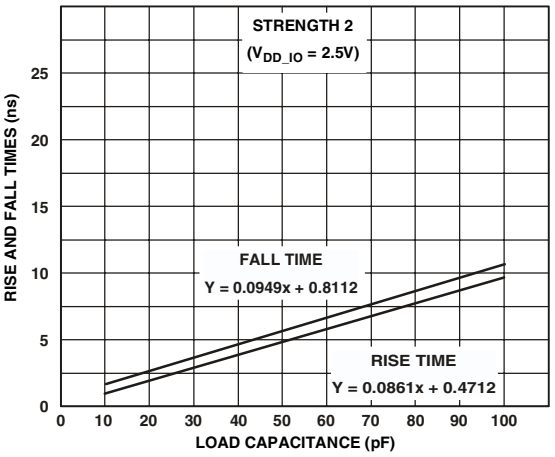

Figure 39. Typical Output Rise and Fall Time (10% to 90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 2

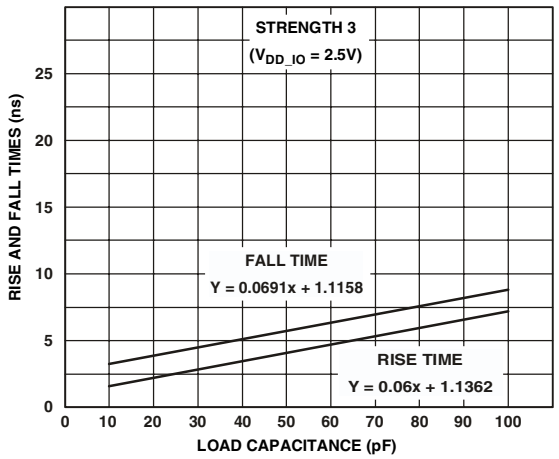

Figure 40. Typical Output Rise and Fall Time (10% to 90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 3

ENVIRONMENTAL CONDITIONS

The ADSP-TS202S processor is rated for performance under T_{CASE} environmental conditions specified in the Operating Conditions on Page 21.

Thermal Characteristics

The ADSP-TS202S processor is packaged in a 25 mm × 25 mm, thermally enhanced ball grid array (BGA_ED). The ADSP-TS202S processor is specified for a case temperature (T_{CASE}). To ensure that the T_{CASE} data sheet specification is not exceeded, a heat sink and/or an air flow source may be required.

Table 34 shows the thermal characteristics of the 25 mm × 25 mm BGA_ED package. All parameters are based on a JESD51-9 four-layer 2s2p board. All data are based on 3 W power dissipation.

Table 34. Thermal Characteristics for 25 mm × 25 mm Package

Parameter	Condition	Typical	Unit
θ_{JA}[1]	Airflow = 0 m/s	12.9[2]	°C/W
	Airflow = 1 m/s	10.2	°C/W
	Airflow = 2 m/s	9.0	°C/W
	Airflow = 3 m/s	8.0	°C/W
θ_{JB}[3]	—	7.7	°C/W
θ_{JC}[4]	—	0.7	°C/W

[1] θ_{JA} measured per JEDEC standard JESD51-6.
[2] θ_{JA} = 12.9°C/W for 0 m/s is for vertically mounted boards. For horizontally mounted boards, use 17.0°C/W for 0 m/s.
[3] θ_{JB} measured per JEDEC standard JESD51-9.
[4] θ_{JC} measured by cold plate test method (no approved JEDEC standard).

ORDERING GUIDE

Model	Temperature Range[1]	Instruction Rate[2]	On-Chip DRAM	Operating Voltage	Package Option	Package Description
ADSP-TS202SABP-050	–40°C to +85°C	500 MHz	12M bit	1.05 V_{DD}, 2.5 V_{DD_IO}, 1.5 V_{DD_DRAM}	BP-576	576-Ball BGA_ED
ADSP-TS202SABPZ050[3]	–40°C to +85°C	500 MHz	12M bit	1.05 V_{DD}, 2.5 V_{DD_IO}, 1.5 V_{DD_DRAM}	BP-576	576-Ball BGA_ED

[1] Represents case temperature.
[2] The instruction rate is the same as the internal processor core clock (CCLK) rate.
[3] Z = Pb-free part.

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