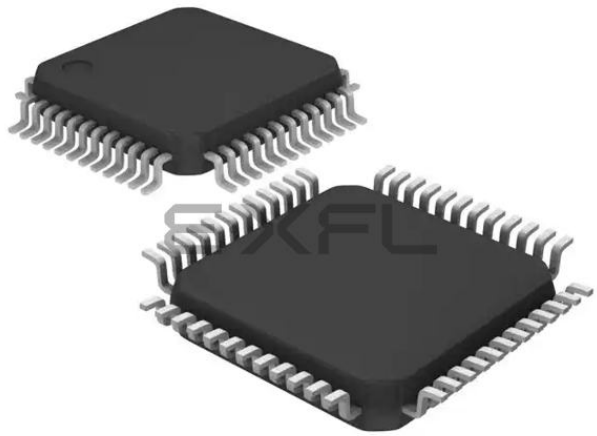


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RS08
Core Size	8-Bit
Speed	20MHz
Connectivity	SCI, SPI
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	33
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/pc9rs08la8clf

2 Pin Assignments

This section shows the pin assignments in the packages available for the MC9RS08LA8 series.

Table 1. Pin Availability by Package Pin-Count

Pin Number	<-- Lowest **Priority** --> Highest					
48	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**	**Alt 5**
1	PTD7					LCD7
2	PTD6					LCD6
3	PTD5					LCD5
4	PTD4					LCD4
5	PTD3					LCD3
6	PTD2					LCD2
7	PTD1					LCD1
8	PTD0					LCD0
9						V_{CAP1}
10						V_{CAP2}
11						V_{LL1}
12						V_{LL2}
13						V_{LL3}
14	PTA6	KBIP6	ACMP+			
15	PTA7	KBIP7	ACMP–			
16				V_{SSAD}/V_{REFL}		
17				V_{DDAD}/V_{REFH}		
18	PTB0			EXTAL		
19	PTB1			XTAL		
20				V_{DD}		
21				V_{SS}		
22	PTB2		RESET	V_{PP}		
23	PTC0		RxD			
24	PTC1		TxD			
25	PTC2		TPMCH0			
26	PTC3		TPMCH1			
27	PTC6	ACMPO	BKGD	MS		
28	PTC7		TCLK			LCD28
29	PTA0	SS	KBIP0	ADP0		LCD27
30	PTA1	SPSCK	KBIP1	ADP1		LCD26
31	PTA2	MISO	KBIP2	RxD	ADP2	LCD25

Table 1. Pin Availability by Package Pin-Count (continued)

Pin Number	<-- Lowest **Priority** --> Highest					
48	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**	**Alt 5**
32	PTA3	MOSI	KBIP3	TxD	ADP3	LCD24
33	PTA4		KBIP4	ADP4		LCD23
34	PTA5		KBIP5	ADP5		LCD22
35						LCD21
36						LCD20
37						LCD19
38						LCD18
39						LCD17
40						LCD16
41	PTE7					LCD15
42	PTE6					LCD14
43	PTE5					LCD13
44	PTE4					LCD12
45	PTE3					LCD11
46	PTE2					LCD10
47	PTE1					LCD9
48	PTE0					LCD8

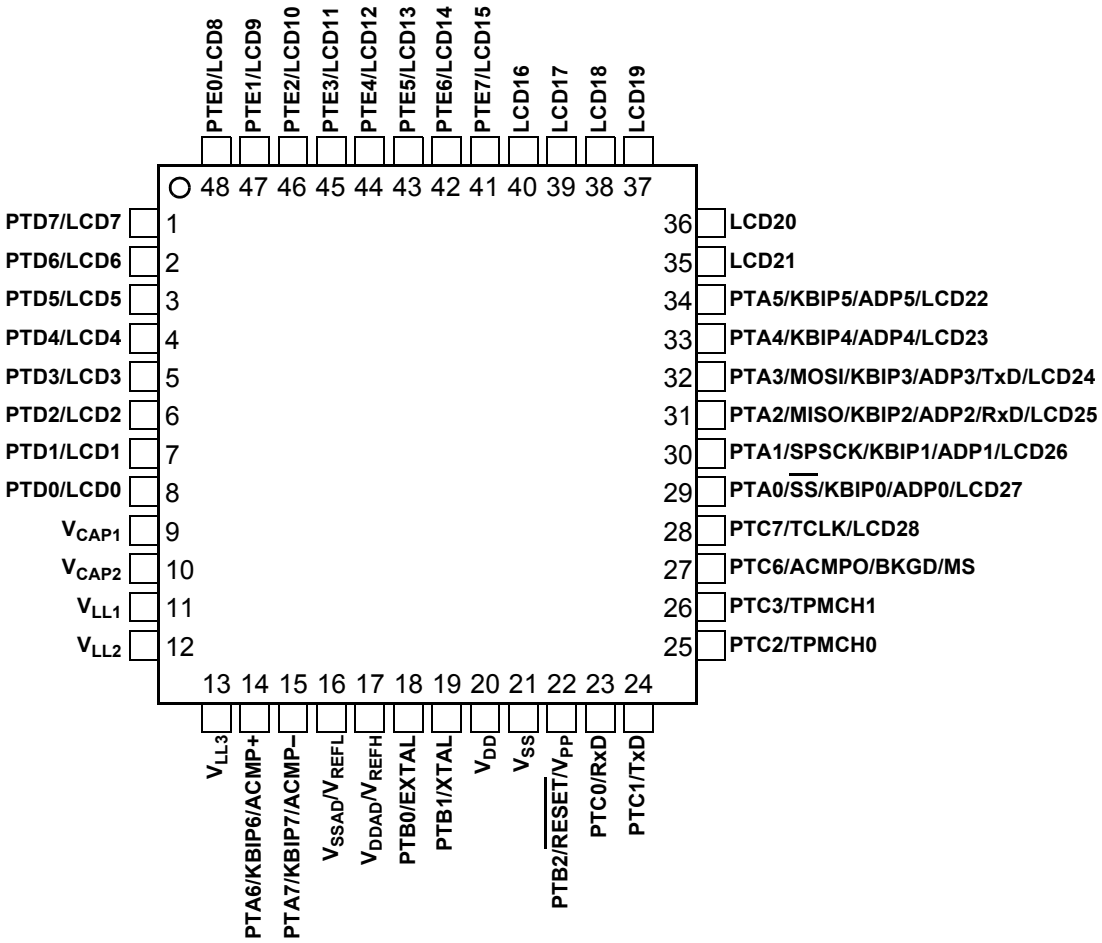


Figure 2. MC9RS08LA8 Series in 48-Pin QFN/LQFP Package

3 Electrical Characteristics

This chapter contains electrical and timing specifications.

3.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this chapter.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 3. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	2.7 to 5.5	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD} except the $\overline{\text{RESET}}/V_{PP}$ pin which is internally clamped to V_{SS} only.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

3.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 4. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H –40 to 85	°C
Maximum junction temperature	T_{JMAX}	105	°C
Thermal resistance Single layer board			
48-pin LQFP	θ_{JA}	71	°C/W
48-pin QFN		84	
Four layer board			
48-pin LQFP		49	
48-pin QFN		28	

The average chip-junction temperature (TJ) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C /W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts chip internal power

$P_{I/O}$ = Power dissipation on input and output pins user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between PD and TJ

Table 7. DC Characteristics (Temperature Range = –40 to 85°C Ambient) (continued)

Num	C	Parameter	Symbol	Min	Typical	Max	Unit
15	P	Output low voltage (port A)[4] I_{OL} = 5 mA ($V_{DD} \geq 4.5$ V) I_{OL} = 3 mA ($V_{DD} \geq 3$ V)	V_{OL}	—	—	 0.8 0.8	V
16	C	Maximum total I_{OL} for all port pins	I_{OLT}	—	—	100	mA
17	C	dc injection current[5,6,7] $V_{In} < V_{SS}$, $V_{In} > V_{DD}$ Single pin limit Total MCU limit, includes sum of all stressed pins		 — —	 — —	 0.2 0.8	 mA mA
18	C	Input capacitance (all non-supply pins)	C_{In}	—	—	7	pF

1 This parameter is characterized and not tested on each device.

2 Measurement condition for pull resistors: $V_{In} = V_{SS}$ for pullup and $V_{In} = V_{DD}$ for pulldown.

3 The I_{OH} is for high output drive strength.

4 It is tested under high output drive strength only.

5 All functional non-supply pins are internally clamped to V_{SS} and V_{DD} except the $\overline{\text{RESET}}/V_{PP}$ which is internally clamped to V_{SS} only

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 This parameter is characterized and not tested on each device.

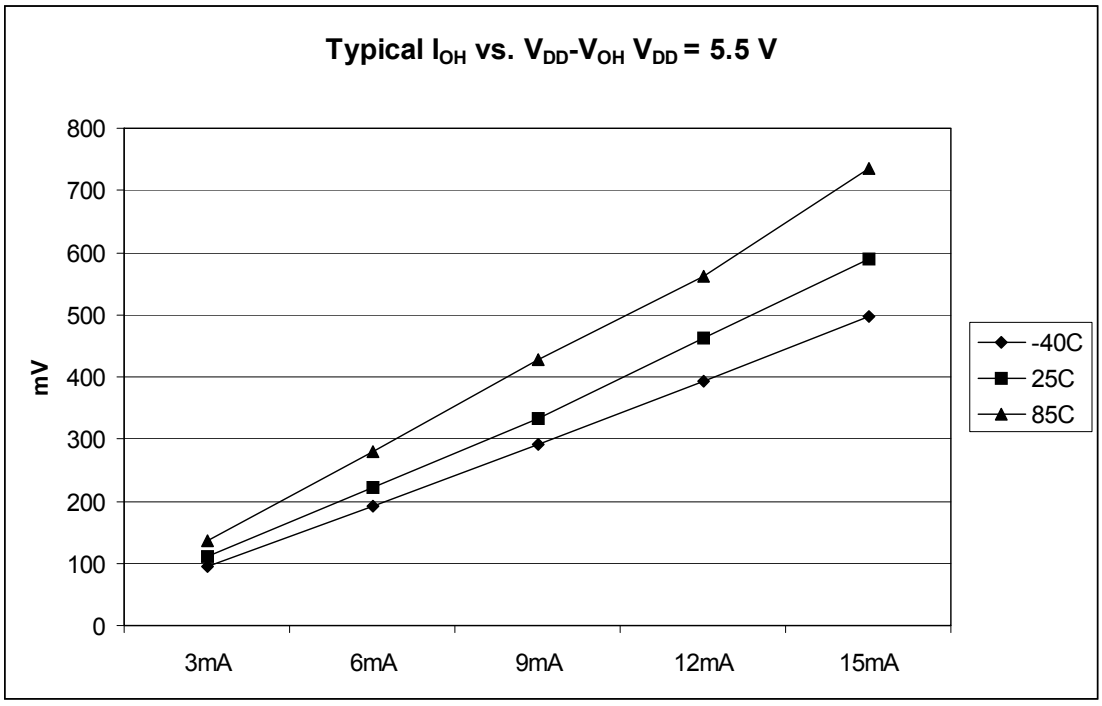


Figure 3. Typical I_{OH} vs. V_{DD}-V_{OH} (V_{DD} = 5.5 V)

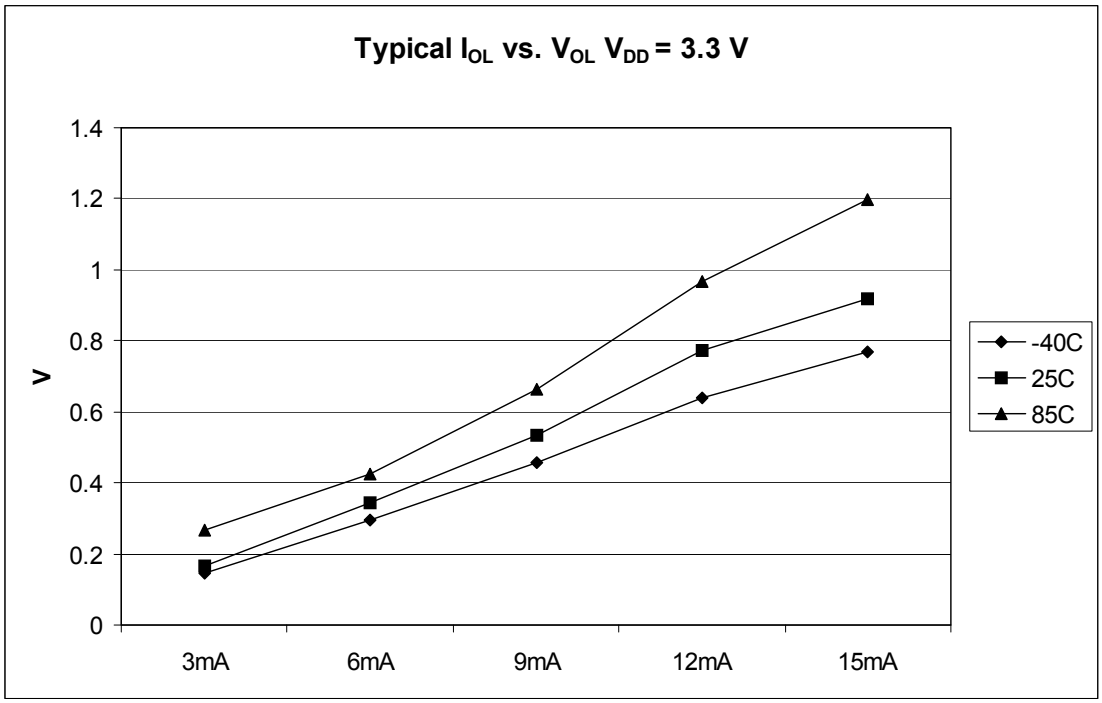


Figure 6. Typical I_{OL} vs. V_{OL} (V_{DD} = 3.3 V)

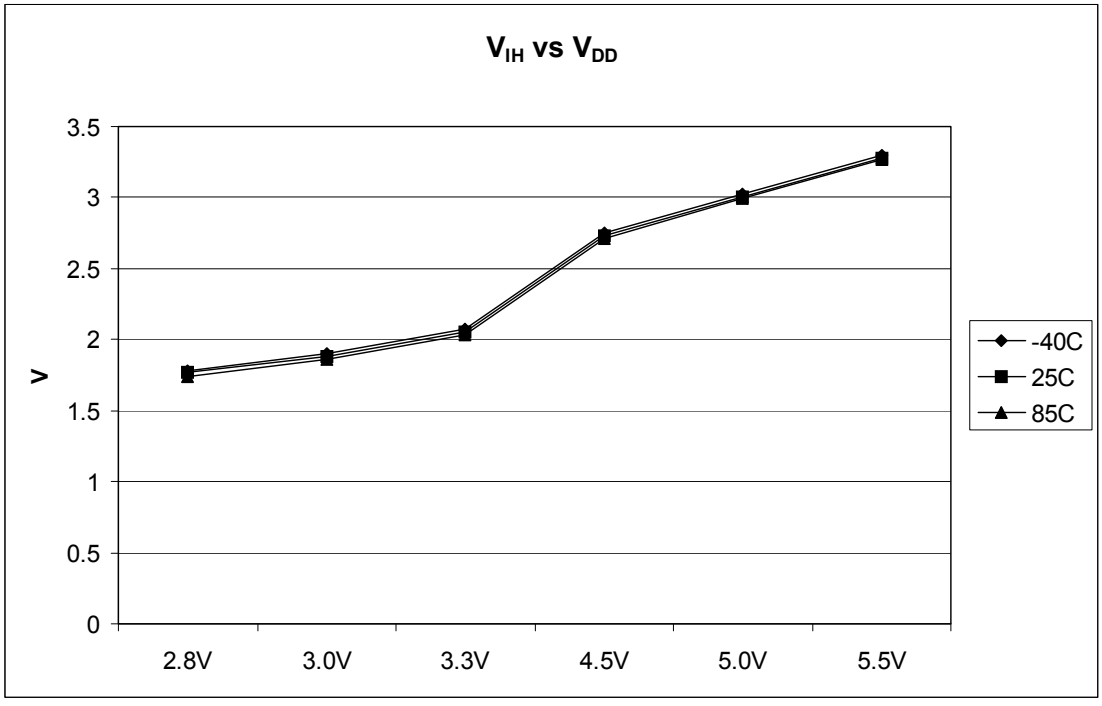


Figure 7. Typical V_{DD} vs. V_{IH}

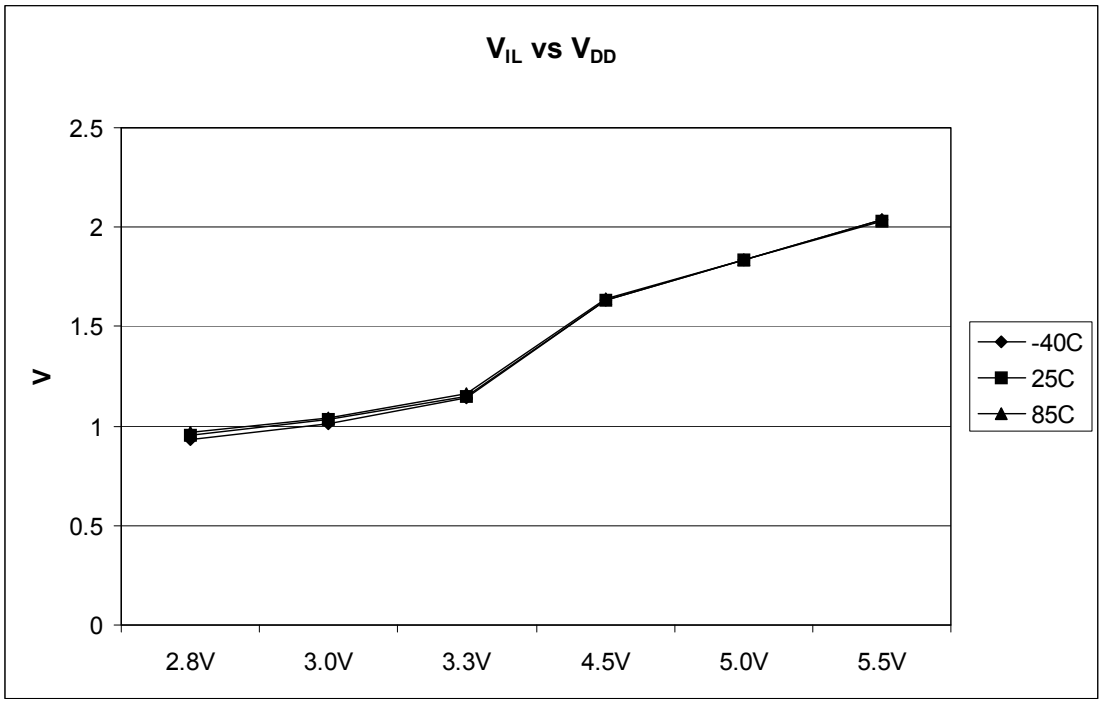


Figure 8. Typical V_{DD} vs. V_{IL}

3.6 Supply Current Characteristics

Table 8. Supply Current Characteristics

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Unit
1	P	Run supply current[2] measured at (f_{Bus} = 10 MHz)	RI_{DD10}	5	3.71	mA
				3.3	3.68	mA
				3	3.67	mA
				2.7	3.66	mA
2	P	Wait mode supply current	WI_{DD1}	5	1.37	mA
				3.3	1.37	mA
				3	1.37	mA
				2.7	1.36	mA
3	P	Stop mode supply current	SI_{DD}	5	1.40	µA
				3.3	1.35	µA
				3	1.31	µA
				2.7	1.25	µA
4	C	ADC adder from stop[3]	—	5	125.45	µA
				3.3	122.04	µA
				3	121.59	µA
				2.7	121.22	µA
5	C	ACMP adder from stop (ACME = 1)	—	5	21	µA
				3	18.5	µA

Table 9. External Oscillator Specifications (Temperature Range = –40 to 85°C Ambient)

Characteristic	Symbol	Min	Typical[1]	Max	Unit
Oscillator crystal or resonator (EREFS = 1) Low range, (IREFS = x) High range, FLL bypassed external (CLKS = 10, IREFS = x) High range, FLL engaged external (CLKS = 00, IREFS = 0)	 f_{lo} f_{hi_byp} f_{hi_eng}	 32 1 1	 — — —	 38.4 10 10	 kHz MHz MHz
Load capacitors	C_1 C_2	See Note [2]			
Feedback resistor Low range (32 kHz to 100 kHz) High range (1 MHz to 16 MHz)	R_F		 10 1		 MΩ MΩ
Series resistor Low range Low Gain (HGO = 0) High Gain (HGO = 1) High range Low Gain (HGO = 0) High Gain (HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 0 100 0 0 10 20	 — — — — — —	kΩ
Crystal start-up time [3, 4] Low range High range	t_{CSTL} t_{CSTH}	 — —	 500 4	 — —	ms
Square wave input clock frequency (EREFS = 0) FLL bypass external (CLKS = 10) FLL engaged external (CLKS = 00)	f_{extal}	 0 0.03125	 — —	 20 5	MHz
Average internal reference frequency - untrimmed	f_{int_ut}	25	31.25	41.66	kHz
Average internal reference frequency - trimmed	f_{int_t}	31.25	31.25	39.0625	kHz
DCO output frequency range - untrimmed	f_{dco_ut}	12.8	16	21.33	MHz
DCO output frequency range - trimmed	f_{dco_t}	16	16	20	MHz
Resolution of trimmed DCO output frequency at fixed voltage and temperature	$\Delta f_{dco\_res\_t}$	—	—	±0.2	$\%f_{dco}$
Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	—	±2	$\%f_{dco}$
FLL acquisition time [3,5]	$t_{acquire}$	—	—	1	ms
Long term Jitter [6] of DCO output clock (averaged over 2ms interval)	C_{Jitter}	—	—	0.6	$\%f_{dco}$

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

2 See crystal or resonator manufacturer's recommendation.

3 This parameter is characterized and not tested on each device.

4 Proper PC board layout procedures must be followed to achieve specifications.

5 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

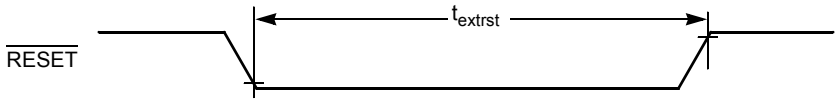


Figure 10. Reset Timing

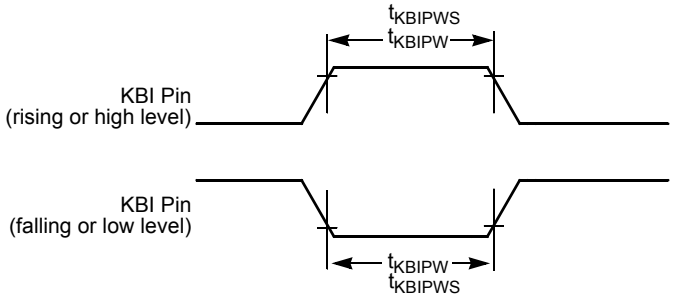


Figure 11. KBI Pulse Width

3.8.2 TPM/MTIM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 11. TPM/MTIM Input Timing

Function	Symbol	Min	Max	Unit
External clock frequency	f_{TCLK}	0	f_{Bus}1/4	MHz
External clock period	t_{TCLK}	4	—	t_{CYC}
External clock high time	t_{clkh}	1.5	—	t_{CYC}
External clock low time	t_{clkl}	1.5	—	t_{CYC}
Input capture pulse width	f_{ICPW}	1.5	—	t_{CYC}

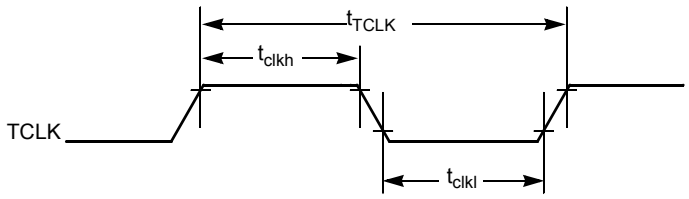


Figure 12. Timer External Clock

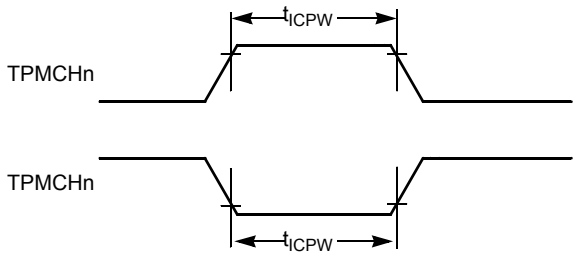


Figure 13. Timer Input Capture Pulse

3.9 Analog Comparator (ACMP) Electrical

Table 12. Analog Comparator Electrical Specifications

Characteristic	Symbol	Min	Typical	Max	Unit
Supply voltage	V_{DD}	2.7	—	5.5	V
Supply current (active)	I_{DDAC}	—	20	35	μA
Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
Analog input offset voltage[1]	V_{AIO}	—	20	40	mV
Analog Comparator hysteresis[1]	V_H	3.0	9.0	15.0	mV
Analog source impedance	R_{AS}	—	—	10	kΩ
Analog input leakage current	I_{ALKG}	—	—	1.0	μA
Analog Comparator initialization delay	t_{AINIT}	—	—	1.0	μs
Analog Comparator bandgap reference voltage	V_{BG}	1.208	1.208	1.208	V

1 These data are characterized but not production tested. Measurements are made with the device entered STOP mode.

3.10 Internal Clock Source Characteristics

Table 13. Internal Clock Source Specifications

Characteristic	Symbol	Min	Typical[1]	Max	Unit
Average internal reference frequency — untrimmed	f_{int_ut}	25	31.25	41.66	kHz
Average internal reference frequency — trimmed	f_{int_t}	31.25	39.0625[2]	39.0625	kHz
DCO output frequency range — untrimmed	f_{dco_ut}	12.8	16	21.33	MHz
DCO output frequency range — trimmed	f_{dco_t}	16	20[3]	20	MHz
Resolution of trimmed DCO output frequency at fixed voltage and temperature	$\Delta f_{dco\_res\_t}$	—	—	0.2	%f_{dco}
Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	—	2	%f_{dco}
FLL acquisition time[4,5]	$t_{acquire}$	—	—	1	ms
Stop recovery time (FLL wakeup to previous acquired frequency) IREFSTEN = 0 IREFSTEN = 1	t_{wakeup}	—	 100 86	—	μs

1 Data in typical column was characterized at 3.0 V and 5.0 V, 25 °C or is typical recommended value.

2 This value has been trimmed to 39.0625 kHz when out of factory

3 This value has been trimmed to 20 MHz when out of factory

4 This parameter is characterized and not tested on each device.

5 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBILP) to FLL enabled (FEI, FBI).

3.11 ADC Characteristics

Table 14. 5 Volt 10-bit ADC Operating Conditions

Characteristic	Conditions	Symbol	Min	Typical[1]	Max	Unit
Supply voltage	Absolute	V_{DDAD}	2.7	—	5.5	V
	Delta to V_{DD} (V_{DD} – V_{DDAD})[2]	ΔV_{DDAD}	–100	0	100	mV
Ground voltage	Delta to V_{SS} (V_{SS} – V_{SSAD})[2]	ΔV_{SSAD}	–100	0	100	mV
Ref voltage high	—	V_{REFH}	2.7	V_{DDAD}	V_{DDAD}	V
Ref voltage low	—	V_{REFL}	V_{SSAD}	V_{SSAD}	V_{SSAD}	V
Input voltage	—	V_{ADIN}	V_{REFL}	—	V_{REFH}	V
Input capacitance	—	C_{ADIN}	—	4.5	5.5	pF
Input resistance	—	R_{ADIN}	—	3	5	kΩ
Analog source resistance external to MCU	10-bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	 — —	 — —	 5 10	kΩ
	8-bit mode (all valid f_{ADCK})		—	—	10	
ADC conversion clock frequency	High speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz
	Low power (ADLPC = 1)		0.4	—	4.0	

1 Typical values assume V_{DDAD} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

Table 16. Control Timing (continued)

Characteristic	Symbol	Min	Typical	Max	Unit
External $\overline{\text{RESET}}$ pulse width[1]	t_{extrst}	150		—	ns
KBI pulse width[2]	t_{KBIPW}	1.5 t_{cyc}		—	ns
KBI pulse width in stop[1]	t_{KBIPWS}	100		—	ns
Port rise and fall time (load = 50 pF)[3] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	11 35	— —	ns

1 This is the shortest pulse that is guaranteed to pass through the pin input filter circuitry. Shorter pulses may or may not be recognized.

2 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

3 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 85 °C.

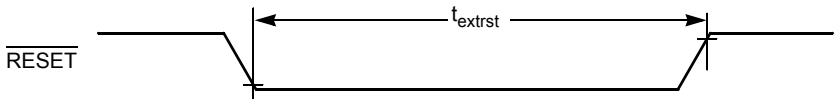


Figure 15. Reset Timing

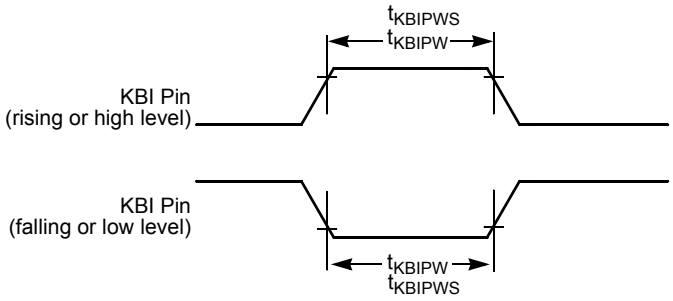


Figure 16. KBI Pulse Width

3.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory. For detailed information about program/erase operations, see the reference manual.

Table 17. Flash Characteristics

Characteristic	Symbol	Min	Typical[1]	Max	Unit
Supply voltage for program/erase	V_{DD}	2.7	—	5.5	V
Program/Erase voltage	V_{PP}	11.8	12	12.2	V
V_{PP} current Program Mass erase	 I_{VPP_prog} I_{VPP_erase}	 — —	 — —	 200 100	 µA µA
Supply voltage for read operation 0 < f_{Bus} < 10 MHz	V_{Read}	2.7	—	5.5	V

Table 17. Flash Characteristics (continued)

Characteristic	Symbol	Min	Typical[1]	Max	Unit
Byte program time	t_{prog}	20	—	40	µs
Mass erase time	t_{me}	500	—	—	ms
Cumulative program HV time[2]	t_{hv}	—	—	8	ms
Total cumulative HV time (total of t_{me} & t_{hv} applied to device)	t_{hv_total}	—	—	2	hours
HVEN to program setup time	t_{pgs}	10	—	—	µs
PGM/MASS to HVEN setup time	t_{nvs}	5	—	—	µs
HVEN hold time for PGM	t_{nvh}	5	—	—	µs
HVEN hold time for MASS	t_{nvh1}	100	—	—	µs
V_{PP} to PGM/MASS setup time	t_{vps}	20	—	—	ns
HVEN to V_{PP} hold time	t_{vph}	20	—	—	ns
V_{PP} rise time[3]	t_{vrs}	200	—	—	ns
Recovery time	t_{rcv}	1	—	—	µs
Program/erase endurance T_L to T_H = –40 °C to 85 °C	—	1000	—	—	cycles
Data retention	t_{D_ret}	15	—	—	years

1 Typicals are measured at 25 °C.

2 t_{hv} is the cumulative high voltage programming time to the same row before next erase. Same address can not be programmed more than twice before next erase.

3 Fast V_{PP} rise time may potentially trigger the ESD protection structure, which may result in over current flowing into the pad and cause permanent damage to the pad. External filtering for the V_{PP} power source is recommended. An example V_{PP} filter is shown in Figure 17.

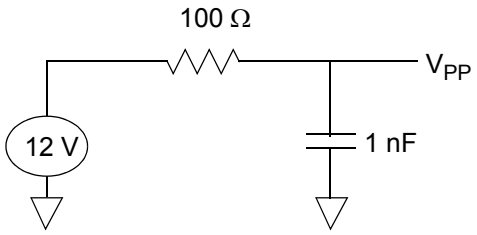
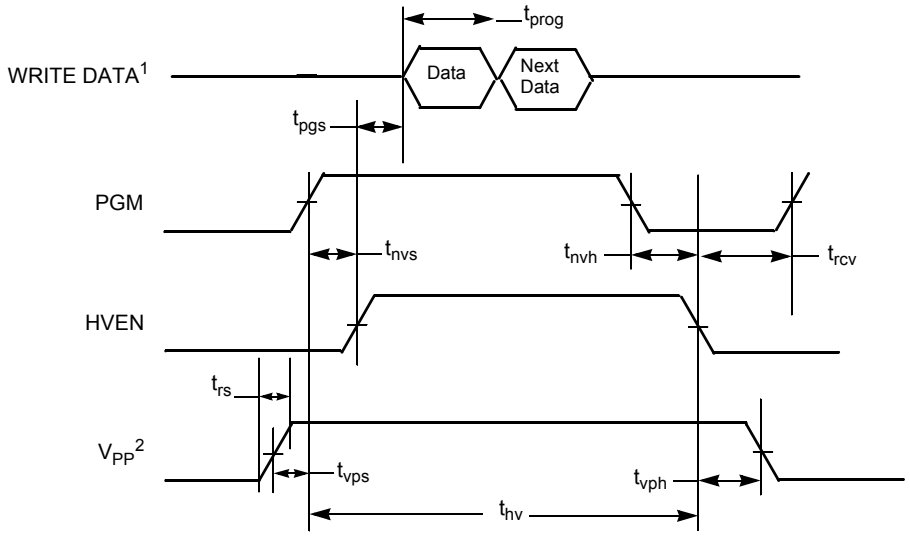


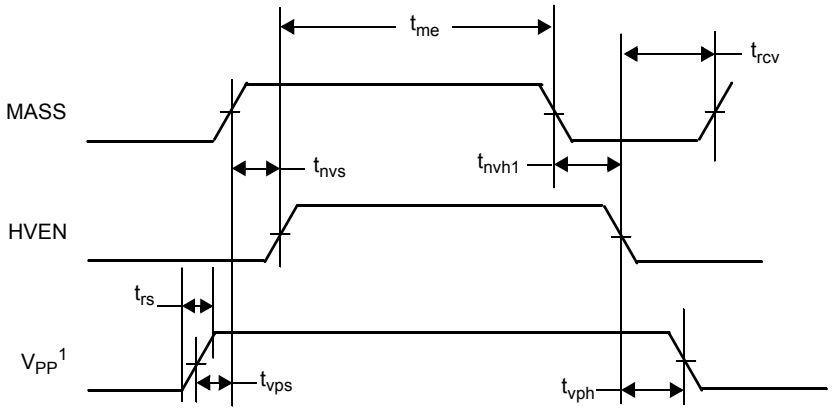
Figure 17. Example V_{PP} Filtering



1 Next Data applies if programming multiple bytes in a single row, refer to *MC9RS08LA8 Series Reference Manual*.

2 V_{DD} must be at a valid operating voltage before voltage is applied or removed from the V_{PP} pin.

Figure 18. Flash Program Timing

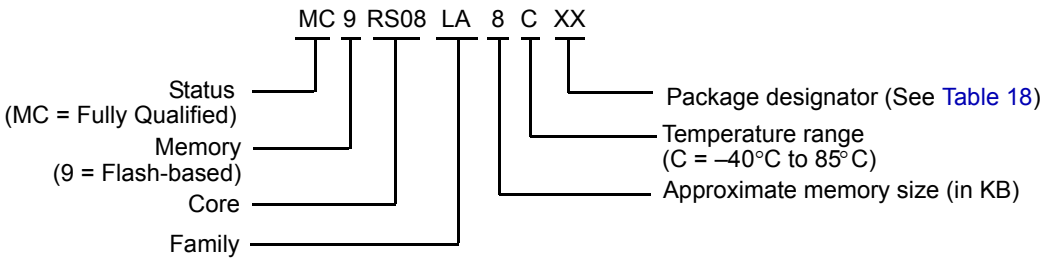


1 V_{DD} must be at a valid operating voltage before voltage is applied or removed from the V_{PP} pin.

Figure 19. Flash Mass Erase Timing

4 Ordering Information

This section contains ordering information for MC9RS08LA8 devices. See below for an example of the device numbering system.



5 Package Information and Mechanical Drawings

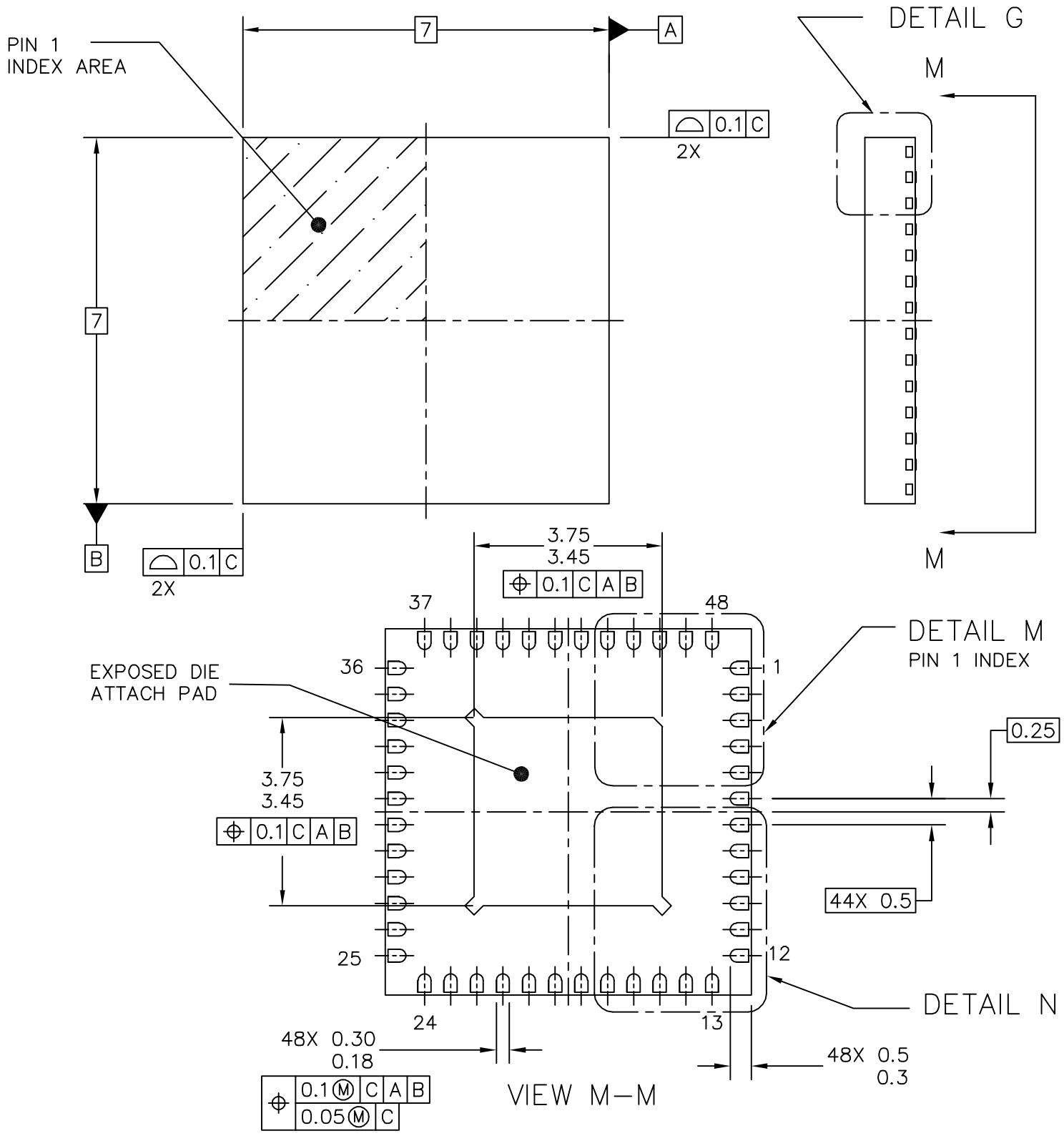
Table 18 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9RS08LA8 Series Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table 18, or
- Open a browser to the Freescale® website (http://www.freescale.com), and enter the appropriate document number (from Table 18) in the "Enter Keyword" search box at the top of the page.

Table 18. Device Numbering System

Device Number	Memory		Package		
	FLASH	RAM	Type	Designator	Document No.
MC9RS08LA8	8 KB	256 bytes	48-Pin QFN	FT	98ARL10606D
			48-Pin LQFP	LF	98ASH00962A



MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 48 TERMINAL, 0.5 PITCH (7 X 7 X 1)	DOCUMENT NO: 98ARL10606D	REV: O
	CASE NUMBER: 1975–01	29 AUG 2007
	STANDARD: JEDEC–MO–220 VKKD–2	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFN.
4. COPLANARITY APPLIES TO LEADS, CORNER LEADS, AND DIE ATTACH PAD.
5. MIN METAL GAP SHOULD BE 0.2MM.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 48 TERMINAL, 0.5 PITCH (7 X 7 X 1)	DOCUMENT NO: 98ARL10606D	REV: O
	CASE NUMBER: 1975–01	29 AUG 2007
	STANDARD: JEDEC–MO–220 VKKD–2	

NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.

2. CONTROLLING DIMENSION: MILLIMETER.

3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.

4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.

5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE AC.

6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.

7. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.350.

8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.

9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASH00962A	REV: G
LQFP, 48 LEAD, 0.50 PITCH (7.0 X 7.0 X 1.4)	CASE NUMBER: 932-03	14 APR 2005
	STANDARD: JEDEC MS-026-BBC	