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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	28
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08pt32avlc

Table 2. DC characteristics (continued)

Symbol	C	Descriptions			Min	Typical ¹	Max	Unit
I _{OHT}	D	Output high current	Max total I _{OH} for all ports	5 V	—	—	-100	mA
				3 V	—	—	-50	
V _{OL}	P	Output low voltage	All I/O pins, standard-drive strength	5 V, I _{load} = 5 mA	—	—	0.8	V
	C			3 V, I _{load} = 2.5 mA	—	—	0.8	V
	P	Output low voltage	High current drive pins, high-drive strength ²	5 V, I _{load} = 20 mA	—	—	0.8	V
	C			3 V, I _{load} = 10 mA	—	—	0.8	V
I _{OLT}	D	Output low current	Max total I _{OL} for all ports	5 V	—	—	100	mA
				3 V	—	—	50	
V _{IH}	P	Input high voltage	All digital inputs	V _{DD} > 4.5V	0.70 × V _{DD}	—	—	V
	C			V _{DD} > 2.7V	0.75 × V _{DD}	—	—	
V _{IL}	P	Input low voltage	All digital inputs	V _{DD} > 4.5V	—	—	0.30 × V _{DD}	V
	C			V _{DD} > 2.7V	—	—	0.35 × V _{DD}	
V _{hys}	C	Input hysteresis	All digital inputs	—	0.06 × V _{DD}	—	—	mV
I _{Iin}	P	Input leakage current	All input only pins (per pin)	V _{IN} = V _{DD} or V _{SS}	—	0.1	1	μA
I _{OZ}	P	Hi-Z (off-state) leakage current	All input/output (per pin)	V _{IN} = V _{DD} or V _{SS}	—	0.1	1	μA
I _{OZTOT}	C	Total leakage combined for all inputs and Hi-Z pins	All input only and I/O	V _{IN} = V _{DD} or V _{SS}	—	—	2	μA
R _{PU}	P	Pullup resistors	All digital inputs, when enabled (all I/O pins other than PTA2 and PTA3)	—	30.0	—	50.0	kΩ
R _{PU} ³	P	Pullup resistors	PTA2 and PTA3 pin	—	30.0	—	60.0	kΩ
I _{IC}	D	DC injection current ^{4, 5, 6}	Single pin limit	V _{IN} < V _{SS} , V _{IN} > V _{DD}	-0.2	—	2	mA
			Total MCU limit, includes sum of all stressed pins		-5	—	25	
C _{in}	C	Input capacitance, all pins		—	—	—	7	pF
V _{RAM}	C	RAM retention voltage		—	2.0	—	—	V

- Typical values are measured at 25 °C. Characterized, not tested.
- Only PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0, and PTH1 support ultra high current output.
- The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
- All functional non-supply pins, except for PTA2 and PTA3, are internally clamped to V_{SS} and V_{DD}.
- Input must be current-limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the large one.

6. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{IN} > V_{DD}$) is higher than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current higher than maximum injection current when the MCU is not consuming power, such as no system clock is present, or clock rate is very low (which would reduce overall power consumption).

Table 3. LVD and POR Specification

Symbol	C	Description		Min	Typ	Max	Unit
V _{POR}	D	POR re-arm voltage ^{1, 2}		1.5	1.75	2.0	V
V _{LVDH}	C	Falling low-voltage detect threshold - high range (LVDV = 1) ³		4.2	4.3	4.4	V
V _{LVW1H}	C	Falling low-voltage warning threshold - high range	Level 1 falling (LVWV = 00)	4.3	4.4	4.5	V
V _{LVW2H}	C		Level 2 falling (LVWV = 01)	4.5	4.5	4.6	V
V _{LVW3H}	C		Level 3 falling (LVWV = 10)	4.6	4.6	4.7	V
V _{LVW4H}	C		Level 4 falling (LVWV = 11)	4.7	4.7	4.8	V
V _{HYSH}	C	High range low-voltage detect/warning hysteresis		—	100	—	mV
V _{LVDL}	C	Falling low-voltage detect threshold - low range (LVDV = 0)		2.56	2.61	2.66	V
V _{LVDW1L}	C	Falling low-voltage warning threshold - low range	Level 1 falling (LVWV = 00)	2.62	2.7	2.78	V
V _{LVDW2L}	C		Level 2 falling (LVWV = 01)	2.72	2.8	2.88	V
V _{LVDW3L}	C		Level 3 falling (LVWV = 10)	2.82	2.9	2.98	V
V _{LVDW4L}	C		Level 4 falling (LVWV = 11)	2.92	3.0	3.08	V
V _{HYSDL}	C	Low range low-voltage detect hysteresis		—	40	—	mV
V _{HYSWL}	C	Low range low-voltage warning hysteresis		—	80	—	mV
V _{BG}	P	Buffered bandgap output ⁴		1.14	1.16	1.18	V

1. Maximum is highest voltage that POR is guaranteed.
2. POR ramp time must be longer than 20us/V to get a stable startup.
3. Rising thresholds are falling threshold + hysteresis.
4. Voltage factory trimmed at $V_{DD} = 5.0$ V, Temp = 25 °C

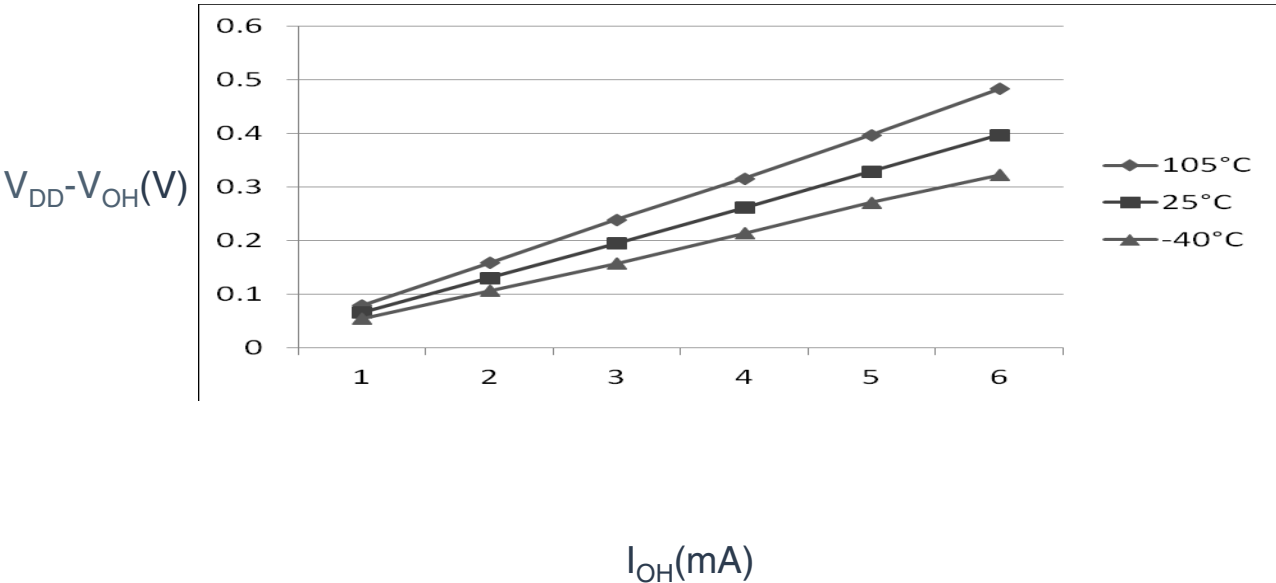


Figure 1. Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (standard drive strength) ($V_{DD} = 5\text{ V}$)

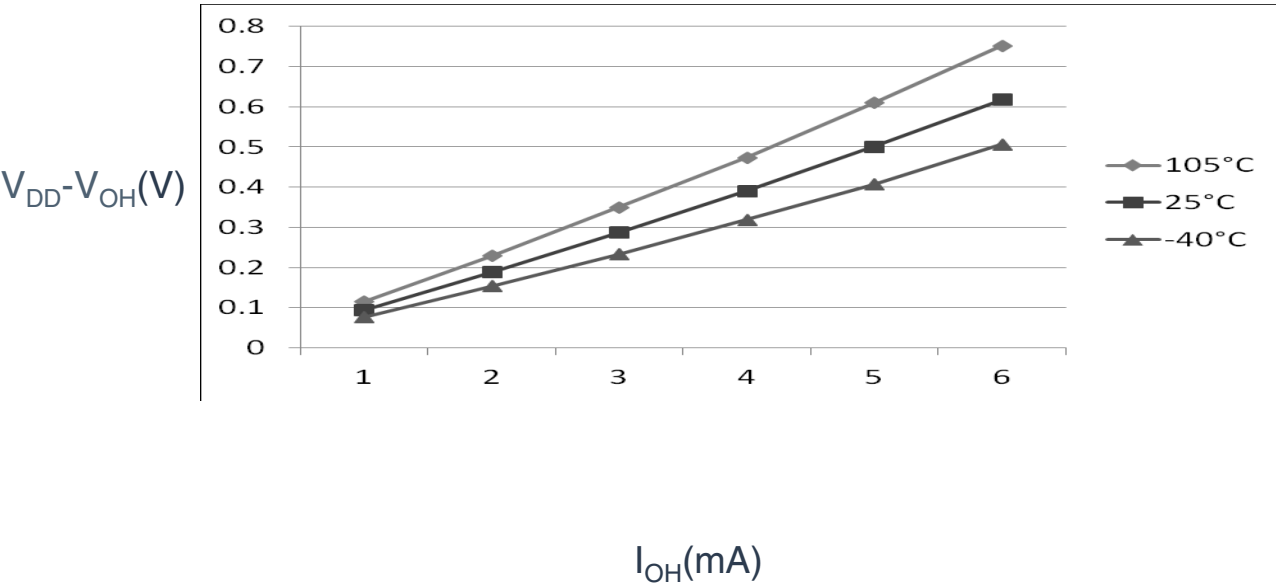


Figure 2. Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (standard drive strength) ($V_{DD} = 3\text{ V}$)

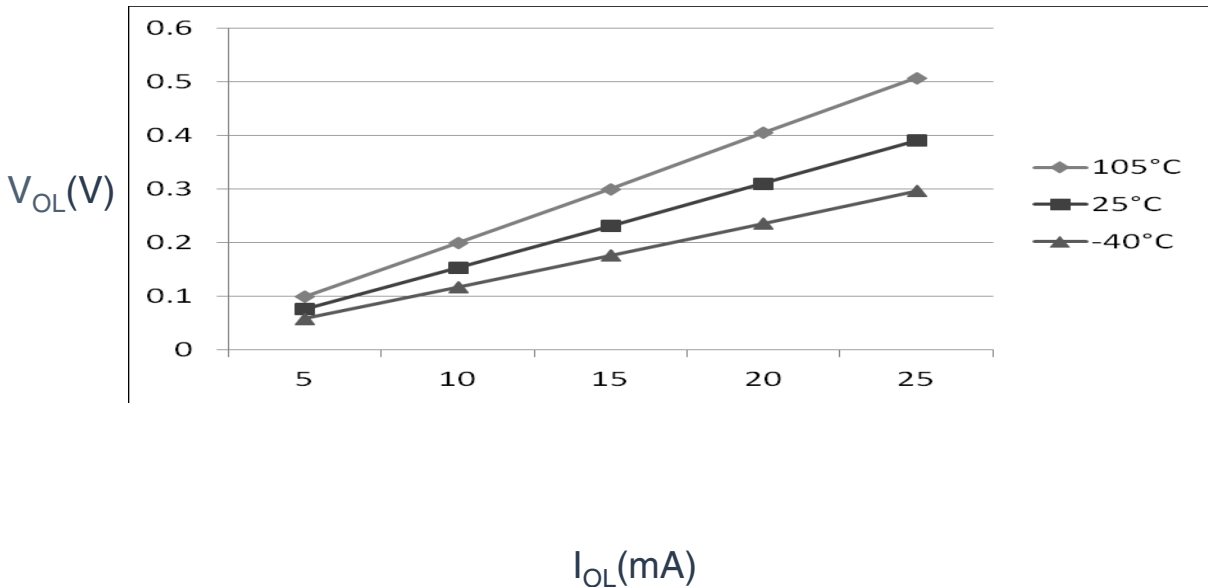


Figure 7. Typical I_{OL} Vs. V_{OL} (high drive strength) ($V_{DD} = 5\text{ V}$)

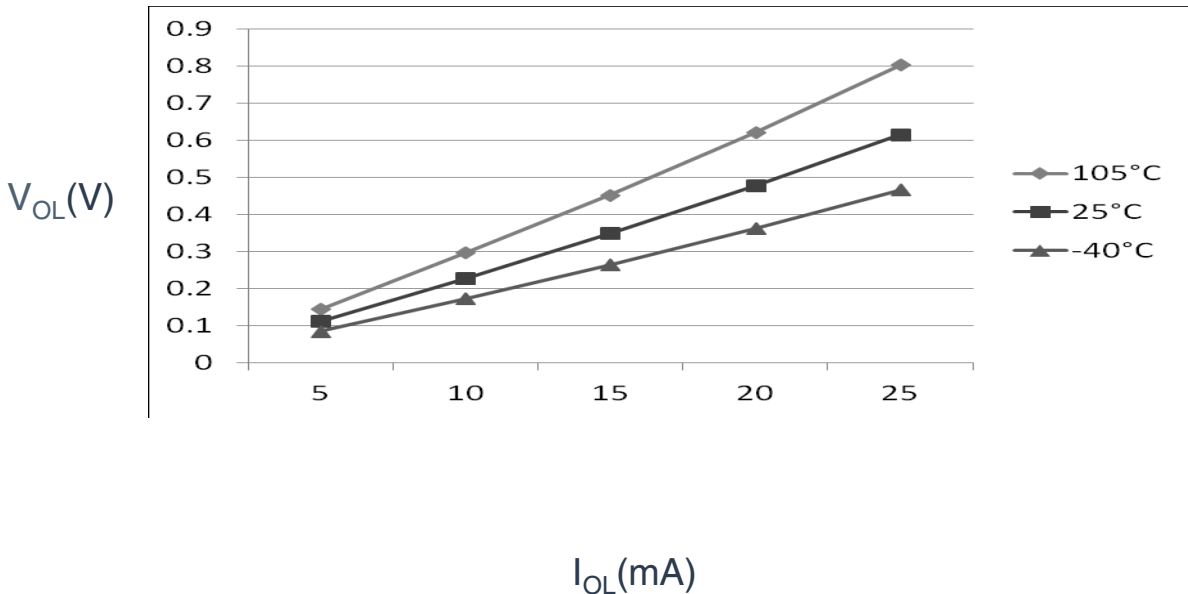


Figure 8. Typical I_{OL} Vs. V_{OL} (high drive strength) ($V_{DD} = 3\text{ V}$)

5.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 4. Supply current characteristics

Num	C	Parameter	Symbol	Bus Freq	V _{DD} (V)	Typical ¹	Max	Unit	Temp
1	C	Run supply current FEI mode, all modules on; run from flash	RI _{DD}	20 MHz	5	12.6	—	mA	-40 to 105 °C
	C			10 MHz		7.2	—		
	C			1 MHz		2.4	—		
	C			20 MHz	3	9.6	—		
	C			10 MHz		6.1	—		
	C			1 MHz		2.1	—		
2	C	Run supply current FEI mode, all modules off & gated; run from flash	RI _{DD}	20 MHz	5	10.5	—	mA	-40 to 105 °C
	C			10 MHz		6.2	—		
	C			1 MHz		2.3	—		
	C			20 MHz	3	7.4	—		
	C			10 MHz		5.0	—		
	C			1 MHz		2.0	—		
3	P	Run supply current FBE mode, all modules on; run from RAM	RI _{DD}	20 MHz	5	12.1	14.8	mA	-40 to 105 °C
	C			10 MHz		6.5	—		
	C			1 MHz		1.8	—		
	P			20 MHz	3	9.1	11.8		
	C			10 MHz		5.5	—		
	C			1 MHz		1.5	—		
4	P	Run supply current FBE mode, all modules off & gated; run from RAM	RI _{DD}	20 MHz	5	9.8	12.3	mA	-40 to 105 °C
	C			10 MHz		5.4	—		
	C			1 MHz		1.6	—		
	P			20 MHz	3	6.9	9.2		
	C			10 MHz		4.4	—		
	C			1 MHz		1.4	—		
5	C	Wait mode current FEI mode, all modules on	WI _{DD}	20 MHz	5	7.8	—	mA	-40 to 105 °C
	C			10 MHz		4.5	—		
	C			1 MHz		1.3	—		
	C			20 MHz	3	5.1	—		
	C			10 MHz		3.5	—		
	C			1 MHz		1.2	—		
6	C	Stop3 mode supply current no clocks active (except 1 kHz LPO clock) ^{2,3}	S3I _{DD}	—	5	3.8	—	μA	-40 to 105 °C
	C			—	3	3	—		-40 to 105 °C
7	C	ADC adder to stop3	—	—	5	44	—	μA	-40 to 105 °C

Table continues on the next page...

Table 4. Supply current characteristics (continued)

Num	C	Parameter	Symbol	Bus Freq	V _{DD} (V)	Typical ¹	Max	Unit	Temp
	C	ADLPC = 1 ADLSMP = 1 ADCO = 1 MODE = 10B ADICLK = 11B			3	40	—		
8	C	TSI adder to stop3 ⁴	—	—	5	111	—	μA	-40 to 105 °C
	C	PS = 010B NSCN = 0x0F EXTCHRG = 0 REFCHRG = 0 DVOLT = 01B			3	110	—		
9	C	LVD adder to stop3 ⁵	—	—	5	130	—	μA	-40 to 105 °C
	C				3	125	—		

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. RTC adder cause <1 μA I_{DD} increase typically, RTC clock source is 1 kHz LPO clock.
3. ACMP adder cause <10 μA I_{DD} increase typically.
4. The current varies with TSI configuration and capacity of touch electrode. Please refer to [TSI electrical specifications](#).
5. LVD is periodically woken up from stop3 by 5% duty cycle. The period is equal to or less than 2 ms.

5.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as [AN2321](#), [AN1050](#), [AN1263](#), [AN2764](#), and [AN1259](#) for advice and guidance specifically targeted at optimizing EMC performance.

5.1.3.1 EMC radiated emissions operating behaviors

Table 5. EMC radiated emissions operating behaviors for 64-pin SOIC package

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V _{RE1}	Radiated emissions voltage, band 1	0.15–50	12	dBμV	1, 2
V _{RE2}	Radiated emissions voltage, band 2	50–150	10	dBμV	
V _{RE3}	Radiated emissions voltage, band 3	150–500	4	dBμV	
V _{RE4}	Radiated emissions voltage, band 4	500–1000	5	dBμV	
V _{RE_IEC}	IEC level	0.15–1000	N	—	2, 3

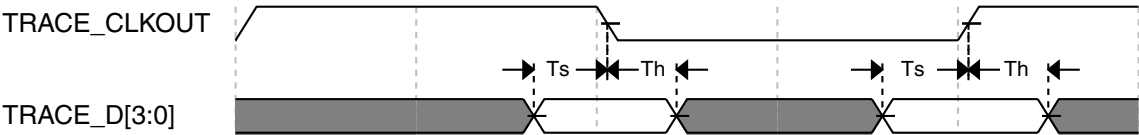


Figure 12. Trace data specifications

5.2.3 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 8. FTM input timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

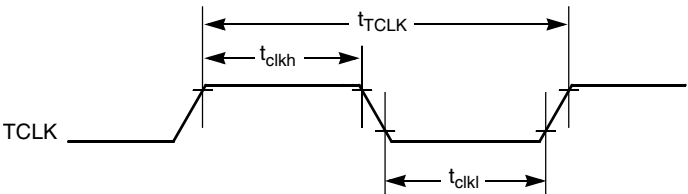


Figure 13. Timer external clock

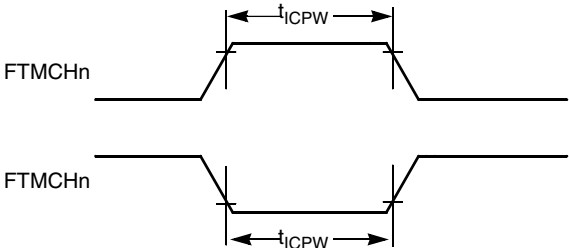


Figure 14. Timer input capture pulse

5.3 Thermal specifications

5.3.1 Thermal operating requirements

Table 9. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	−40	125	°C
T_A	Ambient temperature	−40	105	°C

NOTE

Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times \text{chip power dissipation}$.

5.3.2 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 10. Thermal attributes

Board type	Symbol	Description	64 LQFP	64 QFP	48 LQFP	44 LQFP	32 LQFP	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	71	61	81	75	86	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	53	47	57	53	57	°C/W	1, 3
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	59	50	68	62	72	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	46	41	50	47	51	°C/W	1, 3

Table continues on the next page...

Table 10. Thermal attributes (continued)

Board type	Symbol	Description	64 LQFP	64 QFP	48 LQFP	44 LQFP	32 LQFP	Unit	Notes
—	$R_{\theta JB}$	Thermal resistance, junction to board	35	32	34	34	33	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	20	23	24	20	24	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	5	8	6	5	6	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization.

6 Peripheral operating requirements and behaviors

6.1 External oscillator (XOSC) and ICS characteristics

Table 11. XOSC and ICS specifications (temperature range = -40 to 105 °C ambient)

Num	C	Characteristic		Symbol	Min	Typical ¹	Max	Unit
1	C	Oscillator crystal or resonator	Low range (RANGE = 0)	f_{lo}	31.25	32.768	39.0625	kHz
	C		High range (RANGE = 1) FEE or FBE mode ²	f_{hi}	4	—	20	MHz
	C		High range (RANGE = 1), high gain (HGO = 1), FBELP mode	f_{hi}	4	—	20	MHz
	C		High range (RANGE = 1), low power (HGO = 0), FBELP mode	f_{hi}	4	—	20	MHz
2	D	Load capacitors		C1, C2	See Note ³			
3	D	Feedback resistor	Low Frequency, Low-Power Mode ⁴	R_F	—	—	—	MΩ
			Low Frequency, High-Gain Mode		—	10	—	MΩ
			High Frequency, Low-Power Mode		—	1	—	MΩ

Table continues on the next page...

**Table 11. XOSC and ICS specifications (temperature range = -40 to 105 °C ambient)
(continued)**

Num	C	Characteristic		Symbol	Min	Typical ¹	Max	Unit
			High Frequency, High-Gain Mode		—	1	—	MΩ
4	D	Series resistor - Low Frequency	Low-Power Mode ⁴	R _S	—	—	—	kΩ
			High-Gain Mode		—	200	—	kΩ
5	D	Series resistor - High Frequency	Low-Power Mode ⁴	R _S	—	—	—	kΩ
	D	Series resistor - High Frequency, High-Gain Mode	4 MHz		—	0	—	kΩ
	D		8 MHz		—	0	—	kΩ
	D		16 MHz		—	0	—	kΩ
6	C	Crystal start-up time Low range = 32.768 kHz crystal; High range = 20 MHz crystal ^{5, 6}	Low range, low power	t _{CSTL}	—	1000	—	ms
	C		Low range, high power	t _{CSTH}	—	800	—	ms
	C		High range, low power		—	3	—	ms
	C		High range, high power		—	1.5	—	ms
7	T	Internal reference start-up time		t _{IRST}	—	20	50	μs
8	D	Square wave input clock frequency	FEE or FBE mode ²	f _{extal}	0.03125	—	5	MHz
	D		FBELP mode		0	—	20	MHz
9	P	Average internal reference frequency - trimmed		f _{int_t}	—	32.768	—	kHz
10	P	DCO output frequency range - trimmed		f _{dco_t}	16	—	20	MHz
11	P	Total deviation of DCO output from trimmed frequency ⁵	Over full voltage and temperature range	Δf _{dco_t}	—	—	±2.0	%f _{dco}
	C		Over fixed voltage and temperature range of 0 to 70 °C				±1.0	
12	C	FLL acquisition time ^{5, 7}		t _{Acquire}	—	—	2	ms
13	C	Long term jitter of DCO output clock (averaged over 2 ms interval) ⁸		C _{Jitter}	—	0.02	0.2	%f _{dco}

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. When ICS is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.
3. See crystal or resonator manufacturer's recommendation.
4. Load capacitors (C₁, C₂), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.
5. This parameter is characterized and not tested on each device.
6. Proper PC board layout procedures must be followed to achieve specifications.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

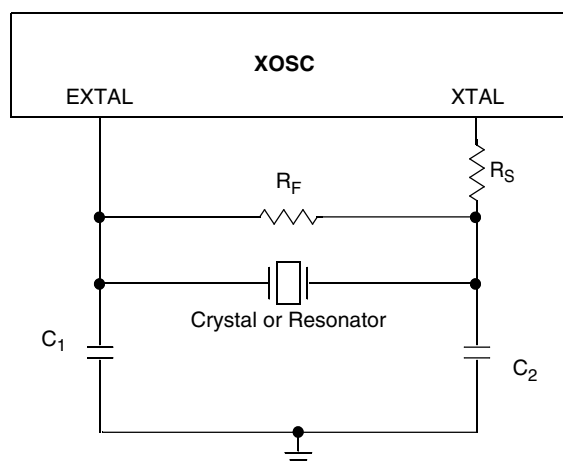


Figure 15. Typical crystal or resonator circuit

6.2 NVM specifications

This section provides details about program/erase times and program/erase endurance for the flash and EEPROM memories.

Table 12. Flash characteristics

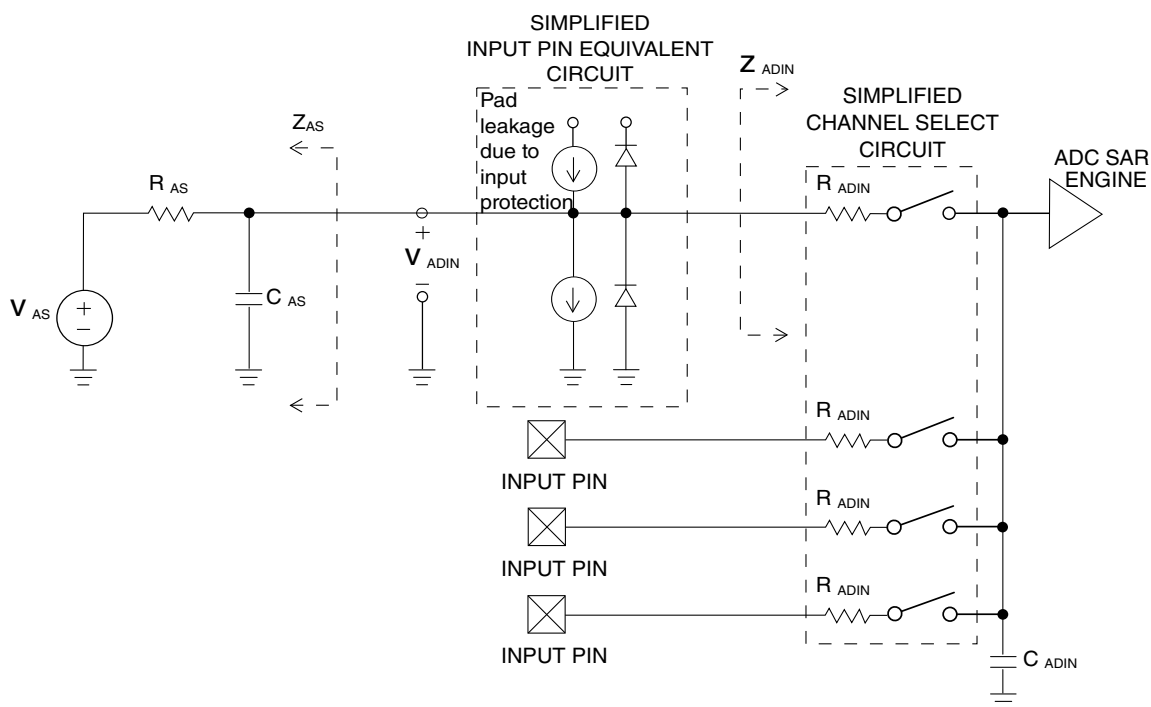
C	Characteristic	Symbol	Min ¹	Typical ²	Max ³	Unit ⁴
D	Supply voltage for program/erase -40 °C to 105 °C	$V_{\text{prog/erase}}$	2.7	—	5.5	V
D	Supply voltage for read operation	V_{Read}	2.7	—	5.5	V
D	NVM Bus frequency	f_{NVMBUS}	1	—	25	MHz
D	NVM Operating frequency	f_{NVMOP}	0.8	1	1.05	MHz
D	Erase Verify All Blocks	t_{VFYALL}	—	—	17338	t_{cyc}
D	Erase Verify Flash Block	t_{RD1BLK}	—	—	16913	t_{cyc}
D	Erase Verify EEPROM Block	t_{RD1BLK}	—	—	810	t_{cyc}
D	Erase Verify Flash Section	t_{RD1SEC}	—	—	484	t_{cyc}
D	Erase Verify EEPROM Section	t_{DRD1SEC}	—	—	555	t_{cyc}
D	Read Once	t_{RDONCE}	—	—	450	t_{cyc}
D	Program Flash (2 word)	t_{PGM2}	0.12	0.12	0.29	ms
D	Program Flash (4 word)	t_{PGM4}	0.20	0.21	0.46	ms
D	Program Once	t_{PGMONCE}	0.20	0.21	0.21	ms
D	Program EEPROM (1 Byte)	t_{DPGM1}	0.10	0.10	0.27	ms
D	Program EEPROM (2 Byte)	t_{DPGM2}	0.17	0.18	0.43	ms
D	Program EEPROM (3 Byte)	t_{DPGM3}	0.25	0.26	0.60	ms
D	Program EEPROM (4 Byte)	t_{DPGM4}	0.32	0.33	0.77	ms
D	Erase All Blocks	t_{ERSALL}	96.01	100.78	101.49	ms
D	Erase Flash Block	t_{ERSBLK}	95.98	100.75	101.44	ms

Table continues on the next page...

Table 13. 5 V 12-bit ADC operating conditions (continued)

Characteristic	Conditions	Symb	Min	Typ ¹	Max	Unit	Comment
	10-bit mode		—	—	5		
	• $f_{ADCK} > 4$ MHz		—	—	10		
	• $f_{ADCK} < 4$ MHz		—	—	10		
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC conversion clock frequency	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	—
	Low power (ADLPC=1)		0.4	—	4.0		

- Typical values assume $V_{DDA} = 5.0$ V, Temp = 25°C, $f_{ADCK}=1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- DC potential difference.


Figure 16. ADC input impedance equivalency diagram
Table 14. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Characteristic	Conditions	C	Symb	Min	Typ ¹	Max	Unit
Supply current		T	I_{DDA}	—	133	—	μ A
ADLPC = 1							
ADLSMP = 1							
ADCO = 1							
Supply current		T	I_{DDA}	—	218	—	μ A

Table continues on the next page...

Table 14. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Characteristic	Conditions	C	Symb	Min	Typ ¹	Max	Unit
ADLPC = 1 ADLSMP = 0 ADCO = 1							
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	327	—	μA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	I_{DDAD}	—	582	990	μA
Supply current	Stop, reset, module off	T	I_{DDA}	—	0.011	1	μA
ADC asynchronous clock source	High speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz
	Low power (ADLPC = 1)			1.25	2	3.3	
Conversion time (including sample time)	Short sample (ADLSMP = 0)	T	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	40	—	
Sample time	Short sample (ADLSMP = 0)	T	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted Error ²	12-bit mode	T	E_{TUE}	—	± 5.0	—	LSB ³
	10-bit mode	P		—	± 1.5	± 2.0	
	8-bit mode	P		—	± 0.7	± 1.0	
Differential Non-Linearity	12-bit mode	T	DNL	—	± 1.0	—	LSB ³
	10-bit mode ⁴	P		—	± 0.25	± 0.5	
	8-bit mode ⁴	P		—	± 0.15	± 0.25	
Integral Non-Linearity	12-bit mode	T	INL	—	± 1.0	—	LSB ³
	10-bit mode	T		—	± 0.3	± 0.5	
	8-bit mode	T		—	± 0.15	± 0.25	
Zero-scale error ⁵	12-bit mode	C	E_{ZS}	—	± 2.0	—	LSB ³
	10-bit mode	P		—	± 0.25	± 1.0	
	8-bit mode	P		—	± 0.65	± 1.0	
Full-scale error ⁶	12-bit mode	T	E_{FS}	—	± 2.5	—	LSB ³
	10-bit mode	T		—	± 0.5	± 1.0	
	8-bit mode	T		—	± 0.5	± 1.0	
Quantization error	≤ 12 bit modes	D	E_Q	—	—	± 0.5	LSB ³

Table continues on the next page...

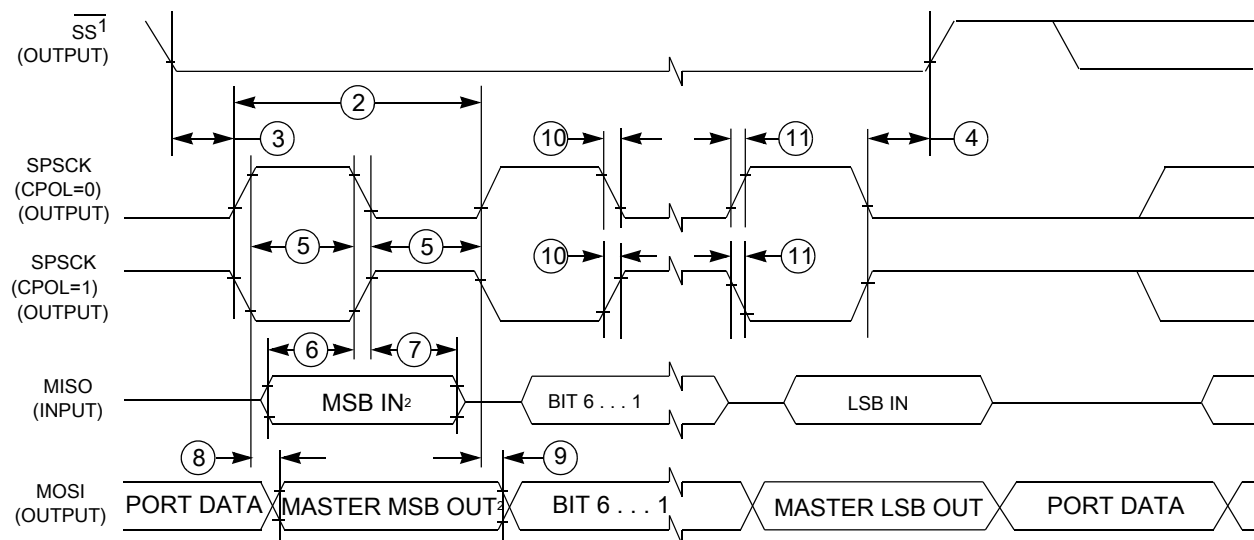


Figure 18. SPI master mode timing (CPHA=1)

Table 17. SPI slave mode timing

Nu m.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	0	$f_{Bus}/4$	Hz	f_{Bus} is the bus clock as defined in .
2	t_{SPSCCK}	SPSCCK period	$4 \times t_{Bus}$	—	ns	$t_{Bus} = 1/f_{Bus}$
3	t_{Lead}	Enable lead time	1	—	t_{Bus}	—
4	t_{Lag}	Enable lag time	1	—	t_{Bus}	—
5	$t_{WSPSCCK}$	Clock (SPSCCK) high or low time	$t_{Bus} - 30$	—	ns	—
6	t_{SU}	Data setup time (inputs)	15	—	ns	—
7	t_{HI}	Data hold time (inputs)	25	—	ns	—
8	t_a	Slave access time	—	t_{Bus}	ns	Time to data active from high-impedance state
9	t_{dis}	Slave MISO disable time	—	t_{Bus}	ns	Hold time to high-impedance state
10	t_v	Data valid (after SPSCCK edge)	—	25	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	$t_{Bus} - 25$	ns	—
	t_{FI}	Fall time input	—	$t_{Bus} - 25$	ns	—
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output	—	25	ns	—

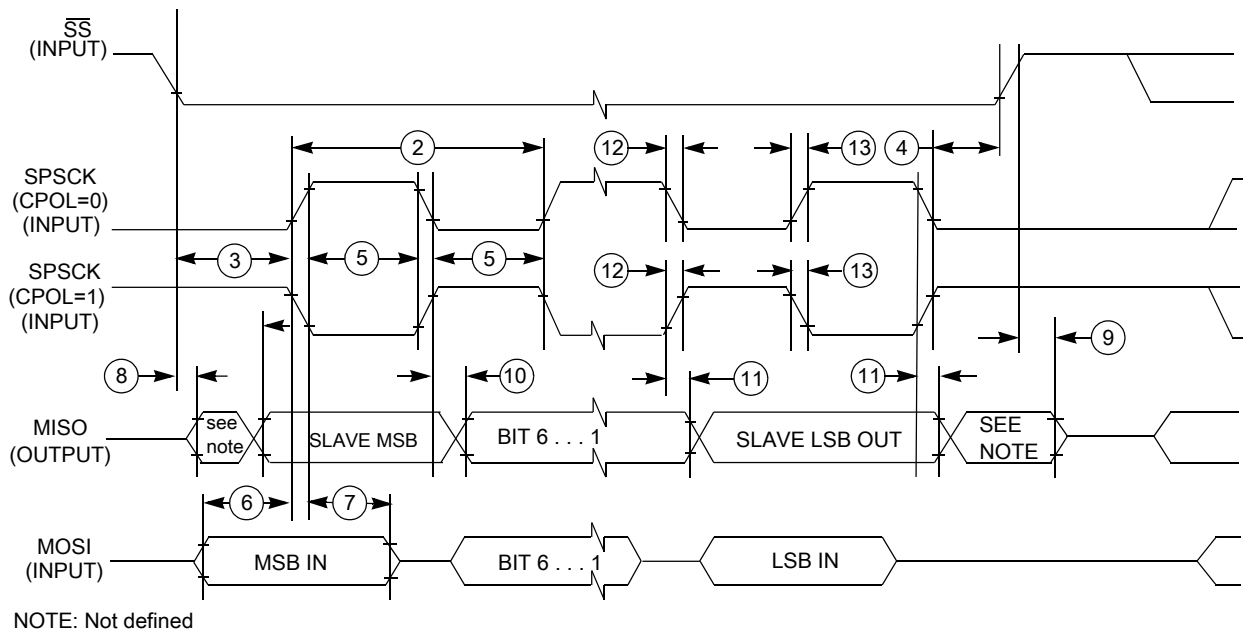


Figure 19. SPI slave mode timing (CPHA = 0)

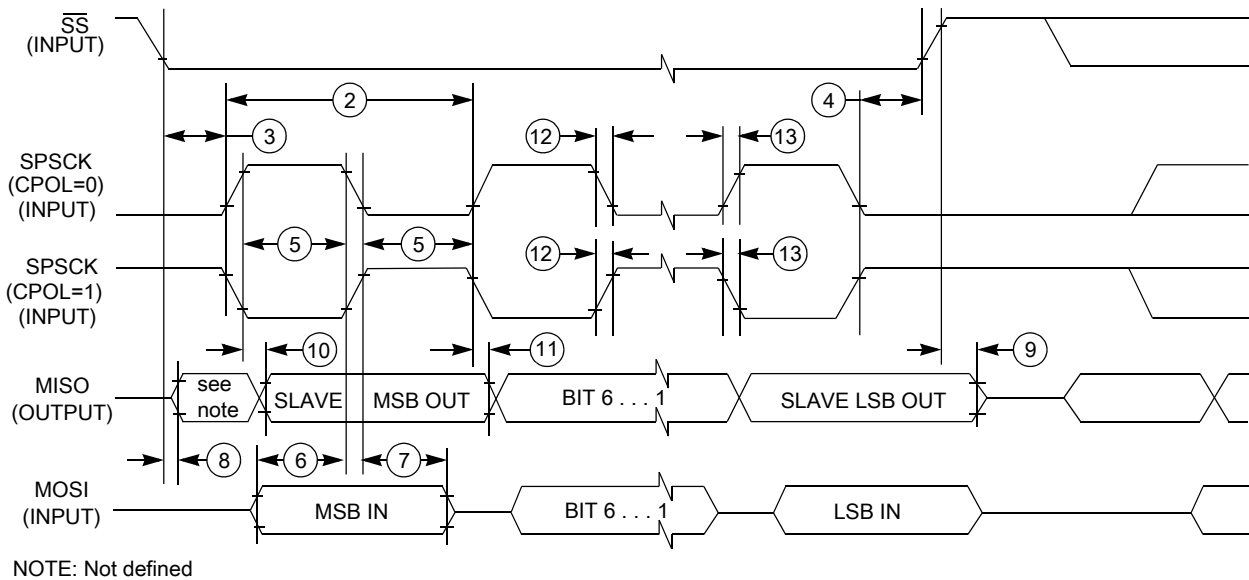


Figure 20. SPI slave mode timing (CPHA=1)

6.5 Human-machine interfaces (HMI)

Table 19. Pin availability by package pin-count

Pin Number				Lowest Priority <-- --> Highest				
64-LQFP 64-QFP	48-LQFP	44-LQFP	32-LQFP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
1	1	1	1	PTD1 ¹	KBI1P1	FTM2CH3	MOSI1	—
2	2	2	2	PTD0 ¹	KBI1P0	FTM2CH2	SPSCK1	—
3	—	—	—	PTH7	—	—	—	—
4	—	—	—	PTH6	—	—	—	—
5	3	3	—	PTE7	—	TCLK2	—	—
6	4	4	—	PTH2	—	BUSOUT	—	—
7	5	5	3	—	—	—	—	V _{DD}
8	6	6	4	—	—	—	V _{DDA}	V _{REFH}
9	7	7	5	—	—	—	V _{SSA}	V _{REFL}
10	8	8	6	—	—	—	—	V _{SS}
11	9	9	7	PTB7	—	SCL	—	EXTAL
12	10	10	8	PTB6	—	SDA	—	XTAL
13	11	11	—	—	—	—	—	V _{SS}
14	—	—	—	PTH1 ¹	—	FTM2CH1	—	—
15	—	—	—	PTH0 ¹	—	FTM2CH0	—	—
16	12	—	—	PTE6	—	—	—	—
17	13	—	—	PTE5	—	—	—	—
18	14	12	9	PTB5 ¹	FTM2CH5	$\overline{SS0}$	—	—
19	15	13	10	PTB4 ¹	FTM2CH4	MISO0	—	—
20	16	14	11	PTC3	FTM2CH3	—	ADP11	—
21	17	15	12	PTC2	FTM2CH2	—	ADP10	—
22	18	16	—	PTD7	KBI1P7	TXD2	—	—
23	19	17	—	PTD6	KBI1P6	RXD2	—	—
24	20	18	—	PTD5	KBI1P5	—	—	—
25	21	19	13	PTC1	—	FTM2CH1	ADP9	TSI7
26	22	20	14	PTC0	—	FTM2CH0	ADP8	TSI6
27	—	—	—	PTF7	—	—	ADP15	—
28	—	—	—	PTF6	—	—	ADP14	—
29	—	—	—	PTF5	—	—	ADP13	—
30	—	—	—	PTF4	—	—	ADP12	—
31	23	21	15	PTB3	KBI0P7	MOSI0	ADP7	TSI5
32	24	22	16	PTB2	KBI0P6	SPSCK0	ADP6	TSI4
33	25	23	17	PTB1	KBI0P5	TXD0	ADP5	TSI3
34	26	24	18	PTB0	KBI0P4	RXD0	ADP4	TSI2
35	—	—	—	PTF3	—	—	—	TSI15
36	—	—	—	PTF2	—	—	—	TSI14
37	27	25	19	PTA7	FTM2FAULT2	—	ADP3	TSI1

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already enabled can cause spurious edges to the lower priority module. Disable all modules that share a pin before enabling another module.

8.2 Device pin assignment

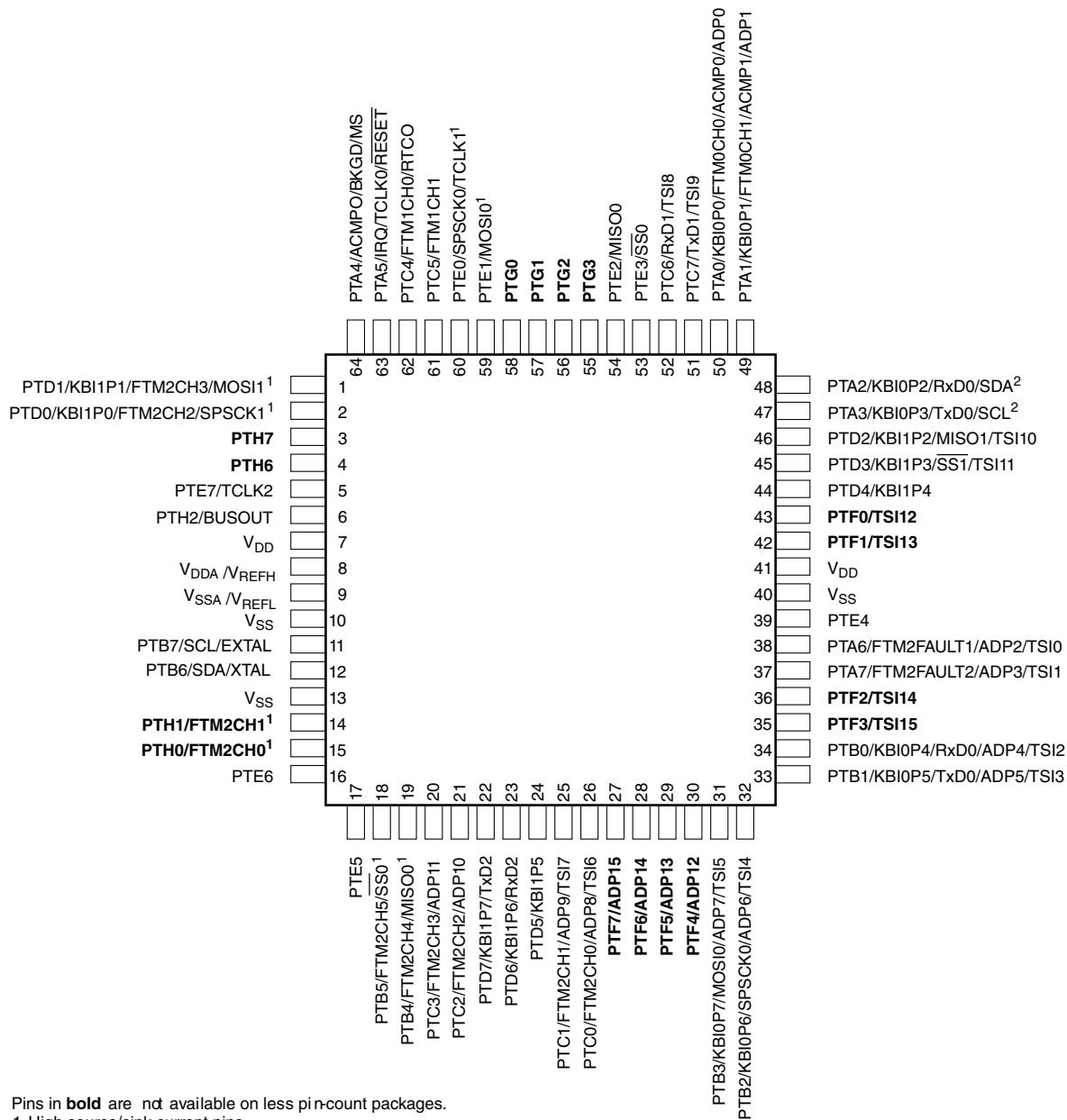


Figure 21. MC9S08PT60 64-pin QFP and LQFP package

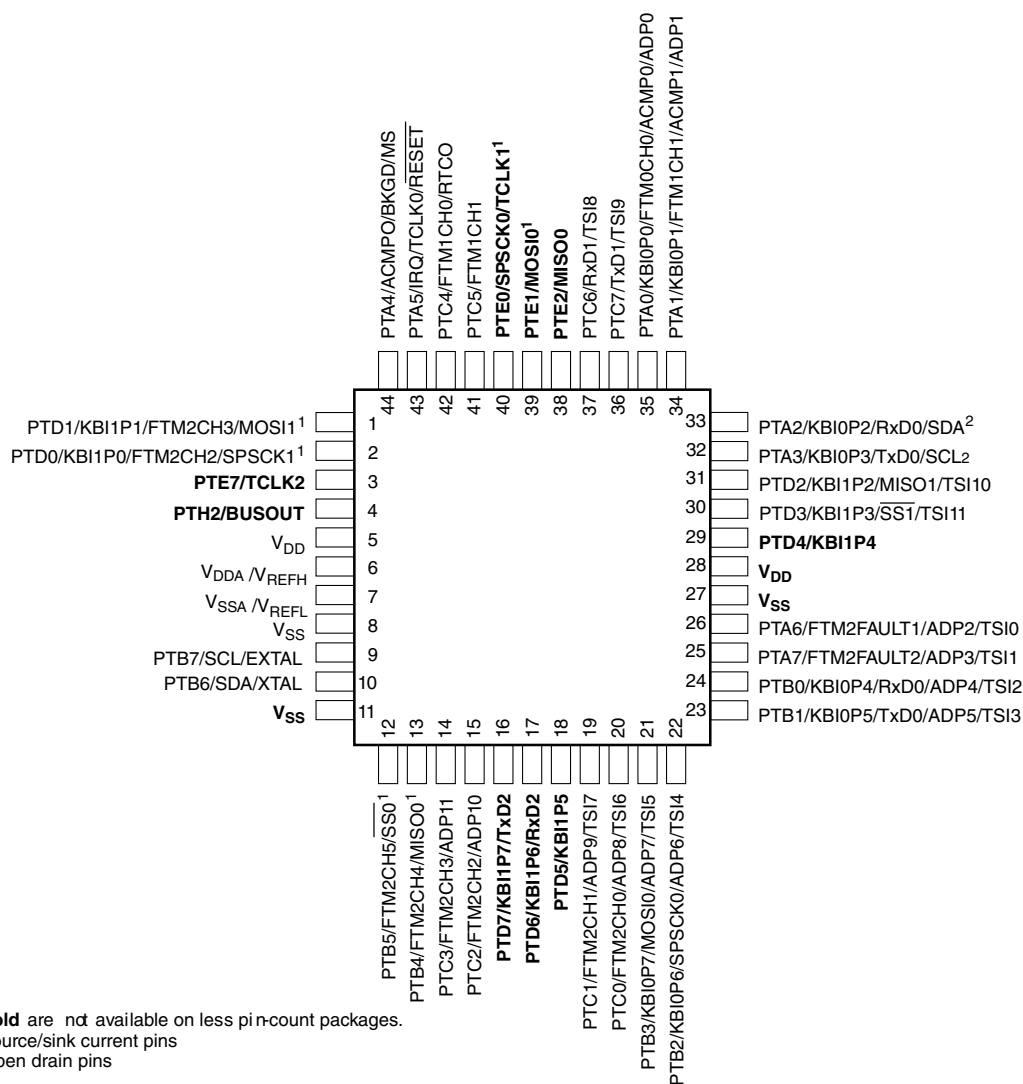


Figure 23. MC9S08PT60 44-pin LQFP package

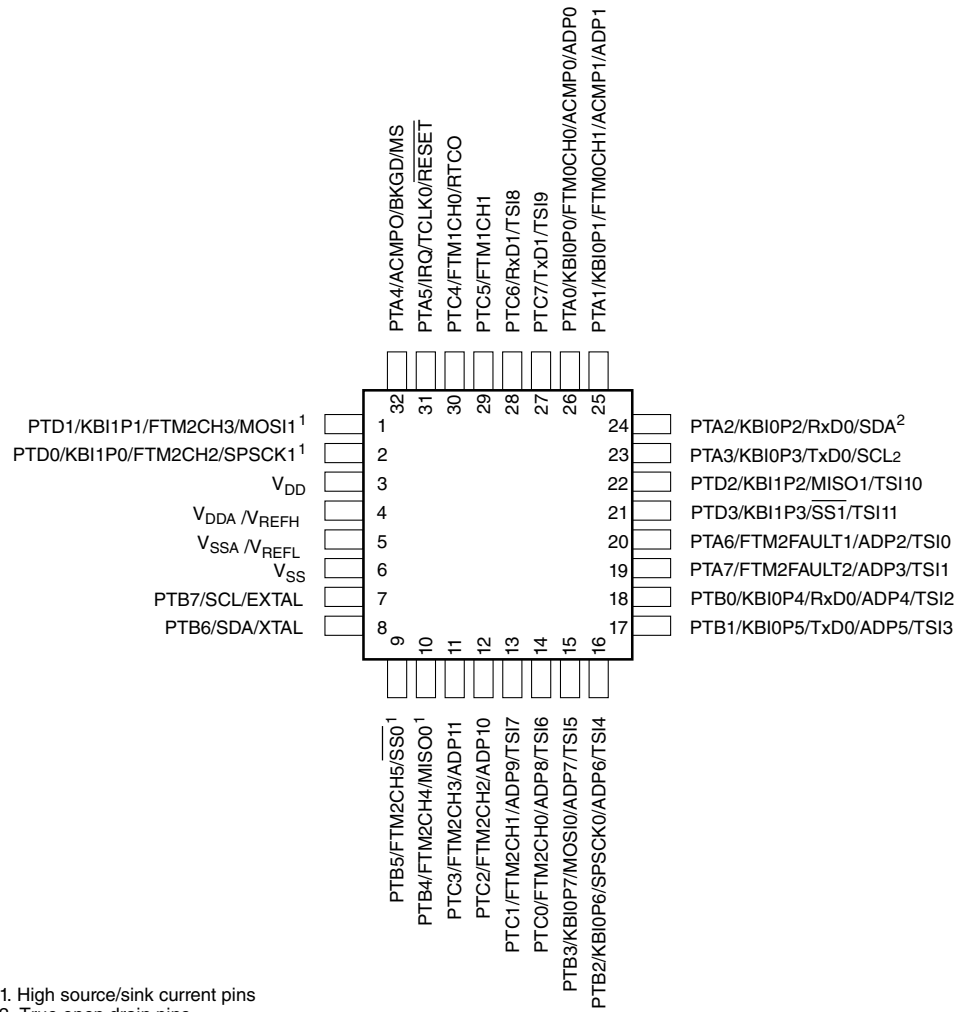


Figure 24. MC9S08PT60 32-pin LQFP package

9 Revision history

The following table provides a revision history for this document.

Table 20. Revision history

Rev. No.	Date	Substantial Changes
1	10/2011	Initial public revision.
2	11/2011	- Updated some TBDs - Updated LVD and POR data - Updated ADC data - Updated SPI data - Updated TSI data.
3	4/2012	- Finished all the TBDs - Updated package information
4	09/2014	Updated V_{HBM} in ESD handling ratings

Table continues on the next page...

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