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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	41
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08pt60avlf

- Input/Output
 - Up to 57 GPIOs including one output-only pin
 - Two 8-bit keyboard interrupt modules (KBI)
 - Two true open-drain output pins
 - Eight, ultra-high current sink pins supporting 20 mA source/sink current
- Package options
 - 64-pin LQFP; 64-pin QFP
 - 48-pin LQFP
 - 44-pin LQFP
 - 32-pin LQFP

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Table 2. DC characteristics (continued)

Symbol	C	Descriptions			Min	Typical ¹	Max	Unit
I _{OHT}	D	Output high current	Max total I _{OH} for all ports	5 V	—	—	-100	mA
				3 V	—	—	-50	
V _{OL}	P	Output low voltage	All I/O pins, standard-drive strength	5 V, I _{load} = 5 mA	—	—	0.8	V
	C			3 V, I _{load} = 2.5 mA	—	—	0.8	V
	P	Output low voltage	High current drive pins, high-drive strength ²	5 V, I _{load} = 20 mA	—	—	0.8	V
	C			3 V, I _{load} = 10 mA	—	—	0.8	V
I _{OLT}	D	Output low current	Max total I _{OL} for all ports	5 V	—	—	100	mA
				3 V	—	—	50	
V _{IH}	P	Input high voltage	All digital inputs	V _{DD} > 4.5V	0.70 × V _{DD}	—	—	V
	C			V _{DD} > 2.7V	0.75 × V _{DD}	—	—	
V _{IL}	P	Input low voltage	All digital inputs	V _{DD} > 4.5V	—	—	0.30 × V _{DD}	V
	C			V _{DD} > 2.7V	—	—	0.35 × V _{DD}	
V _{hys}	C	Input hysteresis	All digital inputs	—	0.06 × V _{DD}	—	—	mV
I _{IN}	P	Input leakage current	All input only pins (per pin)	V _{IN} = V _{DD} or V _{SS}	—	0.1	1	μA
I _{OZ}	P	Hi-Z (off-state) leakage current	All input/output (per pin)	V _{IN} = V _{DD} or V _{SS}	—	0.1	1	μA
I _{OZTOT}	C	Total leakage combined for all inputs and Hi-Z pins	All input only and I/O	V _{IN} = V _{DD} or V _{SS}	—	—	2	μA
R _{PU}	P	Pullup resistors	All digital inputs, when enabled (all I/O pins other than PTA2 and PTA3)	—	30.0	—	50.0	kΩ
R _{PU} ³	P	Pullup resistors	PTA2 and PTA3 pin	—	30.0	—	60.0	kΩ
I _{IC}	D	DC injection current ^{4, 5, 6}	Single pin limit	V _{IN} < V _{SS} , V _{IN} > V _{DD}	-0.2	—	2	mA
			Total MCU limit, includes sum of all stressed pins		-5	—	25	
C _{in}	C	Input capacitance, all pins		—	—	—	7	pF
V _{RAM}	C	RAM retention voltage		—	2.0	—	—	V

- Typical values are measured at 25 °C. Characterized, not tested.
- Only PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0, and PTH1 support ultra high current output.
- The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
- All functional non-supply pins, except for PTA2 and PTA3, are internally clamped to V_{SS} and V_{DD}.
- Input must be current-limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the large one.

6. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{IN} > V_{DD}$) is higher than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current higher than maximum injection current when the MCU is not consuming power, such as no system clock is present, or clock rate is very low (which would reduce overall power consumption).

Table 3. LVD and POR Specification

Symbol	C	Description		Min	Typ	Max	Unit
V _{POR}	D	POR re-arm voltage ^{1, 2}		1.5	1.75	2.0	V
V _{LVDH}	C	Falling low-voltage detect threshold - high range (LVDV = 1) ³		4.2	4.3	4.4	V
V _{LVW1H}	C	Falling low-voltage warning threshold - high range	Level 1 falling (LVWV = 00)	4.3	4.4	4.5	V
V _{LVW2H}	C		Level 2 falling (LVWV = 01)	4.5	4.5	4.6	V
V _{LVW3H}	C		Level 3 falling (LVWV = 10)	4.6	4.6	4.7	V
V _{LVW4H}	C		Level 4 falling (LVWV = 11)	4.7	4.7	4.8	V
V _{HYSH}	C	High range low-voltage detect/warning hysteresis		—	100	—	mV
V _{LVDL}	C	Falling low-voltage detect threshold - low range (LVDV = 0)		2.56	2.61	2.66	V
V _{LVDW1L}	C	Falling low-voltage warning threshold - low range	Level 1 falling (LVWV = 00)	2.62	2.7	2.78	V
V _{LVDW2L}	C		Level 2 falling (LVWV = 01)	2.72	2.8	2.88	V
V _{LVDW3L}	C		Level 3 falling (LVWV = 10)	2.82	2.9	2.98	V
V _{LVDW4L}	C		Level 4 falling (LVWV = 11)	2.92	3.0	3.08	V
V _{HYSDL}	C	Low range low-voltage detect hysteresis		—	40	—	mV
V _{HYSWL}	C	Low range low-voltage warning hysteresis		—	80	—	mV
V _{BG}	P	Buffered bandgap output ⁴		1.14	1.16	1.18	V

1. Maximum is highest voltage that POR is guaranteed.
2. POR ramp time must be longer than 20us/V to get a stable startup.
3. Rising thresholds are falling threshold + hysteresis.
4. Voltage factory trimmed at $V_{DD} = 5.0$ V, Temp = 25 °C

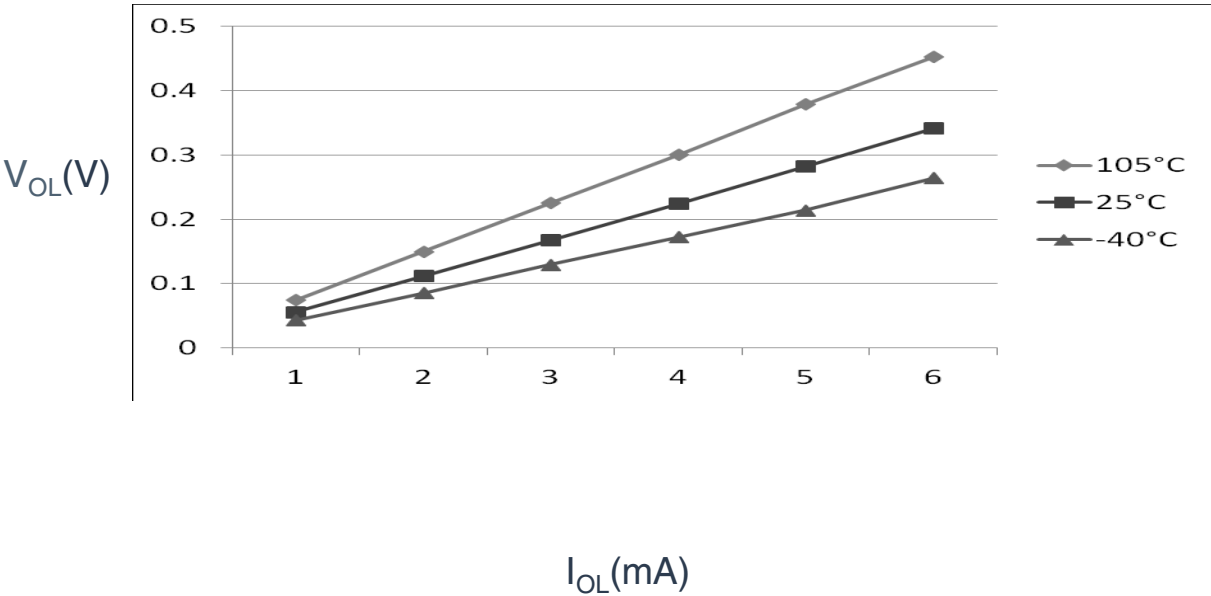


Figure 5. Typical I_{OL} Vs. V_{OL} (standard drive strength) ($V_{DD} = 5$ V)

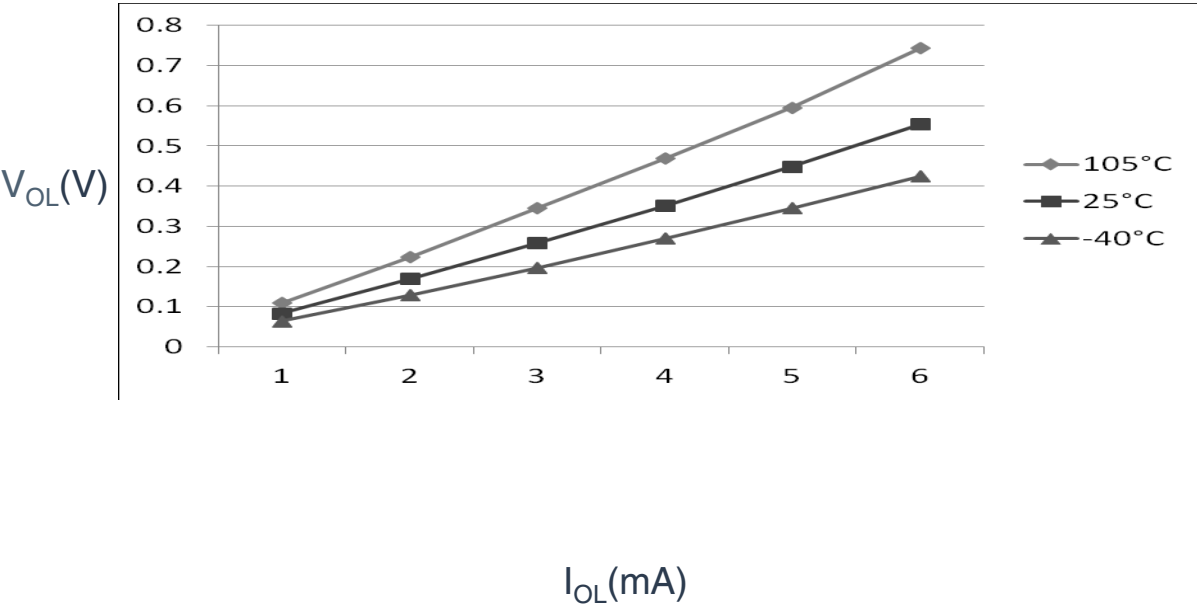


Figure 6. Typical I_{OL} Vs. V_{OL} (standard drive strength) ($V_{DD} = 3$ V)

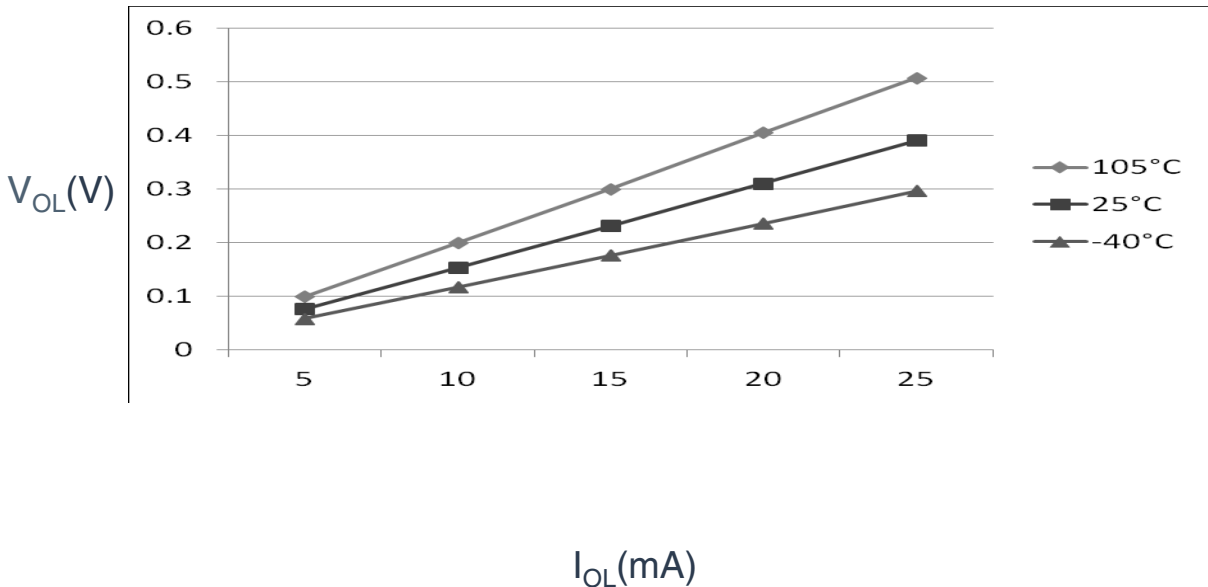


Figure 7. Typical I_{OL} Vs. V_{OL} (high drive strength) ($V_{DD} = 5\text{ V}$)

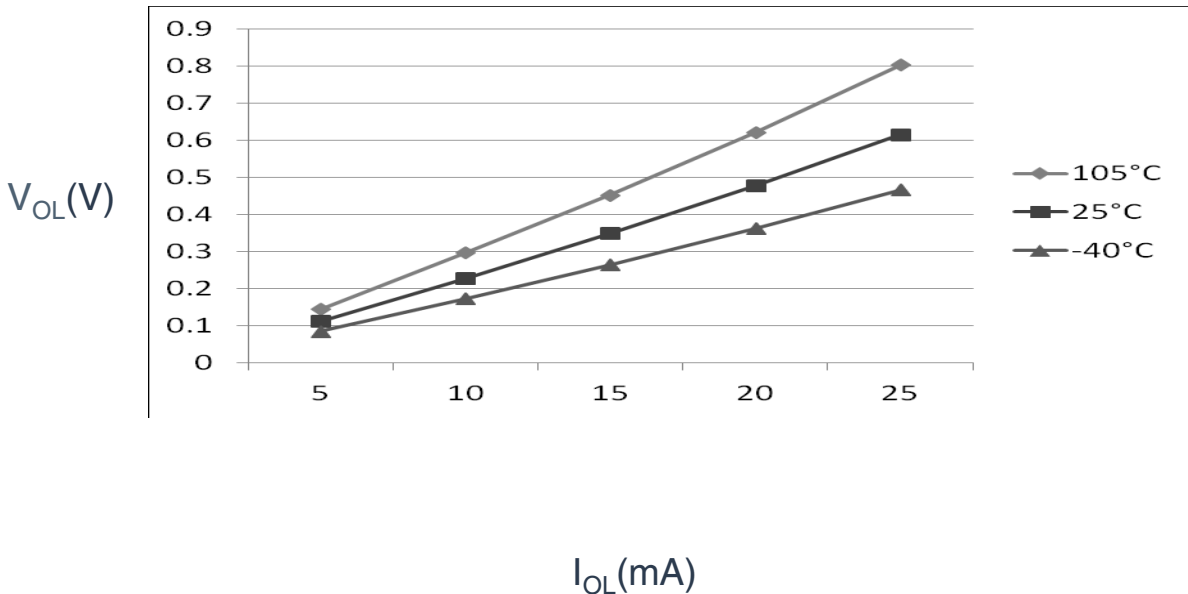


Figure 8. Typical I_{OL} Vs. V_{OL} (high drive strength) ($V_{DD} = 3\text{ V}$)

Table 10. Thermal attributes (continued)

Board type	Symbol	Description	64 LQFP	64 QFP	48 LQFP	44 LQFP	32 LQFP	Unit	Notes
—	$R_{\theta JB}$	Thermal resistance, junction to board	35	32	34	34	33	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	20	23	24	20	24	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	5	8	6	5	6	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization.

6 Peripheral operating requirements and behaviors

6.1 External oscillator (XOSC) and ICS characteristics

Table 11. XOSC and ICS specifications (temperature range = -40 to 105 °C ambient)

Num	C	Characteristic		Symbol	Min	Typical ¹	Max	Unit
1	C	Oscillator crystal or resonator	Low range (RANGE = 0)	f_{lo}	31.25	32.768	39.0625	kHz
	C		High range (RANGE = 1) FEE or FBE mode ²	f_{hi}	4	—	20	MHz
	C		High range (RANGE = 1), high gain (HGO = 1), FBELP mode	f_{hi}	4	—	20	MHz
	C		High range (RANGE = 1), low power (HGO = 0), FBELP mode	f_{hi}	4	—	20	MHz
2	D	Load capacitors		C1, C2	See Note ³			
3	D	Feedback resistor	Low Frequency, Low-Power Mode ⁴	R_F	—	—	—	MΩ
			Low Frequency, High-Gain Mode		—	10	—	MΩ
			High Frequency, Low-Power Mode		—	1	—	MΩ

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**Table 11. XOSC and ICS specifications (temperature range = -40 to 105 °C ambient)
(continued)**

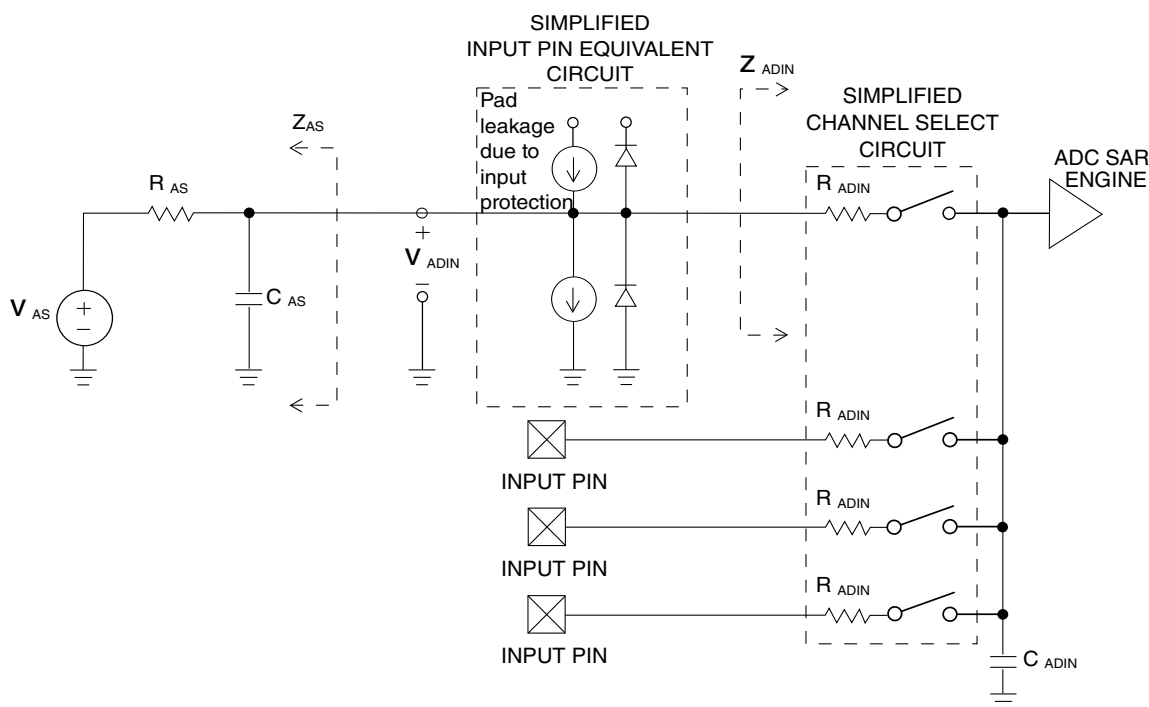
Num	C	Characteristic		Symbol	Min	Typical ¹	Max	Unit
			High Frequency, High-Gain Mode		—	1	—	MΩ
4	D	Series resistor - Low Frequency	Low-Power Mode ⁴	R _S	—	—	—	kΩ
			High-Gain Mode		—	200	—	kΩ
5	D	Series resistor - High Frequency	Low-Power Mode ⁴	R _S	—	—	—	kΩ
	D	Series resistor - High Frequency, High-Gain Mode	4 MHz		—	0	—	kΩ
	D		8 MHz		—	0	—	kΩ
	D		16 MHz		—	0	—	kΩ
6	C	Crystal start-up time Low range = 32.768 kHz crystal; High range = 20 MHz crystal ^{5, 6}	Low range, low power	t _{CSTL}	—	1000	—	ms
	C		Low range, high power	t _{CSTH}	—	800	—	ms
	C		High range, low power		—	3	—	ms
	C		High range, high power		—	1.5	—	ms
7	T	Internal reference start-up time		t _{IRST}	—	20	50	μs
8	D	Square wave input clock frequency	FEE or FBE mode ²	f _{extal}	0.03125	—	5	MHz
	D		FBELP mode		0	—	20	MHz
9	P	Average internal reference frequency - trimmed		f _{int_t}	—	32.768	—	kHz
10	P	DCO output frequency range - trimmed		f _{dco_t}	16	—	20	MHz
11	P	Total deviation of DCO output from trimmed frequency ⁵	Over full voltage and temperature range	Δf _{dco_t}	—	—	±2.0	%f _{dco}
	C		Over fixed voltage and temperature range of 0 to 70 °C				±1.0	
12	C	FLL acquisition time ^{5, 7}		t _{Acquire}	—	—	2	ms
13	C	Long term jitter of DCO output clock (averaged over 2 ms interval) ⁸		C _{Jitter}	—	0.02	0.2	%f _{dco}

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. When ICS is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.
3. See crystal or resonator manufacturer's recommendation.
4. Load capacitors (C₁, C₂), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.
5. This parameter is characterized and not tested on each device.
6. Proper PC board layout procedures must be followed to achieve specifications.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

Table 13. 5 V 12-bit ADC operating conditions (continued)

Characteristic	Conditions	Symb	Min	Typ ¹	Max	Unit	Comment
	10-bit mode		—	—	5		
	• $f_{ADCK} > 4$ MHz		—	—	10		
	• $f_{ADCK} < 4$ MHz		—	—	10		
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC conversion clock frequency	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	—
	Low power (ADLPC=1)		0.4	—	4.0		

- Typical values assume $V_{DDA} = 5.0$ V, Temp = 25°C, $f_{ADCK} = 1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- DC potential difference.


Figure 16. ADC input impedance equivalency diagram
Table 14. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Characteristic	Conditions	C	Symb	Min	Typ ¹	Max	Unit
Supply current		T	I_{DDA}	—	133	—	μ A
ADLPC = 1							
ADLSMP = 1							
ADCO = 1							
Supply current		T	I_{DDA}	—	218	—	μ A

Table continues on the next page...

Table 14. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Characteristic	Conditions	C	Symb	Min	Typ ¹	Max	Unit
ADLPC = 1 ADLSMP = 0 ADCO = 1							
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	327	—	μA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	I_{DDAD}	—	582	990	μA
Supply current	Stop, reset, module off	T	I_{DDA}	—	0.011	1	μA
ADC asynchronous clock source	High speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz
	Low power (ADLPC = 1)			1.25	2	3.3	
Conversion time (including sample time)	Short sample (ADLSMP = 0)	T	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	40	—	
Sample time	Short sample (ADLSMP = 0)	T	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted Error ²	12-bit mode	T	E_{TUE}	—	± 5.0	—	LSB ³
	10-bit mode	P		—	± 1.5	± 2.0	
	8-bit mode	P		—	± 0.7	± 1.0	
Differential Non-Linearity	12-bit mode	T	DNL	—	± 1.0	—	LSB ³
	10-bit mode ⁴	P		—	± 0.25	± 0.5	
	8-bit mode ⁴	P		—	± 0.15	± 0.25	
Integral Non-Linearity	12-bit mode	T	INL	—	± 1.0	—	LSB ³
	10-bit mode	T		—	± 0.3	± 0.5	
	8-bit mode	T		—	± 0.15	± 0.25	
Zero-scale error ⁵	12-bit mode	C	E_{ZS}	—	± 2.0	—	LSB ³
	10-bit mode	P		—	± 0.25	± 1.0	
	8-bit mode	P		—	± 0.65	± 1.0	
Full-scale error ⁶	12-bit mode	T	E_{FS}	—	± 2.5	—	LSB ³
	10-bit mode	T		—	± 0.5	± 1.0	
	8-bit mode	T		—	± 0.5	± 1.0	
Quantization error	≤ 12 bit modes	D	E_Q	—	—	± 0.5	LSB ³

Table continues on the next page...

Table 14. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Characteristic	Conditions	C	Symb	Min	Typ ¹	Max	Unit
Input leakage error ⁷	all modes	D	E_{IL}	$I_{IN} * R_{AS}$			mV
Temp sensor slope	-40°C– 25°C	D	m	—	3.266	—	mV/°C
	25°C– 125°C			—	3.638	—	
Temp sensor voltage	25°C	D	V_{TEMP25}	—	1.396	—	V

1. Typical values assume $V_{DDA} = 5.0$ V, Temp = 25°C, $f_{ADCK} = 1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Includes quantization.
3. $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
4. Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes
5. $V_{ADIN} = V_{SSA}$
6. $V_{ADIN} = V_{DDA}$
7. I_{IN} = leakage current (refer to DC characteristics)

6.3.2 Analog comparator (ACMP) electricals

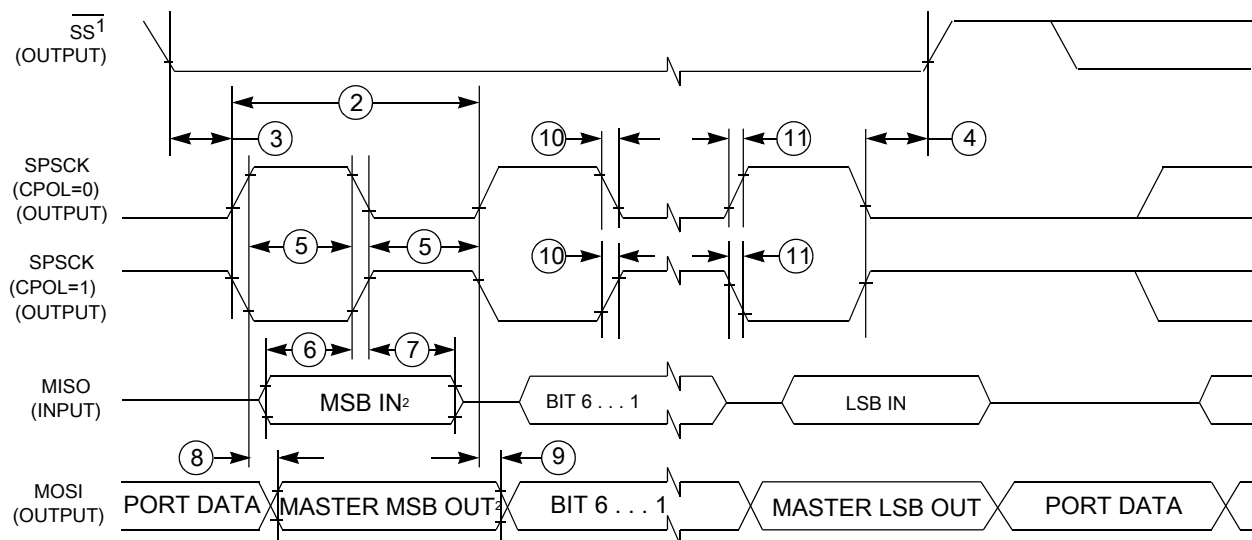
Table 15. Comparator electrical specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DDA}	2.7	—	5.5	V
T	Supply current (Operation mode)	I_{DDA}	—	10	20	μA
D	Analog input voltage	V_{AIN}	$V_{SS} - 0.3$	—	V_{DDA}	V
P	Analog input offset voltage	V_{AIO}	—	—	40	mV
C	Analog comparator hysteresis (HYST=0)	V_H	—	15	20	mV
C	Analog comparator hysteresis (HYST=1)	V_H	—	20	30	mV
T	Supply current (Off mode)	I_{DDAOFF}	—	60	—	nA
C	Propagation Delay	t_D	—	0.4	1	μs

6.4 Communication interfaces

6.4.1 SPI switching specifications

The serial peripheral interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the chip's reference manual for information about the modified transfer formats used for



1. If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. SPI master mode timing (CPHA=1)

Table 17. SPI slave mode timing

Nu m.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	0	$f_{Bus}/4$	Hz	f_{Bus} is the bus clock as defined in .
2	t_{SPSCCK}	SPSCCK period	$4 \times t_{Bus}$	—	ns	$t_{Bus} = 1/f_{Bus}$
3	t_{Lead}	Enable lead time	1	—	t_{Bus}	—
4	t_{Lag}	Enable lag time	1	—	t_{Bus}	—
5	$t_{WSPSCCK}$	Clock (SPSCCK) high or low time	$t_{Bus} - 30$	—	ns	—
6	t_{SU}	Data setup time (inputs)	15	—	ns	—
7	t_{HI}	Data hold time (inputs)	25	—	ns	—
8	t_a	Slave access time	—	t_{Bus}	ns	Time to data active from high-impedance state
9	t_{dis}	Slave MISO disable time	—	t_{Bus}	ns	Hold time to high-impedance state
10	t_v	Data valid (after SPSCCK edge)	—	25	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	$t_{Bus} - 25$	ns	—
	t_{FI}	Fall time input	—	$t_{Bus} - 25$	ns	—
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output	—	25	ns	—

6.5.1 TSI electrical specifications

Table 18. TSI electrical specifications

Symbol	Description	Min.	Type	Max	Unit
TSI_RUNF	Fixed power consumption in run mode	—	100	—	μA
TSI_RUNV	Variable power consumption in run mode (depends on oscillator's current selection)	1.0	—	128	μA
TSI_EN	Power consumption in enable mode	—	100	—	μA
TSI_DIS	Power consumption in disable mode	—	1.2	—	μA
TSI_TEN	TSI analog enable time	—	66	—	μs
TSI_CREF	TSI reference capacitor	—	1.0	—	pF
TSI_DVOLT	Voltage variation of VP & VM around nominal values	-10	—	10	%

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
32-pin LQFP	98ASH70029A
44-pin LQFP	98ASS23225W
48-pin LQFP	98ASH00962A
64-pin QFP	98ASB42844B
64-pin LQFP	98ASS23234W

8 Pinout

8.1 Signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

Table 19. Pin availability by package pin-count

Pin Number				Lowest Priority <-- --> Highest				
64-LQFP 64-QFP	48-LQFP	44-LQFP	32-LQFP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
1	1	1	1	PTD1 ¹	KBI1P1	FTM2CH3	MOSI1	—
2	2	2	2	PTD0 ¹	KBI1P0	FTM2CH2	SPSCK1	—
3	—	—	—	PTH7	—	—	—	—
4	—	—	—	PTH6	—	—	—	—
5	3	3	—	PTE7	—	TCLK2	—	—
6	4	4	—	PTH2	—	BUSOUT	—	—
7	5	5	3	—	—	—	—	V _{DD}
8	6	6	4	—	—	—	V _{DDA}	V _{REFH}
9	7	7	5	—	—	—	V _{SSA}	V _{REFL}
10	8	8	6	—	—	—	—	V _{SS}
11	9	9	7	PTB7	—	SCL	—	EXTAL
12	10	10	8	PTB6	—	SDA	—	XTAL
13	11	11	—	—	—	—	—	V _{SS}
14	—	—	—	PTH1 ¹	—	FTM2CH1	—	—
15	—	—	—	PTH0 ¹	—	FTM2CH0	—	—
16	12	—	—	PTE6	—	—	—	—
17	13	—	—	PTE5	—	—	—	—
18	14	12	9	PTB5 ¹	FTM2CH5	$\overline{SS0}$	—	—
19	15	13	10	PTB4 ¹	FTM2CH4	MISO0	—	—
20	16	14	11	PTC3	FTM2CH3	—	ADP11	—
21	17	15	12	PTC2	FTM2CH2	—	ADP10	—
22	18	16	—	PTD7	KBI1P7	TXD2	—	—
23	19	17	—	PTD6	KBI1P6	RXD2	—	—
24	20	18	—	PTD5	KBI1P5	—	—	—
25	21	19	13	PTC1	—	FTM2CH1	ADP9	TSI7
26	22	20	14	PTC0	—	FTM2CH0	ADP8	TSI6
27	—	—	—	PTF7	—	—	ADP15	—
28	—	—	—	PTF6	—	—	ADP14	—
29	—	—	—	PTF5	—	—	ADP13	—
30	—	—	—	PTF4	—	—	ADP12	—
31	23	21	15	PTB3	KBI0P7	MOSI0	ADP7	TSI5
32	24	22	16	PTB2	KBI0P6	SPSCK0	ADP6	TSI4
33	25	23	17	PTB1	KBI0P5	TXD0	ADP5	TSI3
34	26	24	18	PTB0	KBI0P4	RXD0	ADP4	TSI2
35	—	—	—	PTF3	—	—	—	TSI15
36	—	—	—	PTF2	—	—	—	TSI14
37	27	25	19	PTA7	FTM2FAULT2	—	ADP3	TSI1

Table continues on the next page...

Table 19. Pin availability by package pin-count (continued)

Pin Number				Lowest Priority <-- --> Highest				
64-LQFP 64-QFP	48-LQFP	44-LQFP	32-LQFP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
38	28	26	20	PTA6	FTM2FAULT1	—	ADP2	TSI0
39	29	—	—	PTE4	—	—	—	—
40	30	27	—	—	—	—	—	V _{SS}
41	31	28	—	—	—	—	—	V _{DD}
42	—	—	—	PTF1	—	—	—	TSI13
43	—	—	—	PTF0	—	—	—	TSI12
44	32	29	—	PTD4	KBI1P4	—	—	—
45	33	30	21	PTD3	KBI1P3	$\overline{SS1}$	—	TSI11
46	34	31	22	PTD2	KBI1P2	MISO1	—	TSI10
47	35	32	23	PTA3 ²	KBI0P3	TXD0	SCL	—
48	36	33	24	PTA2 ²	KBI0P2	RXD0	SDA	—
49	37	34	25	PTA1	KBI0P1	FTM0CH1	ACMP1	ADP1
50	38	35	26	PTA0	KBI0P0	FTM0CH0	ACMP0	ADP0
51	39	36	27	PTC7	—	TxD1	—	TSI9
52	40	37	28	PTC6	—	RxD1	—	TSI8
53	41	—	—	PTE3	—	$\overline{SS0}$	—	—
54	42	38	—	PTE2	—	MISO0	—	—
55	—	—	—	PTG3	—	—	—	—
56	—	—	—	PTG2	—	—	—	—
57	—	—	—	PTG1	—	—	—	—
58	—	—	—	PTG0	—	—	—	—
59	43	39	—	PTE1 ¹	—	MOSI0	—	—
60	44	40	—	PTE0 ¹	—	SPSCK0	TCLK1	—
61	45	41	29	PTC5	—	FTM1CH1	—	—
62	46	42	30	PTC4	—	FTM1CH0	RTCO	—
63	47	43	31	PTA5	IRQ	TCLK0	—	$\overline{RESET}$
64	48	44	32	PTA4	—	ACMPO	BKGD	MS

1. This is a high current drive pin when operated as output.
2. This is a true open-drain pin when operated as output.

Note

When an alternative function is first enabled, it is possible to get a spurious edge to the module. User software must clear any associated flags before interrupts are enabled. The table above illustrates the priority if multiple modules are enabled. The highest priority module will have control over the pin. Selecting a higher priority pin function with a lower priority function

already enabled can cause spurious edges to the lower priority module. Disable all modules that share a pin before enabling another module.

8.2 Device pin assignment

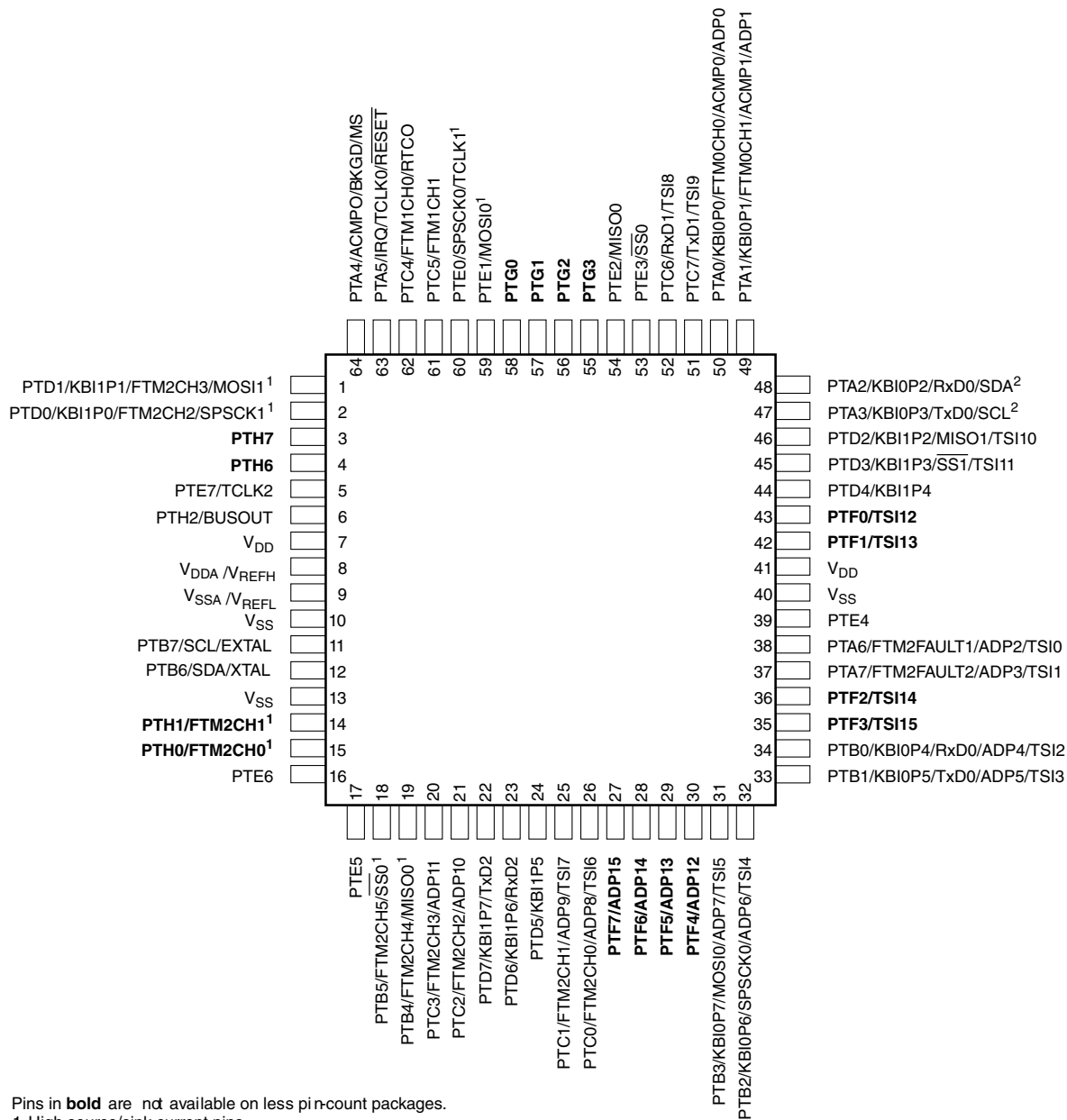


Figure 21. MC9S08PT60 64-pin QFP and LQFP package

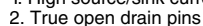
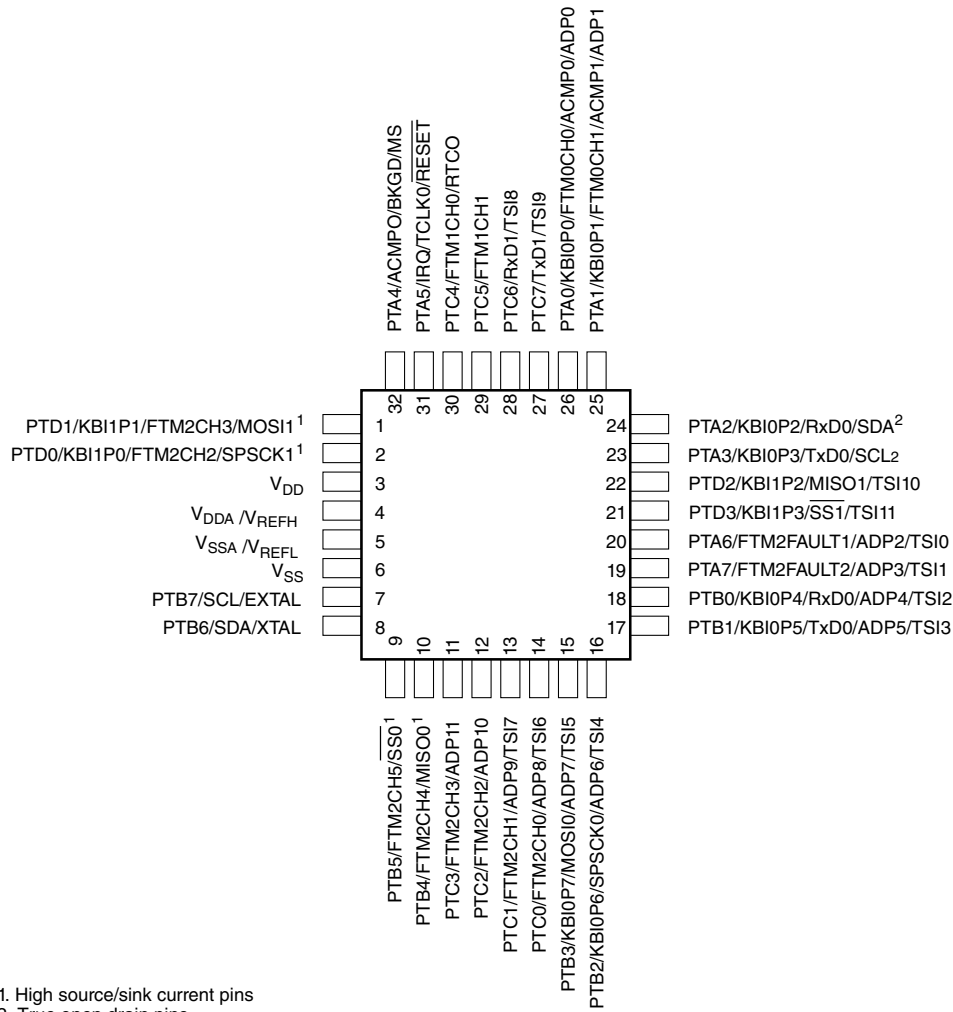


Figure 23. MC9S08PT60 44-pin LQFP package



1. High source/sink current pins
2. True open drain pins

Figure 24. MC9S08PT60 32-pin LQFP package

9 Revision history

The following table provides a revision history for this document.

Table 20. Revision history

Rev. No.	Date	Substantial Changes
1	10/2011	Initial public revision.
2	11/2011	- Updated some TBDs - Updated LVD and POR data - Updated ADC data - Updated SPI data - Updated TSI data.
3	4/2012	- Finished all the TBDs - Updated package information
4	09/2014	Updated V_{HBM} in ESD handling ratings

Table continues on the next page...

Table 20. Revision history (continued)

Rev. No.	Date	Substantial Changes
		- Updated V_{DD} and V_{DIO} in Voltage and current operating ratings - Updated the specs and figures in DC characteristics - Updated Thermal characteristics - Updated f_{IO} and the footnote to the $t_{Acquire}$ in External oscillator (XOSC) and ICS characteristics - Updated footnote on the $S3I_{DD}$ in Supply current characteristics - Updated flash characteristics in NVM specifications - Added EMC radiated emissions operating behaviors - Updated V_{OH} and V_{OL} in DC characteristics - Updated the rating descriptions for t_{Rise} and t_{Fall} in Control timing - Updated the assumption for all the timing values in SPI switching specifications - Updated the part number format to add new field for new part numbers in Fields.
5	06/2015	- Corrected the Min. of the t_{extrst} in Control timing - Added new section of Thermal operating requirements, Updated Thermal characteristics to remove redundant information.

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