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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	LC87F0K08A
Core Size	8-Bit
Speed	12MHz
Connectivity	SIO, UART/USART
Peripherals	LVD, POR, WDT
Number of I/O	9
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 9
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	24-SDIP (0.300", 7.62mm)
Supplier Device Package	24-PDIP/DIPS
Purchase URL	https://www.e-xfl.com/product-detail/onsemi/lc87f0k08auda-e

■ Timers

- Timer 0 : 16-bit timer/counter with a capture register
  - Mode 0 : 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) ×2 channels
  - Mode 1 : 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) + 8-bit counter (with an 8-bit capture register)
  - Mode 2 : 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)
  - Mode 3 : 16-bit counter (with a 16-bit capture register)
- Timer 1 : 16-bit timer/counter
  - Mode 0 : 8-bit timer with an 8-bit prescaler + 8-bit timer/counter with an 8-bit prescaler
  - Mode 2 : 16-bit timer/counter with an 8-bit prescaler
  - Mode 3 : 16-bit timer with an 8-bit prescaler
- Timer 6 : 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Timer 7 : 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Base timer
  1) The clock is selectable from the system clock and timer 0 prescaler output.
  2) Interrupts are programmable in 5 different time schemes

■ Serial interface

- SIO1 : 8-bit synchronous serial interface
  - Mode 0 : Synchronous 8-bit serial I/O (2-wire configuration, 2 to 512 Tcyc transfer clocks)
  - Mode 2 : Bus mode 1 (start bit, 8 data bits, 2 to 512 Tcyc transfer clocks)
  - Mode 3 : Bus mode 2 (start detect, 8 data bits, stop detect)

■ UART

- Full duplex
- 7 / 8 / 9 bit data bits selectable
- 1 stop bit (2 bits in continuous data transmission)
- Built-in baudrate generator

■ AD converter : 12 bits × 5 channels

- 12 / 8-bit AD converter resolution selectable

■ Remote control receiver circuit (multiplexed with P07 / INT3 / T0IN pin)

- Noise rejection function (noise filter time constant selectable from 1 Tcyc / 32 Tcyc / 128 Tcyc)

■ Analog comparator : 8 channels

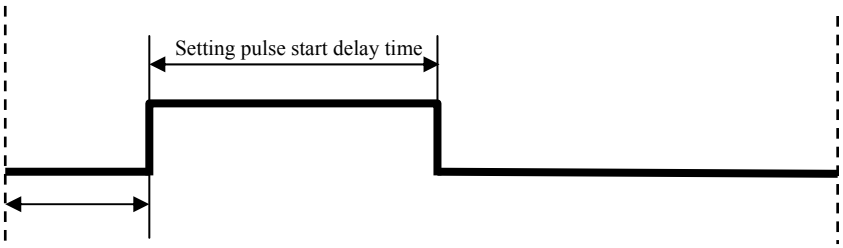
- CMP1 : "+" and "–" input pins
  Output : For PPG output timing generation and capture timer input (INT2)
- CMP2 : "+" input pin,
  "–" input is the internal Vref (user selectable options : 5/12, 6/12, or 7/12 VDD).
  Output for interrupt flag setting (CMP2)
- CMP3 : "+" input is the output of AMP1.
  "–" input is the internal Vref (user selectable options: 1/6, 2/6, 3/6, or 4/6 VDD).
  Output for the PPG output control (only the existing cycle set to OFF), capture trigger of pulse on time and interrupt flag set (CMP3)
- CMP4 : "+" and "–" input pins
  Output for the PPG output control (forced OFF)
- CMP5 : "–" input pin, "+" input is multiplexed with the "–" input pin of CMP4
  Output for the PPG output control (forced OFF)
- CMP6 : "+" input pin, "–" input is the internal Vref (register setting: 1/6, 2/6, 3/6, or 4/6 VDD)
  Output for the PPG output control (forced OFF) and interrupt flag set (CMP6)
- CMP7 : "+" input is multiplexed with the "+" input pin of CMP2
  "–" input is the internal Vref (user selectable options: 6/12, 7/12, or 8/12 VDD)
  Output for the PPG output control (forced OFF) and interrupt flag set (CMP7).
- CMP8 : "+" input is multiplexed with the "+" input pin of CMP3
  "–" input is the internal Vref (register setting: 1/6, 2/6, 3/6, or 4/6 VDD)
  Output for capture trigger of pulse on time and interrupt flag set (CMP8)

■ AMP circuit : 2 channels

- AMP1 : The gain is set by user selectable options (6× / 8× / 10×).
  Input pin (AMP1I)
  Output is CMP3 input, CMP8 input and AMP2 input.
- AMP2 : The gain (1× / 2× / 4×) is set by using a register.
  Input is AMP1 output.
  Output pin (AMP2O)

■ IGBT control circuit (PPG2) : 1 channel

- Output sync signal switching : Set by a register (1-pulse output / continuous pulse output synchronized with the CMP1 output)
- Duty control : Pulse start delay time and pulse on time with respect to a sync signal are set by using a register.
- PPG output control using CMP3 to CMP7 outputs
- Surge detection using CMP4 / 5 / 6 outputs
- CMP1 output : Pulse signal timing detection
- Output polarity selectable : User selectable options



■ Clock output function

Capable of generating a clock output with a frequency of $\frac{1}{1}$, $\frac{1}{2}$, $\frac{1}{4}$, $\frac{1}{8}$, $\frac{1}{16}$, $\frac{1}{32}$, or $\frac{1}{64}$ of the source oscillator clock selected as the system clock.

■ Watchdog timer

- Can generate an internal reset signal on an overflow of timer that is running on the internal low-speed RC oscillation clock (30 kHz).
- Allows selection of continue, stop, or hold mode operation of the counter on entry into the HALT/HOLD mode.

■ Interrupts

- 21 sources, 10 vector addresses
  1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt request of the level equal to or lower than the current interrupt is not accepted.
  2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, an interrupt into the smallest vector address is given priority.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	CMP2 / CMP7
2	0000BH	X or L	CMP3 / CMP8
3	00013H	H or L	INT2 / T0L / INT4
4	0001BH	H or L	INT3 / base timer
5	00023H	H or L	T0H
6	0002BH	H or L	T1L / T1H
7	00033H	H or L	UART receive
8	0003BH	H or L	SIO1 / UART transmit
9	00043H	H or L	ADC / T6 / T7 / CMP1TO
10	0004BH	H or L	CMP6 / Surge detection

- Priority levels X > H > L
- For interrupts of the same level, an interrupt with a smaller vector address is given priority.

■ Subroutine stack levels : Up to 192 levels (the stack is allocated in RAM.)

■ Internal high-speed multiplication/division instructions

- 16 bits × 8 bits (5 Tcyc execution time)
- 24 bits × 16 bits (12 Tcyc execution time)
- 16 bits ÷ 8 bits (8 Tcyc execution time)
- 24 bits ÷ 16 bits (12 Tcyc execution time)

■ Oscillation circuits

- Internal oscillation circuits

  Low-speed RC oscillation circuit : For system clock /Watch dog timer (30 kHz)
  Medium-speed RC oscillation circuit : For system clock (1 MHz)
  High-speed RC oscillation circuit : For system clock /PPG clock (24 MHz)
  *The clock divided by two is used for system clock (12 MHz).

■ System clock divider function

- Can run on low current.
- The minimum instruction cycle selectable from 250 ns, 500 ns, 1 μs, 2 μs, 4 μs, 8 μs, 16 μs, 32 μs, and 64 μs (at a main clock rate of 12 MHz).

■ Internal reset circuit

- Power-on reset (POR) function
  1) POR reset is generated only at power-on time.
  2) The POR release level can be selected from 5 levels (2.37 V, 2.57 V, 2.87 V, 3.86 V, and 4.35 V) by configuring options.
- Low-voltage detection reset (LVD) function
  1) LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.
  2) The use/disuse of the LVD function and the low voltage threshold level (5 levels: 2.31 V, 2.51 V, 2.81 V, 3.79 V, 4.28 V) selectable by configuring options.

■ Standby function

- HALT mode : Halts instruction execution while allowing the peripheral circuits to continue operation.
  1) Oscillation is not halted automatically.
  2) There are three ways of releasing the HALT mode.
     (1) Setting the reset pin to the low level
     (2) System resetting by watchdog timer or low-voltage detection
     (3) Occurrence of an interrupt

- HOLD mode : Suspends instruction execution and the operation of the peripheral circuits.
  1) The RC oscillators automatically stop operation.
  2) There are three ways of releasing the HOLD mode.
     (1) Setting the reset pin to the low level.
     (2) System resetting by watchdog timer or low-voltage detection
     (3) Having an interrupt source established at either INT2 or INT4.

■ On-chip debugger

- Supports software debugging with the IC mounted on the target board.

■ Data security function

- Protects the program data stored in flash memory from unauthorized read or copy.
  Note : This data security function does not necessarily provide absolute data security.

■ Development tools

- On-chip debugger: TCB87 Type C + LC87F0K08A

■ Programming board

Package	Programming board
DIP24S	W87F0KD

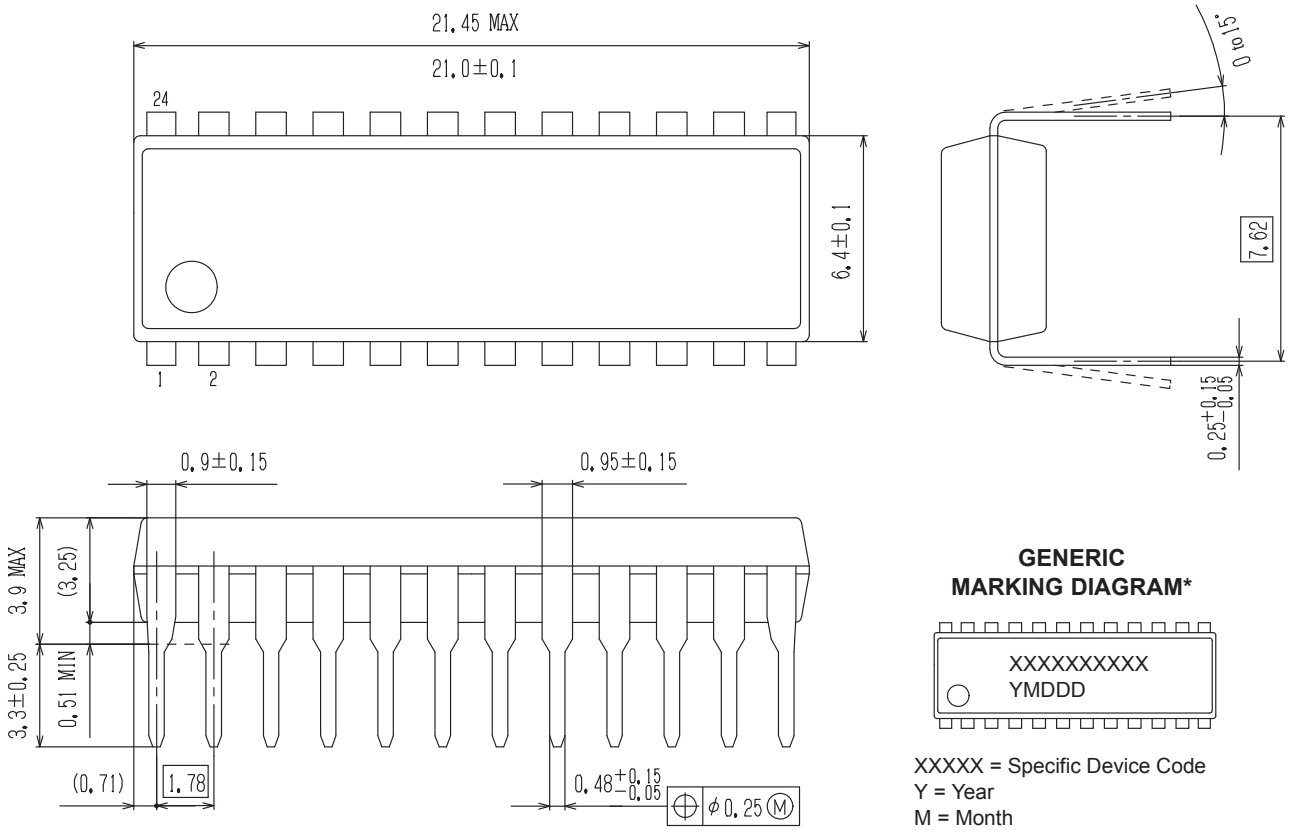
■ Flash ROM programmer

Maker		Model	Supported version	Device
ON Semiconductor	Single/Gang Programmer	SKK/SKK Type B (SanyoFWS)	Application version: 1.08 or later Chip data version: 2.44 or later	LC87F0K08
	Gang Programmer	SKK-4G (SanyoFWS)		

Note : Be sure to check for the latest version.

Package Dimensions
unit : mm

PDIP24 / DIP24S (300 mil)
CASE 646AW
ISSUE A

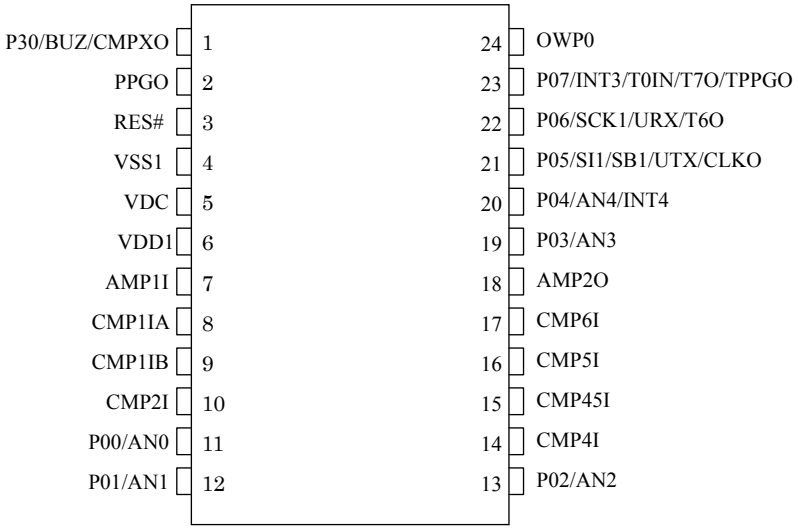


GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪ ”, may or may not be present.

Pin Assignment



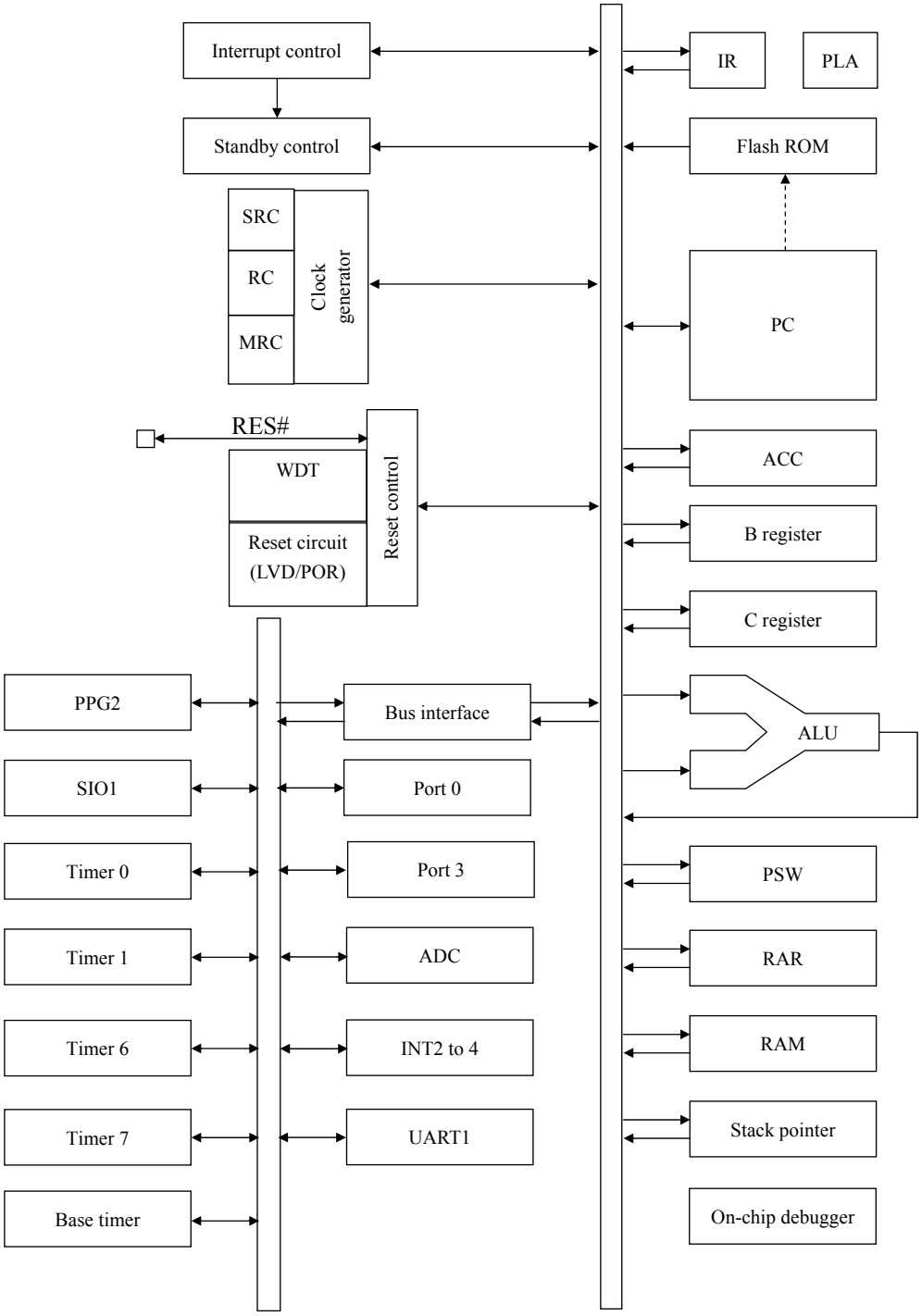
Top view

PDIP24/DIP24S (300mil)
"Pb-Free type"

DIP24S	NAME
1	P30/BUZ/CMPXO
2	PPGO
3	RES#
4	VSS1
5	VDC
6	VDD1
7	AMP1I
8	CMP1IA
9	CMP1IB
10	CMP2I
11	P00/AN0
12	P01/AN1

DIP24S	NAME
13	P02/AN2
14	CMP4I
15	CMP45I
16	CMP5I
17	CMP6I
18	AMP2O
19	P03/AN3
20	P04/AN4/INT4
21	P05/SI1/SB1/UTX/CLKO
22	P06/SCK11/URX/T6O
23	P07/INT3/T0IN/T7O/TPPGO
24	OWP0

System Block Diagram



Pin Function Chart

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>VSS1</td><td>–</td><td>– power supply pin</td><td>No</td></tr>
<tr><td>VDD1</td><td>–</td><td>+ power supply pin</td><td>No</td></tr>
<tr><td>Port 0
P00 to P07</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1 bit units
• Pull-up resistors can be turned on and off in 1 bit units.
• Pin functions
P04: INT4 input / HOLD release input / Timer 1 event input
/ Timer 0L capture input / Timer 0H capture input
P05: SIO1 data I/O / Bus I-O / UART transmit / System clock output
P06: SIO1 clock I/O / UART receive / Timer 6 toggle output
P07: INT3 input (with noise filter) / Timer 0 event input
Timer 0H capture input / Timer 7 toggle output
/ PPGO output (for monitor)
P00(AN0) to P04(AN4): AD convertor input port
Interrupt acknowledge type
<table><tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr><tr><td>INT3</td><td>○</td><td>○</td><td>○</td><td>X</td><td>X</td></tr><tr><td>INT4</td><td>○</td><td>○</td><td>○</td><td>X</td><td>X</td></tr></table></td><td>Yes</td></tr>
<tr><td>Port 3
P30</td><td>I/O</td><td>• 1-bit I/O port
• I/O specifiable in 1 bit units
• Pull-up resistors can be turned on and off in 1 bit units.
• Pin functions
P30: Buzzer output / Comparator output</td><td>Yes</td></tr>
<tr><td>AMP1I</td><td>I</td><td>AMP1 input pin</td><td>No</td></tr>
<tr><td>AMP2O</td><td>O</td><td>AMP2 output pin</td><td>No</td></tr>
<tr><td>CMP1IA</td><td>I</td><td>CMP1 (–) input pin</td><td>No</td></tr>
<tr><td>CMP1IB</td><td>I</td><td>CMP1 (+) input pin</td><td>No</td></tr>
<tr><td>CMP2I</td><td>I</td><td>CMP2 (+) , CMP7 (+) input pin</td><td>No</td></tr>
<tr><td>CMP4I</td><td>I</td><td>CMP4 (+) input pin</td><td>No</td></tr>
<tr><td>CMP45I</td><td>I</td><td>CMP4 (–), CMP5 (+) input pin</td><td>No</td></tr>
<tr><td>CMP5I</td><td>I</td><td>CMP5 (–) input pin</td><td>No</td></tr>
<tr><td>CMP6I</td><td>I</td><td>CMP6(+) input pin</td><td>No</td></tr>
<tr><td>PPGO</td><td>O</td><td>PPG output port</td><td>Yes</td></tr>
<tr><td>RES#</td><td>I/O</td><td>External reset Input / internal reset output pin</td><td>No</td></tr>
<tr><td>OWP0</td><td>I/O</td><td>Debugger-dedicated pin</td><td>No</td></tr>
<tr><td>VDC</td><td>O</td><td>Regulator output pin</td><td>No</td></tr>
</table>

Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

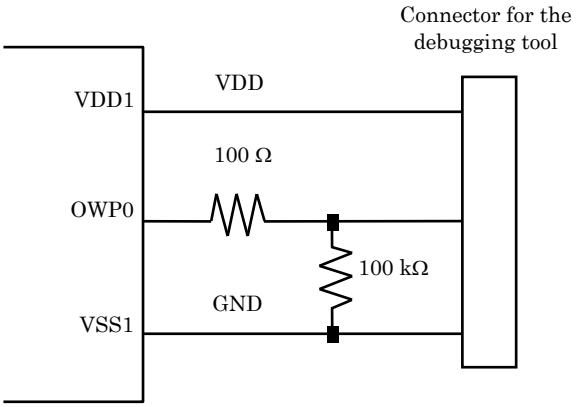
Port Name	Option Selected in Units of	Option Type	Output Type	Pull-up Resistor
P00 to P07	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
P30	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
PPGO	–	1	CMOS	No
		2	N-channel open drain	No

Recommended Unused Pin Connections

Port Name	Recommended Unused Pin Connections	
	Board	Software
P00 to P07	Open	Output low
P30	Open	Output low
AMP1I, CMP1AI, CMP1IB, CMP2I, CMP4I, CMP45I CMP5I, CMP6I	Pull down with a 100 kΩ resistor or less.	–
AMP2O	Open	–

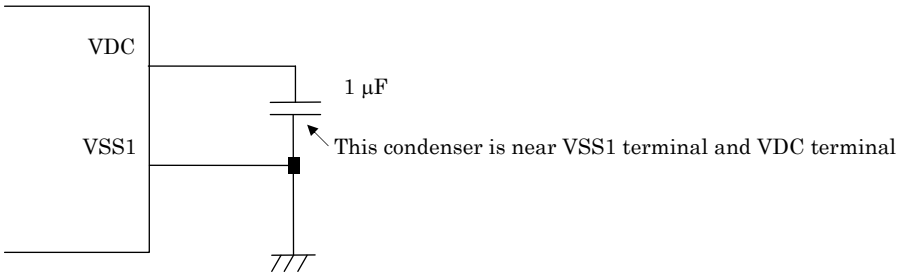
On-chip Debugger Pin Connection Requirements

Install and connect a limiting resistor (100 Ω) to the on-chip debugger dedicated pin (OWP0) on the user board and pull the pin down (100 kΩ). It is recommended to install a dedicated connector to accept the cable to the debugging tool (TCB87 Type C). The connector must accommodate three lines, i.e., VSS1, OWP0, and VDD1.



Regulator Output Pin Connection Requirements

The Regulator output pin (VDC) must be connected a condenser (1 μF) on the user's board.



1. Absolute Maximum Ratings at Ta = 25°C, VSS1 = 0 V

Parameter		Symbol	Pin / Remarks	Conditions		Specification			
					VDD [V]	min.	typ.	max.	unit
Maximum supply voltage		VDDMAX	VDD1			−0.3	−	+6.5	V
Input voltage		VI	RES#, AMP1I, CMP1IA, CMP1IB, CMP2I, CMP4I, CMP45I, CMP5I, CMP6I			−0.3	−	VDD+0.3	
Output voltage		VO	AMP2O, PPGO			−0.3	−	VDD+0.3	
Input/output voltage		VIO	Ports 0, 3 OWP0			−0.3	−	VDD+0.3	
High level output current	Peak output current	IOPH	Ports 0, 3, PPGO, OWP0	CMOS output select Per 1 applicable pin		−10			mA
	Mean output current (Note 1-1)	IOMH	Ports 0, 3, PPGO, OWP0	CMOS output select Per 1 applicable pin		−7.5			
	Total output current	ΣIOAH	Ports 0, 3, PPGO, OWP0	Total of all applicable pins		−25			
Low level output current	Peak output current	IOPL (1)	P02 to P07, Ports 3, PPGO, OWP0	Per 1 applicable pin				20	
		IOPL (2)	P00, P01	Per 1 applicable pin				30	
	Mean output current (Note 1-1)	IOML (1)	P02 to P07, Ports 3, PPGO, OWP0	Per 1 applicable pin				15	
		IOML (2)	P00, P01	Per 1 applicable pin				20	
	Total output current	ΣIOAL (1)	P00 to P03	Total of all applicable pins				40	
		ΣIOAL (2)	P04 to P07, Ports 3, PPGO, OWP0	Total of all applicable pins				40	
		ΣIOAL (3)	Ports 0, 3,PPGO, OWP0	Total of all applicable pins				70	
Allowable power dissipation		Pdmax	DIP24S	Ta = −40 to +85°C Mounted on thermal resistance test board (Note 1-2)				460	mW
Operating ambient temperature		Topr				−40	-	+85	°C
Storage ambient temperature		Tstg				−55	-	+125	

Note 1-1 : The mean output current is a mean value measured over 100 ms.

Note 1-2 : SEMI standards thermal resistance board (size: 76.1 ×114.3 ×1.6 t mm, glass epoxy) is used.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Allowable Operating Conditions at Ta = –40 to +85°C, VSS1 = 0 V

Parameter	Symbol	Pin / Remarks	Conditions	Specification				
				VDD [V]	min.	typ.	max.	unit
Operating supply voltage	VDD	VDD1	0.242 µs ≤ tCYC ≤ 200 µs		4.5		5.5	V
Memory sustaining supply voltage	VHD	VDD1	RAM and register contents sustained in HOLD mode.		2.0			
High level input voltage	VIH (1)	Ports 0, 3, OWP0		4.5 to 5.5	0.3VDD +0.7		VDD	
	VIH (2)	RES#		4.5 to 5.5	0.75VDD		VDD	
Low level input voltage	VIL (1)	Ports 3, OWP0		4.5 to 5.5	VSS		0.1VDD +0.4	
	VIL (2)	Port 0		4.5 to 5.5	VSS		0.15VDD +0.4	
	VIL (3)	RES#		4.5 to 5.5	VSS		0.25VDD	
Instruction cycle time (Note 2-1)	tCYC (Note 2-1)			4.5 to 5.5	0.242		200	µs
Oscillation frequency range	FmMRC		Internal high-speed RC oscillation. (Note 2-2)	4.5 to 5.5	23.28	24.0	24.72	MHz
	FmRC		Internal medium-speed RC oscillation	4.5 to 5.5	0.5	1.0	2.0	
	FmSRC2		Internal low-speed RC oscillation	4.5 to 5.5	15	30	60	kHz

Note 2-1 : Relationship between tCYC and oscillation frequency is 3/FmMRC at a division ratio of 1/1 and 6/FmMRC at a division ratio of 1/2.

Note 2-2 : When switching the system clock, allow an oscillation stabilization time of 100 µs or longer after the high-speed RC oscillator circuit transmits from the "oscillation stopped" to "oscillation enabled" state. The signal that divided high-speed RC oscillator clock by two is used for system clock (Typ. 12 MHz).

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Serial I/O Characteristics at Ta = –40 to +85°C, VSS1 = 0 V
(Note 4-1)

Parameter			Symbol	Pin / Remarks	Conditions	Specification				
						VDD [V]	min.	typ.	max.	unit
Serial clock	Input clock	Frequency	tSCK (1)	SCK1 (P06)	・See Fig. 2.	4.5 to 5.5	2			tCYC
		Low level pulse width	tSCKL (1)				1			
		High level pulse width	tSCKH (1)				1			
	Output clock	Frequency	tSCK (2)	SCK1 (P06)	・CMOS output selected ・See Fig. 2.	4.5 to 5.5	2			
		Low level pulse width	tSCKL (2)				1/2			tSCK
		High level pulse width	tSCKH (2)				1/2			
Serial input	Data setup time		tsDI	SB1 (P05)	・Must be specified with respect to rising edge of SIOCLK. ・See Fig. 2.	4.5 to 5.5	(1/3)tCYC +0.01			µs
	Data hold time		thDI				0.03			
Serial output	Output delay time		tdD0	SB1 (P05)	・Must be specified with respect to falling edge of SIOCLK. ・Must be specified as the time to the beginning of output state change in open drain output mode. ・See Fig. 2	4.5 to 5.5			(1/2)tCYC +0.05	

Note 4-1: These specifications are theoretical values. Be sure to add margin depending on its use.

5. Pulse Input Conditions at Ta = –40 to +85°C, VSS1 = 0 V

Parameter	Symbol	Pin / Remarks	Conditions	Specification				
				VDD [V]	min.	typ.	max.	unit
High/low level pulse width	tPIH (1) tPIL (1)	INT3 (P07) when no noise filter is used, INT4 (P04)	・Interrupt source flag can be set. ・Event inputs for timer 0 or 1 are enabled.	4.5 to 5.5	1			tCYC
	tPIH (2) tPIL (2)	INT3 (P07) when noise filter time constant is 1/1.	・Interrupt source flag can be set. ・Event inputs for timer 0 are enabled.	4.5 to 5.5	2			
	tPIH (3) tPIL (3)	INT3 (P07) when noise filter time constant is 1/32.	・Interrupt source flag can be set. ・Event inputs for timer 0 are enabled.	4.5 to 5.5	64			
	tPIH (4) tPIL (4)	INT3 (P07) when noise filter time constant is 1/128.	・Interrupt source flag can be set. ・Event inputs for timer 0 are enabled.	4.5 to 5.5	256			
	tPIL (5)	RES#	・Resetting is enabled.	4.5 to 5.5	200			µs

6. AD Converter Characteristics at VSS1 = 0 V

<12 bits AD Converter Mode at Ta = −40 to +85°C >

Parameter	Symbol	Pin / Remarks	Conditions	Specification				
				VDD [V]	min.	typ.	max.	unit
Resolution	N	AN0 (P00) to AN4 (P04)		4.5 to 5.5		12		bit
Absolute accuracy	ET		(Note 6-1)	4.5 to 5.5			±16	LSB
Conversion time	TCAD		• See conversion time calculation formulas. (Note 6-2)	4.5 to 5.5	32		115	µs
Analog input voltage range	VAIN			4.5 to 5.5	VSS		VDD	V
Analog port input current	IAINH		VAIN = VDD	4.5 to 5.5			1	µA
	IAINL		VAIN = VSS	4.5 to 5.5	−1			

<8 bits AD Converter Mode at Ta = −40 to +85°C >

Parameter	Symbol	Pin / Remarks	Conditions	Specification				
				VDD [V]	min.	typ.	max.	unit
Resolution	N	AN0 (P00) to AN4 (P04)		4.5 to 5.5		8		bit
Absolute accuracy	ET		(Note 6-1)	4.5 to 5.5			±1.5	LSB
Conversion time	TCAD		• See conversion time calculation formulas. (Note 6-2)	4.5 to 5.5	20		90	µs
Analog input voltage range	VAIN			4.5 to 5.5	VSS		VDD	V
Analog port input current	IAINH		VAIN = VDD	4.5 to 5.5			1	µA
	IAINL		VAIN = VSS	4.5 to 5.5	−1			

Conversion time calculation formulas :

12 bits AD Converter Mode: TCAD (Conversion time) = ((52 / (AD division ratio)) + 2) × (1/3) × tCYC

8 bits AD Converter Mode: TCAD (Conversion time) = ((32 / (AD division ratio)) + 2) × (1/3) × tCYC

<Recommended Operating Conditions>

Internal oscillation (FmMRC)	Operating supply voltage range (VDD)	System division ratio (SYSDIV)	Cycle time (tCYC)	AD division ratio (ADDIV)	AD conversion time (TCAD)	
					12-bit AD	8-bit AD
12 MHz	4.5 V to 5.5 V	1/1	250 ns	1/8	34.8 µs	21.5 µs

Note 6-1: The quantization error (±1/2LSB) must be excluded from the absolute accuracy. The absolute accuracy must be measured in the microcontroller's state in which no I/O operations occur at the pins adjacent to the analog input channel.

Note 6-2: The conversion time refers to the period from the time an instruction for starting a conversion process till the time the conversion results register(s) are loaded with a complete digital conversion value corresponding to the analog input value.

The conversion time is 2 times the normal-time conversion time when :

- The first AD conversion is performed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion is performed after the AD conversion mode is switched from 8-bit to 12-bit conversion mode.

7. Power-on Reset (POR) Characteristics at Ta = –40 to +85°C, VSS1 = 0 V

Parameter	Symbol	Pin / Remarks	Conditions	Option selected voltage	Specification min.	typ.	max.	unit
POR release voltage	PORRL		・Select from options. (Note 7-1)	2.37 V	2.25	2.37	2.49	V
				2.57 V	2.45	2.57	2.69	
				2.87 V	2.73	2.85	2.97	
				3.86 V	3.69	3.84	3.99	
				4.35 V	4.15	4.33	4.50	
Detection voltage unknown state	POUKS		・See Fig. 4. (Note 7-2)			0.7	0.95	
Power supply rise time	PORIS		・Power supply rise time from VDD = 0 V to 1.6 V.				100	ms

Note7-1 : The POR release level can be selected out of 5 levels when the LVD reset function is disabled.

Note7-2 : POR is in an unknown state before transistors start operation.

8. Low Voltage Detection Reset (LVD) Characteristics at Ta = –40 to +85°C, VSS1 = 0 V

Parameter	Symbol	Pin / Remarks	Conditions	Option selected voltage	Specification min.	typ.	max.	unit
LVD reset voltage (Note 8-2)	LVDET		Select from options. See Fig. 5. (Note 8-1) (Note 8-3)	2.31 V	2.21	2.31	2.41	V
				2.51 V	2.41	2.51	2.61	
				2.81 V	2.66	2.81	2.96	
				3.79 V	3.61	3.79	3.97	
				4.28 V	4.10	4.28	4.46	
LVD detection voltage hysteresis	LVHYS			2.31 V		50		mV
				2.51 V		50		
				2.81 V		50		
				3.79 V		50		
				4.28 V		50		
Detection voltage unknown state	LVUKS		See Fig. 5. (Note 8-4)			0.7	0.95	V
Low voltage detection minimum width (Reply sensitivity)	TLVDW		LVDET–0.5 V See Fig. 6.		0.2			ms

Note8-1 : The LVD reset level can be selected out of 5 levels when the LVD reset function is enabled.

Note8-2 : LVD reset voltage specification values do not include hysteresis voltage.

Note8-3 : LVD reset voltage may exceed its specification values when port output state changes and/or when a large current flows through port.

Note8-4 : LVD is in an unknown state before transistors start operation.

9. Amplifier and Comparator Characteristics at Ta = −40 to +85°C, VSS1 = 0 V

Parameter	Symbol	Pin / Remarks	Conditions		Specification			
				VDD [V]	min.	typ.	max.	unit
Common-mode input voltage (Note 9-1)	VCMIN	CMP1IA,CMP1IB, CMP2I, CMP4I, CMP45I, CMP5I, CMP6I		4.5 to 5.5	VSS		VDD −1.5 V	V
Internal reference voltage error	VREF	CMP2, CMP3, CMP6, CMP7, CMP8		4.5 to 5.5	−0.02		+0.02	
AMP input voltage range (Note 9-2)	VAMIN	AMP1I		4.5 to 5.5	VSS		(VDD −1.5 V) /AMP gain	
Offset voltage	VOFF(1)	CMP1IA, CMP1IB (CMP1) CMP4I, CMP45I (CMP4) CMP45I, CMP5I (CMP5)	・Within common-mode input voltage range	4.5 to 5.5			±20	mV
	VOFF(2)	CMP2I (CMP2,CMP7), CMP6I (CMP6)	・Within common-mode input voltage range ・Including VREF error	4.5 to 5.5			±40	
	VOFF(3)	AMP1I (CMP3,CMP8)	・Within AMP Input voltage range ・AMP1 gain set at 8x ・Including AMP1 output error and VREF error	4.5 to 5.5			±28	
AMP output error	VAER(1)	AMP2O	・AMP1I = 0.41 V ・AMP1 gain set at 8x ・AMP2 gain set at 1x			±155	±180	
CMP1/CMP4/ CMP5 response time	tC145RT	PPGO, CMPXO(P30)	・Within common-mode input voltage range ・Input amplitude = 100 mV ・Over drive = 50 mV	4.5 to 5.5		200		ns
CMP3/CMP8 response time	tC38RT	PPGO, CMPXO(P30)	・AMP1 gain set at 8x ・AMP1I rising time ・MP1I = (VREF ±100 mV) / 8 ・See Fig. 7.	4.5 to 5.5		600		
CMP2 response time	tC2RT	CMPXO(P30)	・CMP input pin rising time ・CMP input = VREF ±50 mV	4.5 to 5.5		200		
CMP6/CMP7 response time	tC67RT	PPGO, CMPXO(P30)	・CMP input pin rising time ・CMP input = VREF ±50 mV ・See Fig. 7.	4.5 to 5.5		200		

Note 9-1 : When VDD = 5 V, the comparator input voltage is effective from 0 to 3.5 V.

Note 9-2 : AMP gain = AMP1 gain × AMP2 gain

When VDD = 5 V, AMP1 gain = 8x, AMP2 gain = 1x, the AMP input voltage is effective from 0 to 0.4375 V.

Note 9-3 : PPG output for CMP1 has a delay of 1/6 tCYC to 1/2 tCYC from CMPXO falling timing for synchronization with system clock, when the pulse start delay setup register is set to 000H.

11. F-ROM Programming Characteristics at Ta = +10 to +55°C, VSS1 = 0 V

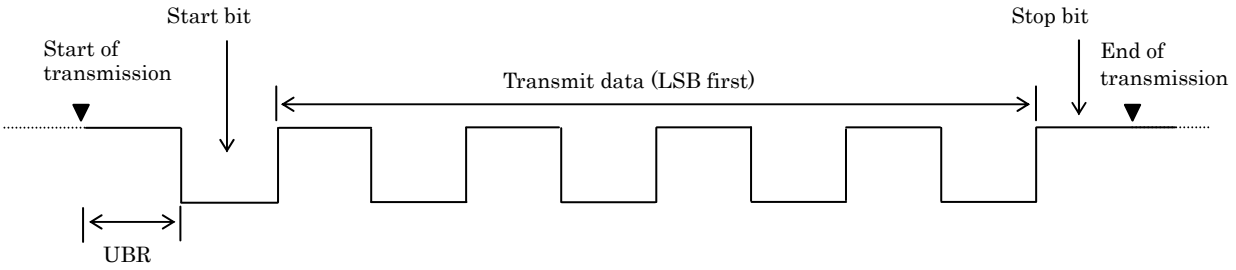
Parameter	Symbol	Pin / Remarks	Conditions	VDD [V]	Specification min.	typ.	max.	unit
Onboard programming current	IDDFW	VDD1	· Excluding current consumption of the microcontroller block	4.5 to 5.5		7	11	mA
Programming time	tFW (1)		· Erasing operation	4.5 to 5.5		12	15	ms
	tFW (2)		· Programming operation			35	45	µs

12. UART (Full Duplex) Operating Conditions at Ta = −40 to +85°C, VSS1 = 0 V

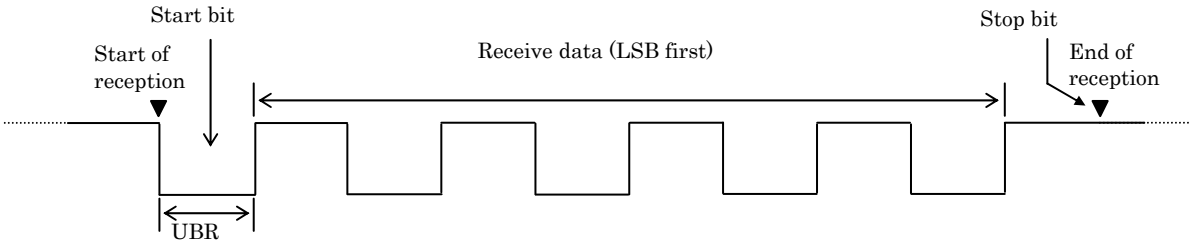
Parameter	Symbol	Pin / Remarks	Conditions	VDD [V]	Specification min.	typ.	max.	unit
Transfer rate	UBR	UTX (P05) URX (P06)		4.5 to 5.5	16/3		8192/3	tCYC

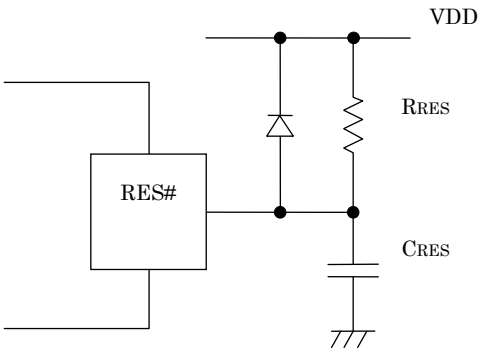
Data length : 7 / 8 / 9 bits (LSB first)
Stop bits : 1 bit (2-bit in continuous data transmission)
Parity bits : None

Example of Continuous 8-bit Data Transmission Mode Processing (First Transmit Data = 55H)



Example of Continuous 8-bit Data Reception Mode Processing (First Receive Data = 55H)





Note :
External circuits for reset may vary depending on the usage of POR and LVD. Please refer to the reset function in the user's manual for more information.

Figure 1 Sample Reset Circuit

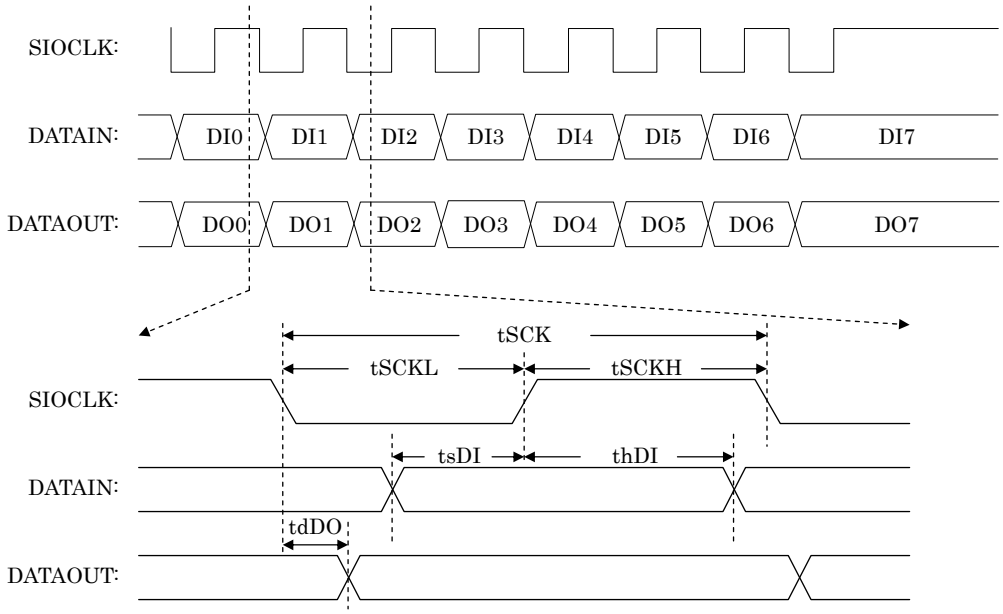


Figure 2 Serial I/O Waveforms

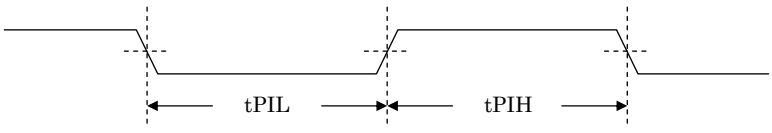
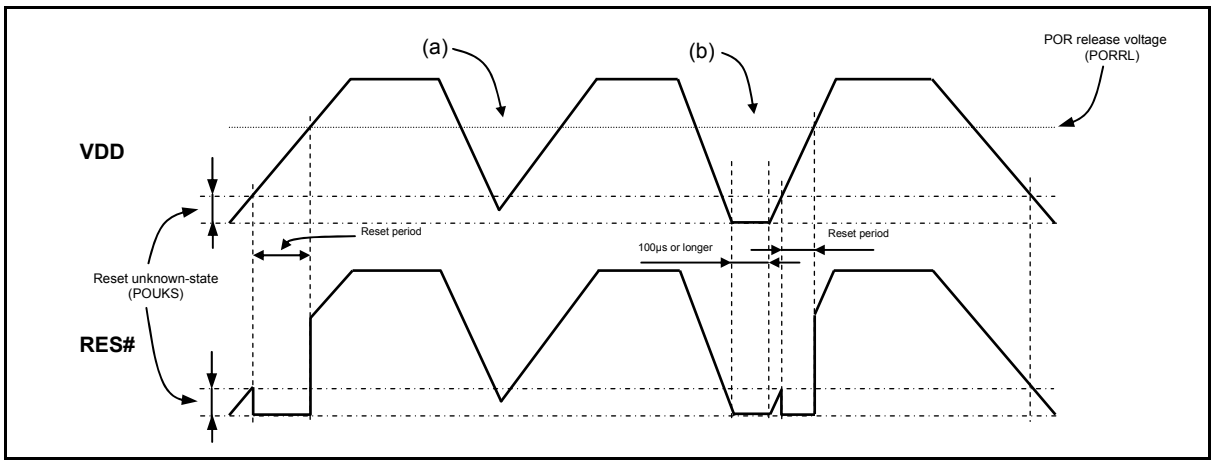


Figure 3 Pulse Input Timing Signal Waveform

Figure 4 Example of waveforms observed when only POR is used (LVD not used) (RESET pin : Pull-up resistor R_{RES} only)

- The POR function generates a reset only when power is turned on starting at the VSS level.
- No stable reset will be generated if power is turned on again when the power level does not go down to the VSS level as shown in (a). If such a case is anticipated, use the LVD function together with the POR function or implement an external reset circuit.
- A reset is generated only when the power level goes down to the VSS level as shown in (b) and power is turned on again after this condition continues for 100μs or longer.



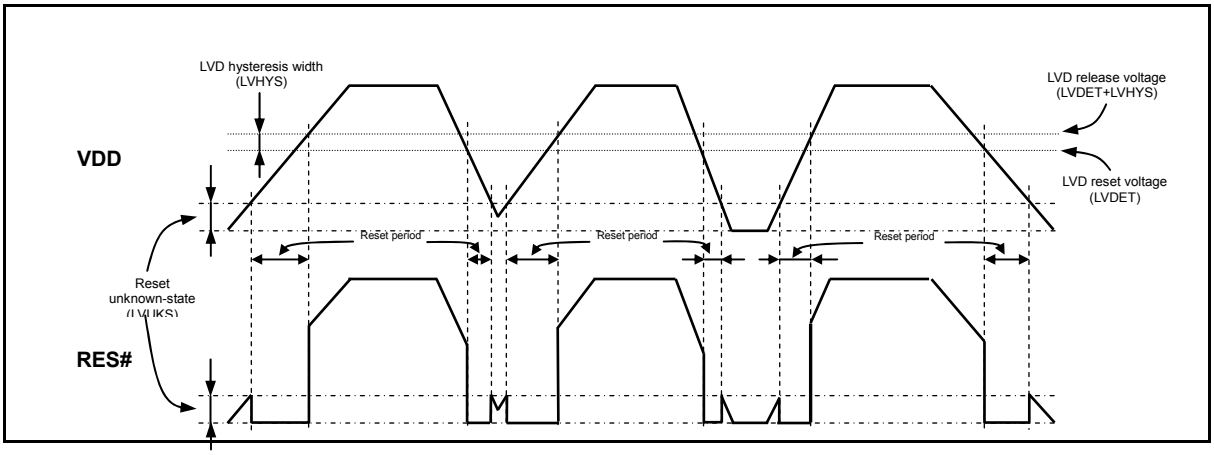


Figure 5 Example of waveforms observed when both POR and LVD functions are used (RESET pin: Pull-up resistor R_{RES} only)

- Resets are generated both when power is turned on and when the power level lowers.
- A hysteresis width (LVHYS) is provided to prevent the repetitions of reset release and entry cycles near the detection level.

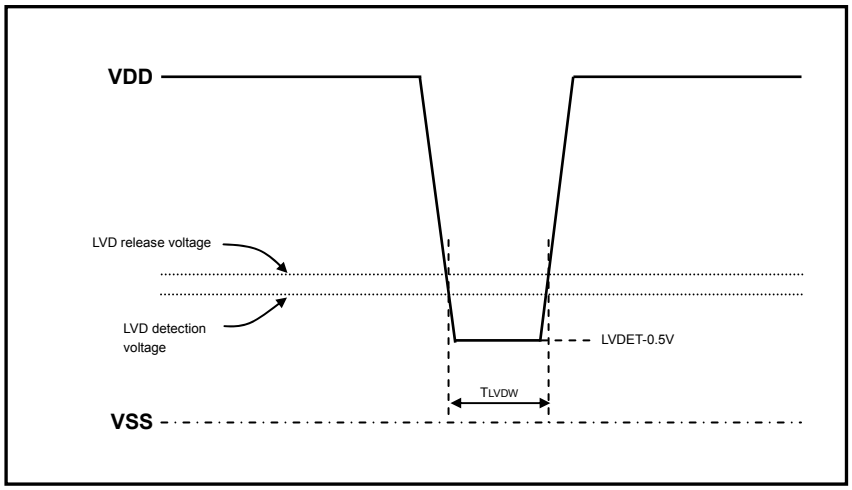


Figure 6 Low voltage detection minimum width (Example of momentary power loss / Voltage variation waveform)

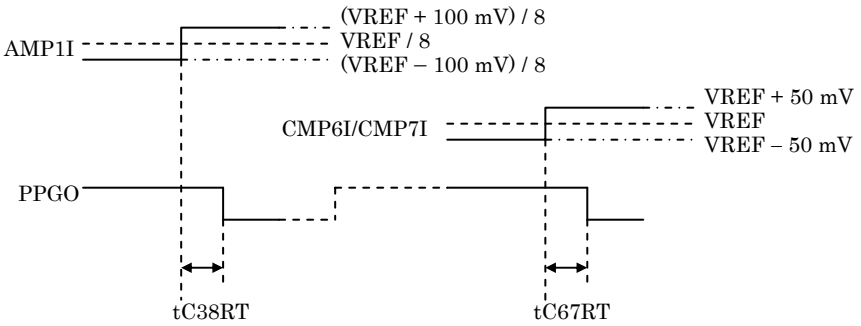


Figure 7 CMP response time

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC87F0K08AUDA-E	DIP24S(300mil) (Pb-Free)	1100 / Fan-Fold