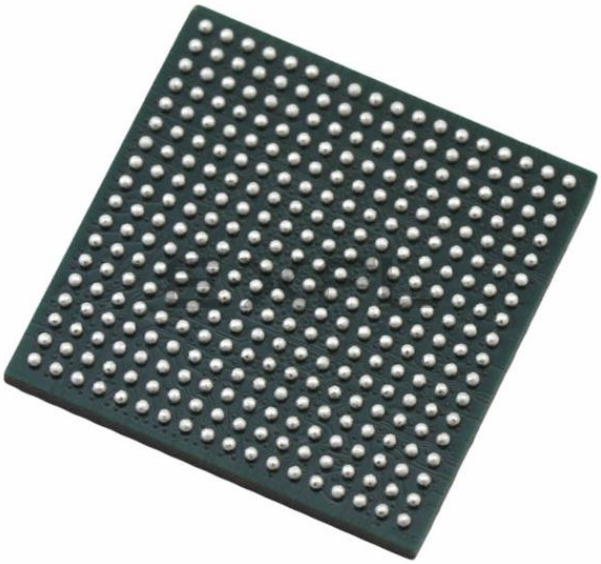

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	DAI, DPI, EBI/EMI, I²C, SCI, SPI, SSP, UART/USART
Clock Rate	400MHz
Non-Volatile Memory	External
On-Chip RAM	5Mbit
Voltage - I/O	3.30V
Voltage - Core	1.05V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	324-BGA, CSPBGA
Supplier Device Package	324-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ad21469wbbcz302

Note that the external memory bank addresses shown are for normal-word (32-bit) accesses. If 48-bit instructions, as well as 32-bit data, are both placed in the same external memory bank, care must be taken while mapping them to avoid overlap.

Asynchronous Memory Controller

The asynchronous memory controller provides a configurable interface for up to four separate banks of memory or I/O devices. Each bank can be independently programmed with different timing parameters, enabling connection to a wide variety of memory devices including SRAM, Flash, and EPROM, as well as I/O devices that interface with standard memory control lines. Bank 0 occupies a 2M word window and banks 1, 2, and 3 occupy a 4M word window in the processor's address space but, if not fully populated, these windows are not made contiguous by the memory controller logic.

External Port Throughput

The throughput for the external port, based on a 400 MHz clock, is 66M bytes/s for the AMI and 800M bytes/s for DDR2.

Link Ports

Two 8-bit wide link ports can connect to the link ports of other DSPs or peripherals. Link ports are bidirectional ports having eight data lines, an acknowledge line, and a clock line. Link ports can operate at a maximum frequency of 166 MHz.

MediaLB

The automotive model has a MLB interface which allows the processors to function as a media local bus device. It includes support for both 3-pin and 5-pin media local bus protocols. It supports speeds up to 1024 FS (49.25M bits/sec, FS = 48.1 kHz) and up to 31 logical channels, with up to 124 bytes of data per media local bus frame.

The MLB interface supports MOST25 and MOST50 data rates. The isochronous mode of transfer is not supported.

Pulse-Width Modulation

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine control or audio power control. The PWM generator can generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate complementary signals on two outputs in paired mode or independent signals in non-paired mode (applicable to a single group of four PWM waveforms). The PWM generator is capable of operating in two distinct modes while generating center-aligned PWM waveforms: single update mode or double update mode.

The entire PWM module has four groups of four PWM outputs each. Therefore, this module generates 16 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM outputs.

Digital Applications Interface (DAI)

The digital applications interface (DAI) provides the ability to connect various peripherals to any of the DAI pins (DAI_P20–1).

Programs make these connections using the signal routing unit (SRU), shown in Figure 1 on Page 1.

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the DAI associated peripherals for a much wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

The DAI includes the peripherals described in the following sections.

Serial Ports

The processors feature eight synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices' AD183x family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial ports can support up to 16 transmit or 16 receive DMA channels of audio data when all eight SPORTs are enabled, or four full duplex TDM streams of 128 channels per frame.

The serial ports operate at a maximum data rate of $f_{PCLK}/4$. Serial port data can be automatically transferred to and from on-chip memory/external memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in five modes:

- Standard DSP serial mode
- Multichannel (TDM) mode
- I^2S mode
- Packed I^2S mode
- Left-justified mode

S/PDIF-Compatible Digital Audio Receiver/Transmitter

The S/PDIF receiver/transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a biphase encoded signal. The serial data input to the receiver/transmitter can be formatted as left justified, I^2S or right justified with word widths of 16, 18, 20, or 24 bits.

The serial data, clock, and frame sync inputs to the S/PDIF receiver/transmitter are routed through the signal routing unit (SRU). They can come from a variety of sources, such as the SPORTs, external pins, and the precision clock generators (PCGs), and are controlled by the SRU control registers.

Asynchronous Sample Rate Converter

The asynchronous sample rate converter (ASRC) contains four ASRC blocks, is the same core as that used in the AD1896 192 kHz stereo asynchronous sample rate converter, and provides up to 128 dB SNR. The ASRC block is used to perform synchronous or asynchronous sample rate conversion across independent stereo channels, without using internal processor resources. The four SRC blocks can also be configured to operate together to convert multichannel audio data without phase mismatches. Finally, the ASRC can be used to clean up audio data from jittery clock sources such as the S/PDIF receiver.

Input Data Port

The IDP provides up to eight serial input channels—each with its own clock, frame sync, and data inputs. The eight channels are automatically multiplexed into a single 32-bit by eight-deep FIFO. Data is always formatted as a 64-bit frame and divided into two 32-bit words. The serial protocol is designed to receive audio channels in I^2S, left-justified sample pair, or right-justified mode. One frame sync cycle indicates one 64-bit left/right pair, but data is sent to the FIFO as 32-bit words (that is, one-half of a frame at a time). The processors support 24- and 32-bit I^2S, 24- and 32-bit left-justified, and 24-, 20-, 18- and 16-bit right-justified formats.

Precision Clock Generators

The precision clock generators (PCG) consist of four units—A, B, C, and D, each of which generates a pair of signals (clock and frame sync) derived from a clock input signal. The units are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

Digital Peripheral Interface (DPI)

The digital peripheral interface provides connections to two serial peripheral interface (SPI) ports, one universal asynchronous receiver-transmitter (UART), 12 flags, a 2-wire interface (TWI), and two general-purpose timers. The DPI includes the peripherals described in the following sections.

Serial Peripheral Interface

The processors contain two serial peripheral interface ports (SPI). The SPI is an industry-standard synchronous serial link, enabling the SPI-compatible port to communicate with other SPI compatible devices. The SPI consists of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multimaster environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device. The SPI-compatible peripheral implementation also features programmable baud rate, clock phase, and polarities. The SPI-compatible port uses open-drain drivers to support a multimaster configuration and to avoid data contention.

UART Port

The processors provide a full-duplex Universal Asynchronous Receiver/Transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART also has multiprocessor communication capability using 9-bit address detection. This allows it to be used in multidrop networks through the RS-485 data interface standard. The UART port also includes support for 5 to 8 data bits, 1 or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O) – The processors send or receive data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory.

Timers

The processors have a total of three timers: a core timer that can generate periodic software interrupts and two general-purpose timers that can generate periodic interrupts and be independently set to operate in one of three modes:

- Pulse waveform generation mode
- Pulse width count/capture mode
- External event watchdog mode

The core timer can be configured to use FLAG3 as a timer expired signal, and each general-purpose timer has one bidirectional pin and four registers that implement its mode of operation. A single control and status register enables or disables both general-purpose timers independently.

2-Wire Interface Port (TWI)

The TWI is a bidirectional, 2-wire serial bus used to move 8-bit data while maintaining compliance with the I^2C bus protocol. The TWI master incorporates the following features:

- 7-bit addressing
- Simultaneous master and slave operation on multiple device systems with support for multi master data arbitration
- Digital filtering and timed event processing
- 100 kbps and 400 kbps data rates
- Low interrupt rate

I/O Processor Features

Automotive versions of the I/O processor provide 67 channels of DMA, while standard versions provide 36 channels of DMA, as well as an extensive set of peripherals that are described in the following sections.

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21467/ADSP-21469 architecture and functionality. For detailed information on the core architecture and instruction set, refer to the *SHARC Processor Programming Reference*.

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in Wikipedia or the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (http://www.analog.com/signal chains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

Table 10. Pin Descriptions (Continued)

Name	Type	State During/ After Reset	Description
$DDR2\_ADDR_{15-0}$	O/T	High-Z/ driven low	**DDR2 Address.** DDR2 address pins.
$DDR2\_BA_{2-0}$	O/T	High-Z/ driven low	**DDR2 Bank Address Input.** Defines which internal bank an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied to. BA_{2-0}define which mode registers, including MR, EMR, EMR(2), and EMR(3) are loaded during the LOAD MODE REGISTER command.
$\overline{DDR2\_CAS}$	O/T	High-Z/ driven high	**DDR2 Column Address Strobe.** Connect to $\overline{DDR2\_CAS}$ pin; in conjunction with other DDR2 command pins, defines the operation for the DDR2 to perform.
DDR2_CKE	O/T	High-Z/ driven low	**DDR2 Clock Enable Output to DDR2.** Active high signal. Connect to DDR2 CKE signal.
$\overline{DDR2\_CS_{3-0}}$	O/T	High-Z/ driven high	**DDR2 Chip Select.** All commands are masked when $\overline{DDR2\_CS_{3-0}}$ is driven high. $\overline{DDR2\_CS_{3-0}}$ are decoded memory address lines. Each $\overline{DDR2\_CS_{3-0}}$ line selects the corresponding external bank.
$DDR2\_DATA_{15-0}$	I/O/T	High-Z	**DDR2 Data In/Out.** Connect to corresponding DDR2_DATA pins.
$DDR2\_DM_{1-0}$	O/T	High-Z/ driven high	**DDR2 Input Data Mask.** Mask for the DDR2 write data if driven high. Sampled on both edges of DDR2_DQS at DDR2 side. DM0 corresponds to DDR2_DATA 7–0 and DM1 corresponds to DDR2_DATA15–8.
$DDR2\_DQS_{1-0}$ $\overline{DDR2\_DQS_{1-0}}$	I/O/T (Differential)	High-Z	**Data Strobe.** Output with Write Data. Input with Read Data. DQS0 corresponds to DDR2_DATA 7–0 and DQS1 corresponds to DDR2_DATA 15–8. Based on software control via the DDR2CTL3 register, this pin can be single-ended or differential.
$\overline{DDR2\_RAS}$	O/T	High-Z/ driven high	**DDR2 Row Address Strobe.** Connect to $\overline{DDR2\_RAS}$ pin; in conjunction with other DDR2 command pins, defines the operation for the DDR2 to perform.
$\overline{DDR2\_WE}$	O/T	High-Z/ driven high	**DDR2 Write Enable.** Connect to $\overline{DDR2\_WE}$ pin; in conjunction with other DDR2 command pins, defines the operation for the DDR2 to perform.
DDR2_CLK0, $\overline{DDR2\_CLK0}$, DDR2_CLK1, $\overline{DDR2\_CLK1}$	O/T (Differential)	High-Z/ driven low	**DDR2 Memory Clocks.** Two differential outputs available via software control (DDR2CTL0 register). Free running, minimum frequency not guaranteed during reset.
DDR2_ODT	O/T	High-Z/ driven low	**DDR2 On Die Termination.** ODT pin when driven high (along with other requirements) enables the DDR2 termination resistances. ODT is enabled/disabled regardless of read or write commands.

The following symbols appear in the Type column of Table 10: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open-drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26 kΩ–63 kΩ. The range of an ipd resistor can be between 31 kΩ–85 kΩ. The three-state voltage of ipu pads will not reach to full the V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.
In this table, the DDR2 pins are SSTL18 compliant. All other pins are LVTTL compliant.

ELECTRICAL CHARACTERISTICS

Parameter[1]	Description	Test Conditions	450 MHz Min	450 MHz Max	400 MHz Min	400 MHz Max	Unit
V_{OH}[2]	High Level Output Voltage	@ V_{DD_EXT} = Min, I_{OH} = –1.0 mA[3]	2.4		2.4		V
V_{OL}[2]	Low Level Output Voltage	@ V_{DD_EXT} = Min, I_{OL} = 1.0 mA[3]		0.4		0.4	V
V_{OH_DDR2}	High Level Output Voltage for DDR2	@ V_{DD_DDR} = Min, I_{OH} = –13.4 mA	1.4		1.4		V
V_{OL_DDR2}	Low Level Output Voltage for DDR2	@ V_{DD_DDR} = Min, IOL = 13.4 mA		0.29		0.29	V
I_{IH}[4, 5]	High Level Input Current	@ V_{DD_EXT} = Max, V_{IN} = V_{DD_EXT} Max		10		10	µA
I_{IL}[4, 6]	Low Level Input Current	@ V_{DD_EXT} = Max, V_{IN} = 0 V		10		10	µA
I_{ILPU}[5]	Low Level Input Current Pull-up	@ V_{DD_EXT} = Max, V_{IN} = 0 V		200		200	µA
I_{IHPD}[6]	High Level Input Current Pull-down	@ V_{DD_EXT} = Max, V_{IN} = V_{DD_EXT} Max		200		200	µA
I_{OZH}[7, 8]	Three-State Leakage Current	@ V_{DD_EXT}/V_{DD_DDR} = Max, V_{IN} = V_{DD_EXT}/V_{DD_DDR} Max		10		10	µA
I_{OZL}[7, 9]	Three-State Leakage Current	@ V_{DD_EXT}/V_{DD_DDR} = Max, V_{IN} = 0 V		10		10	µA
I_{OZLPU}[8]	Three-State Leakage Current Pull-up	@ V_{DD_EXT} = Max, V_{IN} = 0 V		200		200	µA
I_{OZHPD}[9]	Three-State Leakage Current Pull-down	@ V_{DD_EXT} = Max, V_{IN} = V_{DD_EXT} Max		200		200	µA
I_{DD_INT}[10]	Supply Current (Internal)	f_{CCLK} > 0 MHz		Table 13 + Table 14 × ASF		Table 13 + Table 14 × ASF	mA
I_{DD_A}[11]	Supply Current (Analog)	V_{DD_A} = Max		10		10	mA
C_{IN}[12, 13]	Input Capacitance	T_{CASE} = 25°C		5		5	pF

[1] Specifications subject to change without notice.
[2] Applies to output and bidirectional pins: AMI_ADDR23-0, AMI_DATA7-0, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, FLAG3–0, DAI_Px, DPI_Px, $\overline{\text{EMU}}$, TDO.
[3] See Output Drive Currents on Page 62 for typical drive current capabilities.
[4] Applies to input pins: BOOTCFGx, CLKCFGx, TCK, $\overline{\text{RESET}}$, CLKIN.
[5] Applies to input pins with internal pull-ups: $\overline{\text{TRST}}$, TMS, TDI.
[6] Applies to input pins with internal pull-downs: MLBCLK
[7] Applies to three-statable pins: all DDR2 pins.
[8] Applies to three-statable pins with pull-ups: DAI_Px, DPI_Px, $\overline{\text{EMU}}$.
[9] Applies to three-statable pins with pull-downs: MLBDAT, MLBSIG, MLBDO, MLBSO, LDAT07-0, LDAT17-0, LCLK0, LCLK1, LACK0, LACK1.
[10] See Engineer-to-Engineer Note EE-348 “Estimating Power Dissipation for ADSP-214xx SHARC Processors” for further information.
[11] Characterized but not tested.
[12] Applies to all signal pins.
[13] Guaranteed, but not tested.

Table 14. Dynamic Current in CCLK Domain—$I_{DD\_INT\_DYNAMIC}$ (mA, with ASF = 1.0)[1]

f_{CCLK} (MHz)[2]	V_{DD_INT}(V)[2]				
	0.95 V	**1.0 V**	**1.05 V**	**1.10 V**	**1.15 V**
100	78	82	86	91	98
150	115	121	130	136	142
200	150	159	169	177	188
250	186	197	208	219	231
300	222	236	249	261	276
350	259	275	288	304	319
400	293	309	328	344	361
450	N/A	N/A	366	385	406

[1] The values are not guaranteed as standalone maximum specifications. They must be combined with static current per the equations of Electrical Characteristics on Page 20.
[2] Valid frequency and voltage ranges are model-specific. See Operating Conditions on Page 19.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 15 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 15. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DD_INT})	–0.3 V to +1.32 V
Analog (PLL) Supply Voltage (V_{DD_A})	–0.3 V to +1.15 V
External (I/O) Supply Voltage (V_{DD_EXT})	–0.3 V to +3.6 V
Thermal Diode Supply Voltage (V_{DD_THD})	–0.3 V to +3.6 V
DDR2 Controller Supply Voltage (V_{DD_DDR2})	–0.3 V to +1.9 V
DDR2 Input Voltage	–0.3 V to +1.9 V
Input Voltage	–0.3 V to +3.6 V
Output Voltage Swing	–0.3 V to V_{DD_EXT} +0.5 V
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased	125°C

PACKAGE INFORMATION

The information presented in Figure 4 and Table 16 provides details about the package branding for the processor. For a complete listing of product availability, see Ordering Guide on Page 74.

Figure 4. Typical Package Brand

Table 16. Package Brand Information[1]

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Option
cc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

[1] Non-automotive only. For branding information specific to automotive products, contact Analog Devices, Inc.

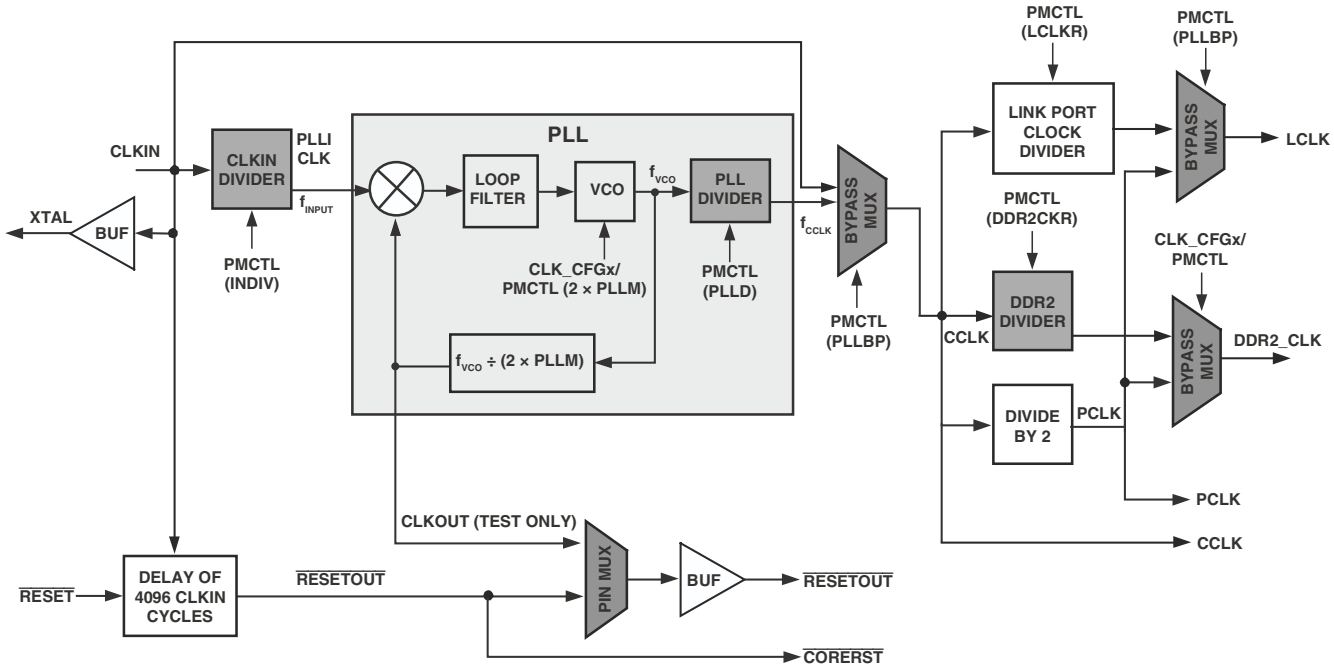

Figure 5. Core Clock and System Clock Relationship to CLKIN

Reset

Table 20. Reset

Parameter		Min	Max	Unit
Timing Requirements				
t_{WRST}[1]	$\overline{\text{RESET}}$ Pulse Width Low	$4 \times t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN Low	8		ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).

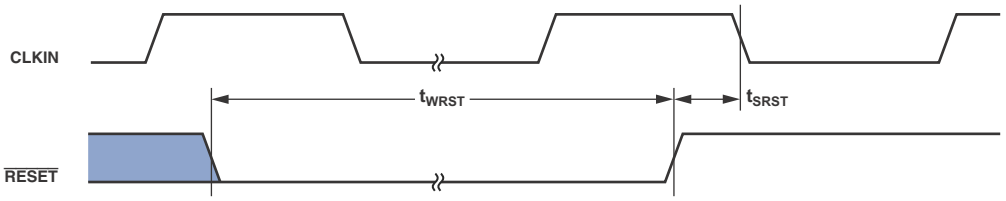

Figure 9. Reset

Running Reset

The following timing specification applies to $\overline{\text{RESETOUT}}$/$\overline{\text{RUNRSTIN}}$ pin when it is configured as $\overline{\text{RUNRSTIN}}$.

Table 21. Running Reset

Parameter		Min	Max	Unit
Timing Requirements				
$t_{WRUNRST}$	Running $\overline{\text{RESET}}$ Pulse Width Low	$4 \times t_{CK}$		ns
$t_{SRUNRST}$	Running $\overline{\text{RESET}}$ Setup Before CLKIN High	8		ns

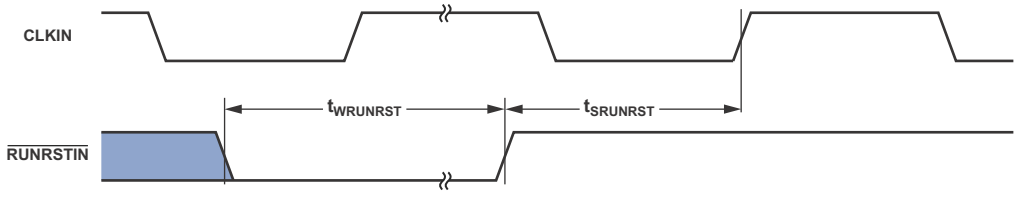

Figure 10. Running Reset

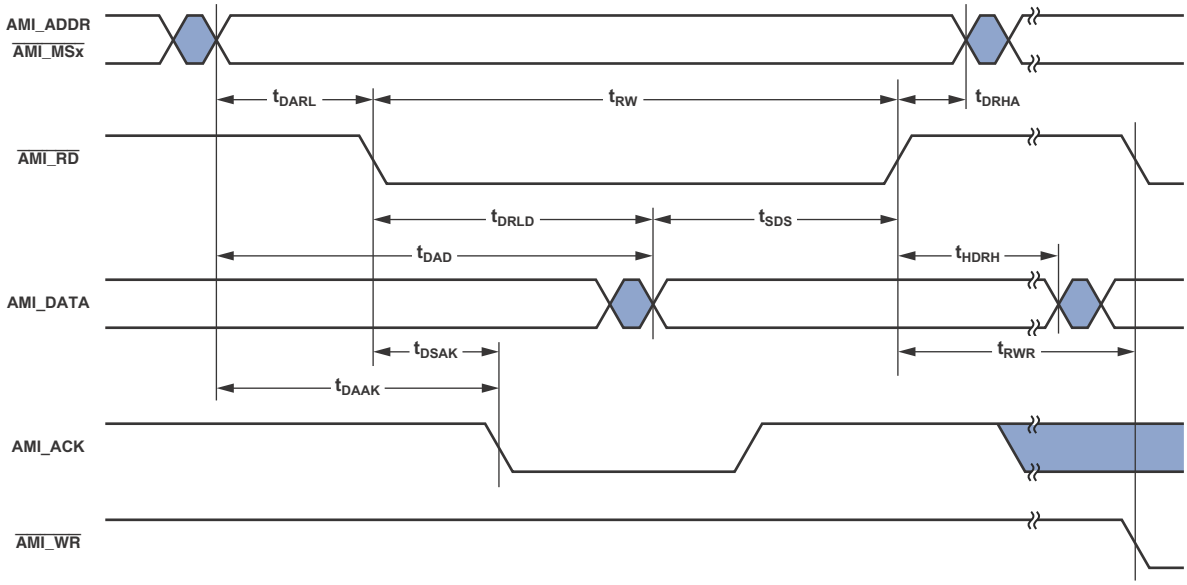

Figure 20. AMI Read

Shared Memory Bus Request

Use these specifications for passing bus mastership between processors ($\overline{BRx}$).

Table 33. Shared Memory Bus Request

Parameter		Min	Max	Unit
Timing Requirements				
t_{SBRI}	$\overline{BRx}$, Setup Before CLKIN High	$2 \times t_{PCLK} + 4$		ns
t_{HBRI}	$\overline{BRx}$, Hold After CLKIN High	5		ns
Switching Characteristics				
t_{DBRO}	$\overline{BRx}$ Delay After CLKIN High		20	ns
t_{HBRO}	$\overline{BRx}$ Hold After CLKIN High	$1 - t_{PCLK}$		ns

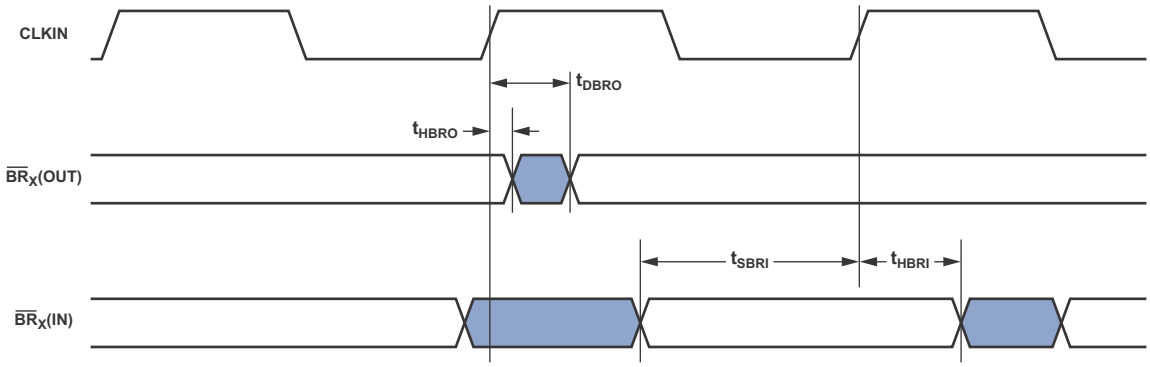

Figure 22. Shared Memory Bus Request

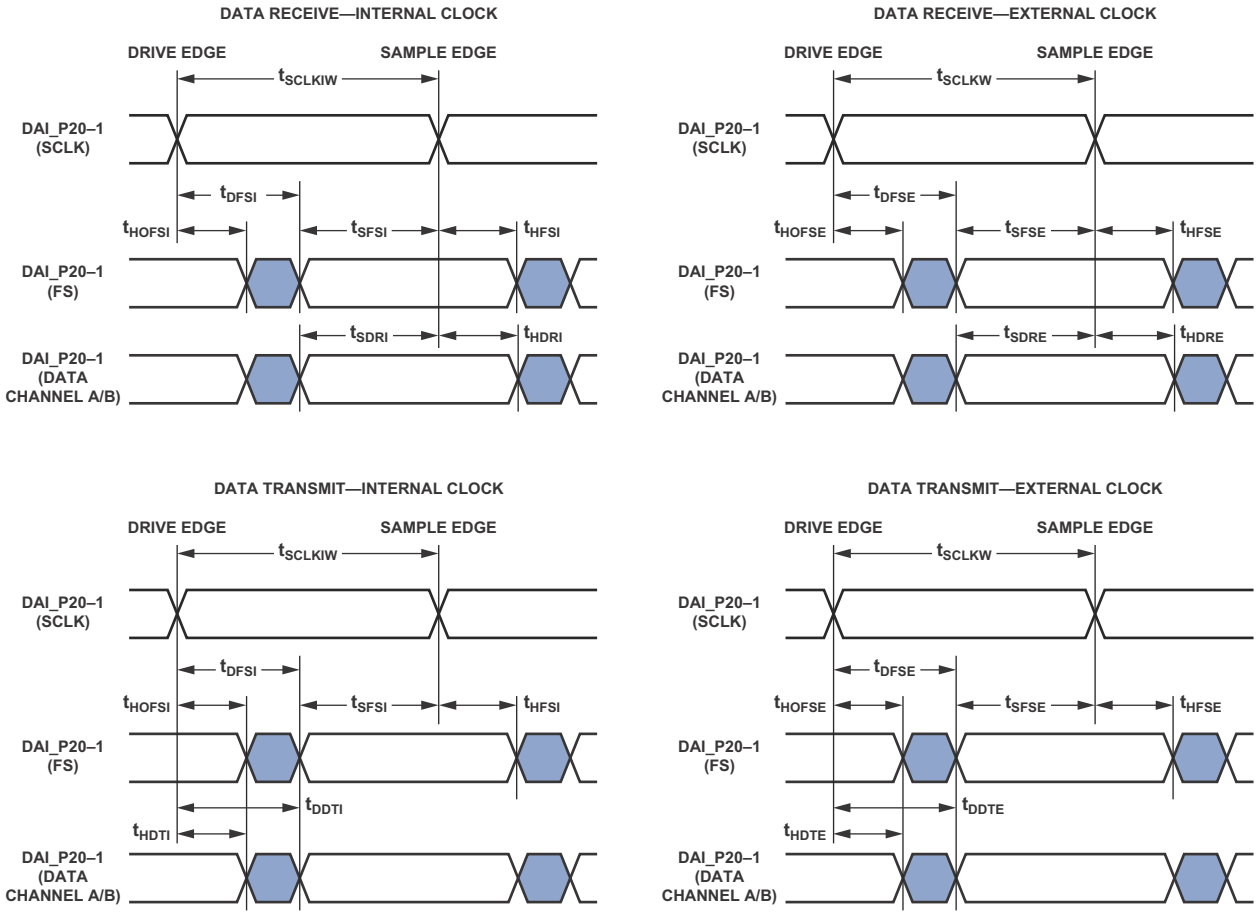

Figure 26. Serial Ports

Table 41. Serial Ports—External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$[1]	Data Delay from Late External Transmit Frame Sync or External Receive Frame Sync with MCE = 1, MFD = 0		7.75	ns
$t_{DDTENFS}$[1]	Data Enable for MCE = 1, MFD = 0	0.5		ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified as well as DSP serial mode, and MCE = 1, MFD = 0.

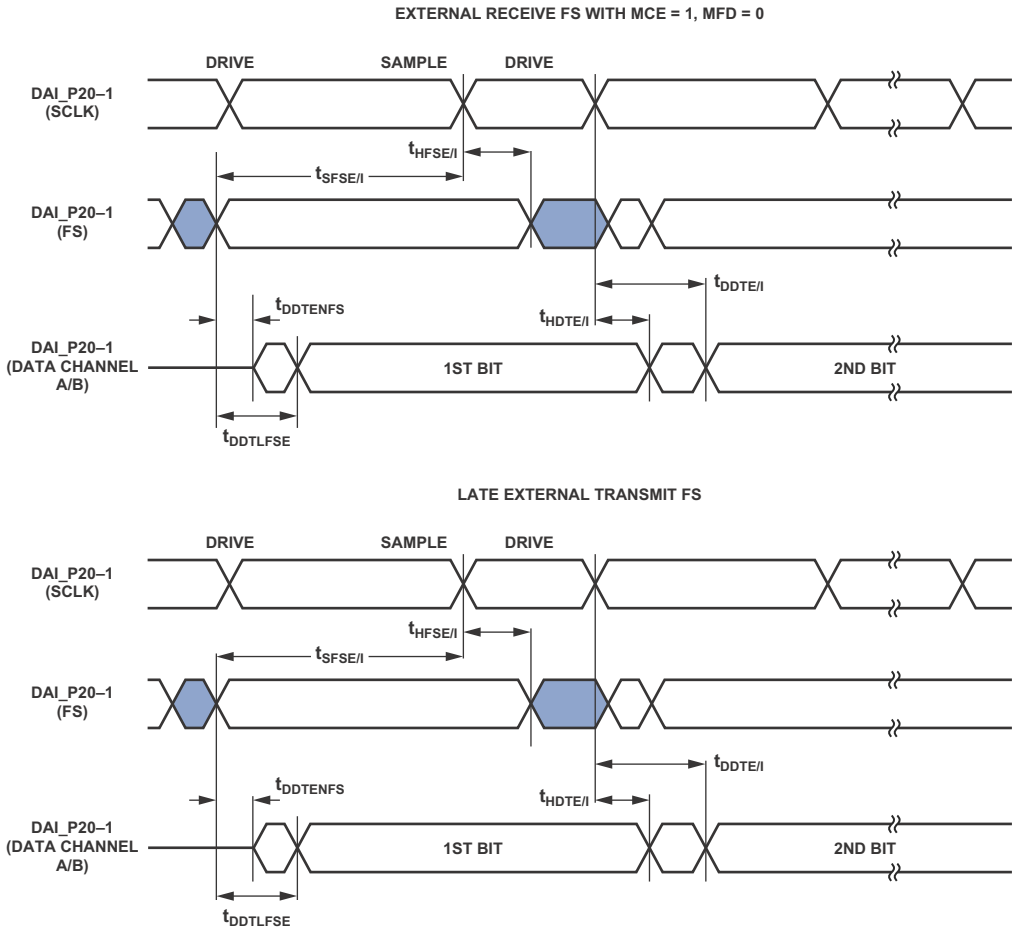

Figure 29. External Late Frame Sync

Input Data Port (IDP)

The timing requirements for the IDP are given in Table 42. IDP signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 42. Input Data Port (IDP)

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	3.8		ns
t_{SIHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	2.5		ns
t_{SISD}[1]	Data Setup Before Serial Clock Rising Edge	2.5		ns
t_{SIHD}[1]	Data Hold After Serial Clock Rising Edge	2.5		ns
$t_{IDPCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{IDPCLK}	Clock Period	$t_{PCLK} \times 4$		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. The PCG's input can be either CLKIN or any of the DAI pins.

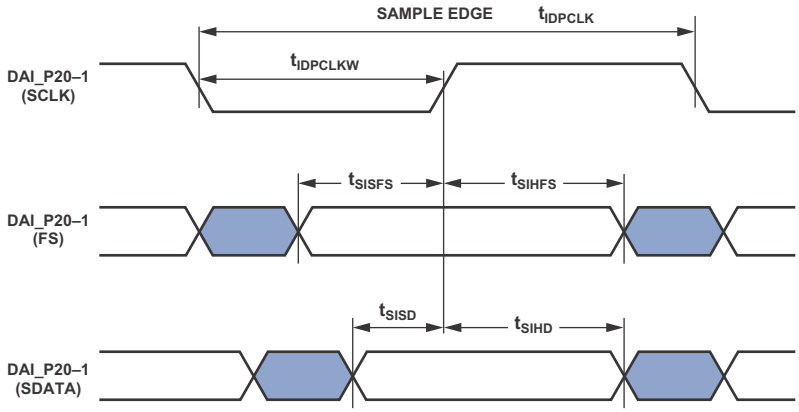

Figure 30. IDP Master Timing

Media Local Bus

All the numbers given are applicable for all speed modes (1024 FS, 512 FS, and 256 FS for 3-pin; 512 FS and 256 FS for 5-pin) unless otherwise specified. Please refer to MediaLB specification document rev 3.0 for more details.

Table 55. MLB Interface, 3-Pin Specifications

Parameter		Min	Typ	Max	Unit
3-Pin Characteristics					
t_{MLBCLK}	MLB Clock Period				
	1024 FS		20.3		ns
	512 FS		40		ns
	256 FS		81		ns
t_{MCKL}	MLBCLK Low Time				
	1024 FS	6.1			ns
	512 FS	14			ns
	256 FS	30			ns
t_{MCKH}	MLBCLK High Time				
	1024 FS	9.3			ns
	512 FS	14			ns
	256 FS	30			ns
t_{MCKR}	MLBCLK Rise Time (V_{IL} to V_{IH})				
	1024 FS			1	ns
	512 FS/256 FS			3	ns
t_{MCKF}	MLBCLK Fall Time (V_{IH} to V_{IL})				
	1024 FS			1	ns
	512 FS/256 FS			3	ns
T_{MPWV}[1]	MLBCLK Pulse Width Variation				
	1024 FS			0.7	ns p-p
	512 FS/256 FS			2.0	ns p-p
t_{DSMCF}	DAT/SIG Input Setup Time	1			ns
t_{DHMCF}	DAT/SIG Input Hold Time	1			ns
t_{MCFDZ}	DAT/SIG Output Time to Three-state	0		15	ns
t_{MCDRV}	DAT/SIG Output Data Delay From MLBCLK Rising Edge			8	ns
t_{MDZH}[2]	Bus Hold Time				
	1024 FS	2			ns
	512 FS/256 FS	4			ns
C_{MLB}	DAT/SIG Pin Load				
	1024 FS			40	pf
	512 FS/256 FS			60	pf

[1] Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in nanoseconds peak-to-peak (ns p-p).
[2] The board must be designed to ensure that the high impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

JTAG Test Access Port and Emulation

Table 57. JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	7		ns
t_{HSYS}[1]	System Inputs Hold After TCK High	18		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width	$4 \times t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		10	ns
t_{DSYS}[2]	System Outputs Delay After TCK Low		$t_{CK} \div 2 + 7$	ns

[1] System Inputs = AMI_DATA, DDR2_DATA, CLKCFG1–0, BOOTCFG2–0 RESET, DAI, DPI, FLAG3–0.
[2] System Outputs = AMI_ADDR/DATA, DDR2_ADDR/DATA, AMI_CTRL, DDR2_CTRL, DAI, DPI, FLAG3–0, $\overline{\text{EMU}}$.

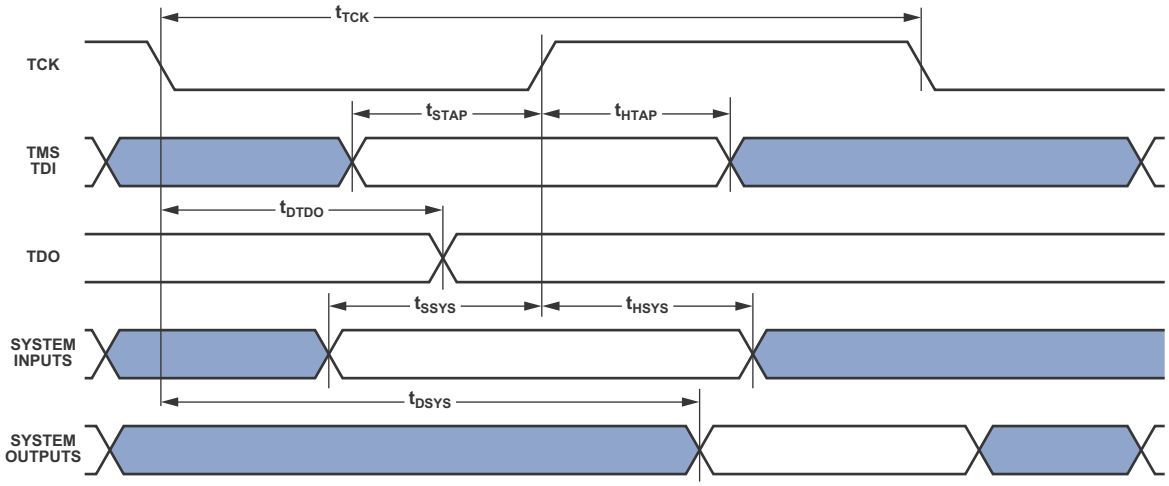

Figure 45. IEEE 1149.1 JTAG Test Access Port

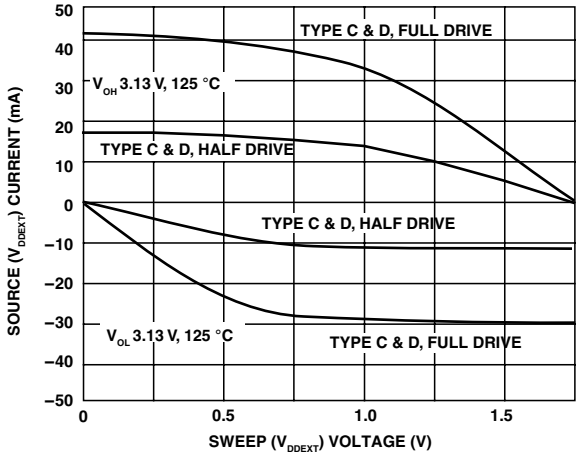

Figure 49. Output Buffer Characteristics (Worst-Case DDR2)

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Table 58). Figure 54 through Figure 59 show graphically how output delays and holds vary with load capacitance. The graphs of Figure 50 through Figure 59 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) vs. Load Capacitance.

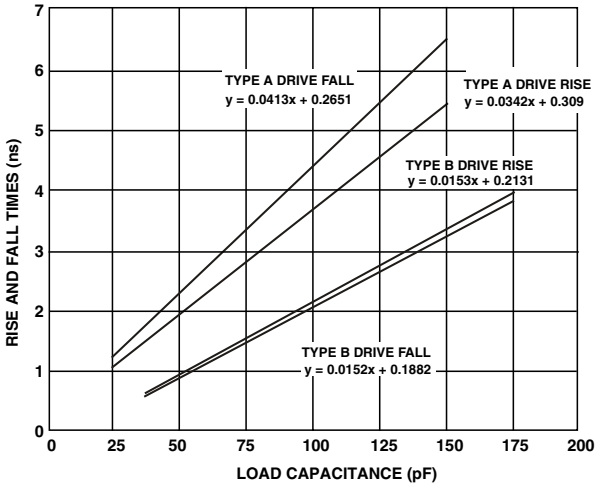

Figure 50. Typical Output Rise/Fall Time Non-DDR2 (20% to 80%, V_{DD_EXT} = Max)

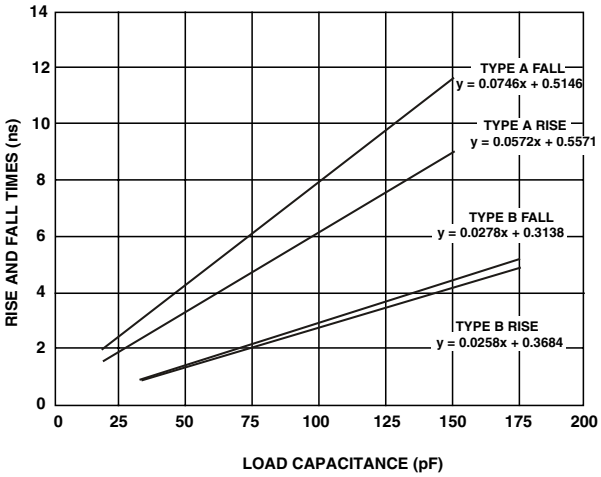

Figure 51. Typical Output Rise/Fall Time Non-DDR2 (20% to 80%, V_{DD_EXT} = Min)

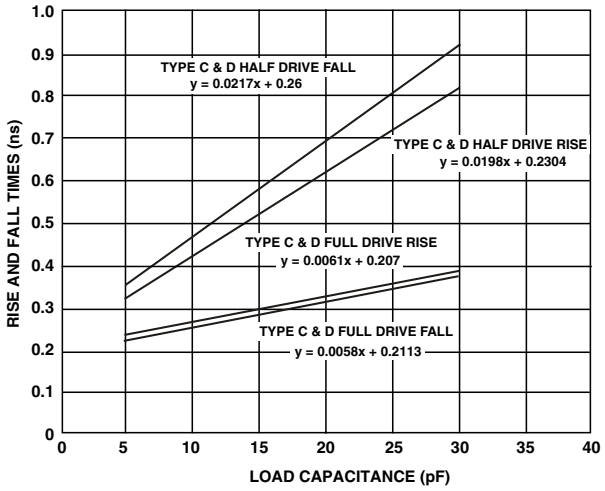

Figure 52. Typical Output Rise/Fall Time DDR2 (20% to 80%, V_{DD_EXT} = Max)

CSP_BGA BALL ASSIGNMENT—STANDARD MODELS

Table 62 lists the standard model CSP_BGA ball assignments by signal.

Table 62. CSP_BGA Ball Assignment (Alphabetical by Signal)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
AGND	H02	BOOT_CFG2	H03	DDR2_BA0	C18	DPI_P03	T01
AMI_ACK	R10	CLK_CFG0	G01	DDR2_BA1	C17	DPI_P04	R01
AMI_ADDR0	V16	CLK_CFG1	G02	DDR2_BA2	B18	DPI_P05	P01
AMI_ADDR01	U16	CLKIN	L01	$\overline{\text{DDR2\_CAS}}$	C07	DPI_P06	P02
AMI_ADDR02	T16	DAI_P01	R06	DDR2_CKE	E01	DPI_P07	P03
AMI_ADDR03	R16	DAI_P02	V05	$\overline{\text{DDR2\_CLK0}}$	A07	DPI_P08	P04
AMI_ADDR04	V15	DAI_P03	R07	DDR2_CLK0	B07	DPI_P09	N01
AMI_ADDR05	U15	DAI_P04	R03	$\overline{\text{DDR2\_CLK1}}$	A13	DPI_P10	N02
AMI_ADDR06	T15	DAI_P05	U05	DDR2_CLK1	B13	DPI_P11	N03
AMI_ADDR07	R15	DAI_P06	T05	$\overline{\text{DDR2\_CS0}}$	C01	DPI_P12	N04
AMI_ADDR08	V14	DAI_P07	V06	$\overline{\text{DDR2\_CS1}}$	D01	DPI_P13	M03
AMI_ADDR09	U14	DAI_P08	V02	$\overline{\text{DDR2\_CS2}}$	C02	DPI_P14	M04
AMI_ADDR10	T14	DAI_P09	R05	$\overline{\text{DDR2\_CS3}}$	D02	$\overline{\text{EMU}}$	K02
AMI_ADDR11	R14	DAI_P10	V04	DDR2_DATA0	B02	FLAG0	R08
AMI_ADDR12	V13	DAI_P11	U04	DDR2_DATA01	A02	FLAG1	V07
AMI_ADDR13	U13	DAI_P12	T04	DDR2_DATA02	B03	FLAG2	U07
AMI_ADDR14	T13	DAI_P13	U06	DDR2_DATA03	A03	FLAG3	T07
AMI_ADDR15	R13	DAI_P14	U02	DDR2_DATA04	B05	GND	A01
AMI_ADDR16	V12	DAI_P15	R04	DDR2_DATA05	A05	GND	A18
AMI_ADDR17	U12	DAI_P16	V03	DDR2_DATA06	B06	GND	C04
AMI_ADDR18	T12	DAI_P17	U03	DDR2_DATA07	A06	GND	C06
AMI_ADDR19	R12	DAI_P18	T03	DDR2_DATA08	B08	GND	C08
AMI_ADDR20	V11	DAI_P19	T06	DDR2_DATA09	A08	GND	D05
AMI_ADDR21	U11	DAI_P20	T02	DDR2_DATA10	B09	GND	D07
AMI_ADDR22	T11	DDR2_ADDR0	D13	DDR2_DATA11	A09	GND	D09
AMI_ADDR23	R11	DDR2_ADDR01	C13	DDR2_DATA12	A11	GND	D10
AMI_DATA0	U18	DDR2_ADDR02	D14	DDR2_DATA13	B11	GND	D17
AMI_DATA1	T18	DDR2_ADDR03	C14	DDR2_DATA14	A12	GND	E03
AMI_DATA2	R18	DDR2_ADDR04	B14	DDR2_DATA15	B12	GND	E05
AMI_DATA3	P18	DDR2_ADDR05	A14	DDR2_DM0	C03	GND	E12
AMI_DATA4	V17	DDR2_ADDR06	D15	DDR2_DM1	C11	GND	E13
AMI_DATA5	U17	DDR2_ADDR07	C15	DDR2_DQS0	A04	GND	E16
AMI_DATA6	T17	DDR2_ADDR08	B15	$\overline{\text{DDR2\_DQS0}}$	B04	GND	F01
AMI_DATA7	R17	DDR2_ADDR09	A15	DDR2_DQS1	A10	GND	F02
$\overline{\text{AMI\_MS0}}$	T10	DDR2_ADDR10	D16	$\overline{\text{DDR2\_DQS1}}$	B10	GND	F04
$\overline{\text{AMI\_MS1}}$	U10	DDR2_ADDR11	C16	DDR2_ODT	B01	GND	F14
$\overline{\text{AMI\_RD}}$	J04	DDR2_ADDR12	B16	$\overline{\text{DDR2\_RAS}}$	C09	GND	F16
$\overline{\text{AMI\_WR}}$	V10	DDR2_ADDR13	A16	$\overline{\text{DDR2\_WE}}$	C10	GND	G05
BOOT_CFG0	J02	DDR2_ADDR14	B17	DPI_P01	R02	GND	G07
BOOT_CFG1	J03	DDR2_ADDR15	A17	DPI_P02	U01	GND	G08

Table 62. CSP_BGA Ball Assignment (Alphabetical by Signal) (Continued)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
GND	G09	GND	M09	TMS	K16	V_{DD_INT}	E08
GND	G10	GND	M10	$\overline{TRST}$	N15	V_{DD_INT}	E09
GND	G11	GND	M11	VDD_A	H01	V_{DD_INT}	E14
GND	G12	GND	M12	V_{DD_DDR2}	C05	V_{DD_INT}	E15
GND	G15	GND	N14	V_{DD_DDR2}	C12	V_{DD_INT}	F06
GND	H04	GND	N17	V_{DD_DDR2}	D03	V_{DD_INT}	F07
GND	H07	GND	P05	V_{DD_DDR2}	D06	V_{DD_INT}	F08
GND	H08	GND	P07	V_{DD_DDR2}	D08	V_{DD_INT}	F09
GND	H09	GND	P09	V_{DD_DDR2}	D18	V_{DD_INT}	F10
GND	H10	GND	P11	V_{DD_DDR2}	E02	V_{DD_INT}	F11
GND	H11	GND	P13	V_{DD_DDR2}	E04	V_{DD_INT}	F12
GND	H12	GND	R09	V_{DD_DDR2}	E07	V_{DD_INT}	F13
GND	J01	GND	V01	V_{DD_DDR2}	E10	V_{DD_INT}	G06
GND	J07	GND	V18	V_{DD_DDR2}	E11	V_{DD_INT}	G13
GND	J08	GND/ID0[1]	G03	V_{DD_DDR2}	E17	V_{DD_INT}	H05
GND	J09	GND/ID1[1]	G04	V_{DD_DDR2}	F03	V_{DD_INT}	H06
GND	J10	LACK_0	K17	V_{DD_DDR2}	F05	V_{DD_INT}	H13
GND	J11	LACK_1	P17	V_{DD_DDR2}	F15	V_{DD_INT}	H14
GND	J12	LCLK_0	J18	V_{DD_DDR2}	G14	V_{DD_INT}	J06
GND	J14	LCLK_1	N18	V_{DD_DDR2}	G16	V_{DD_INT}	J13
GND	J17	LDAT0_0	E18	V_{DD_EXT}	H15	V_{DD_INT}	K06
GND	K03	LDAT0_1	F17	V_{DD_EXT}	H18	V_{DD_INT}	K13
GND	K04	LDAT0_2	F18	V_{DD_EXT}	J05	V_{DD_INT}	L06
GND	K05	LDAT0_3	G17	V_{DD_EXT}	J15	V_{DD_INT}	L13
GND	K07	LDAT0_4	G18	V_{DD_EXT}	K14	V_{DD_INT}	M06
GND	K08	LDAT0_5	H16	V_{DD_EXT}	L05	V_{DD_INT}	M13
GND	K09	LDAT0_6	H17	V_{DD_EXT}	M14	V_{DD_INT}	N06
GND	K10	LDAT0_7	J16	V_{DD_EXT}	M18	V_{DD_INT}	N07
GND	K11	LDAT1_0	K18	V_{DD_EXT}	N05	V_{DD_INT}	N08
GND	K12	LDAT1_1	L16	V_{DD_EXT}	P06	V_{DD_INT}	N09
GND	L02	LDAT1_2	L17	V_{DD_EXT}	P08	V_{DD_INT}	N13
GND	L03	LDAT1_3	L18	V_{DD_EXT}	P10	V_{DD_THD}	N10
GND	L04	LDAT1_4	M16	V_{DD_EXT}	P12	V_{REF}	D04
GND	L07	LDAT1_5	M17	V_{DD_EXT}	P14	V_{REF}	D11
GND	L08	LDAT1_6	N16	V_{DD_EXT}	P15	XTAL	K01
GND	L09	LDAT1_7	P16	V_{DD_EXT}	T08		
GND	L10	$\overline{RESET}$	M01	V_{DD_EXT}	T09		
GND	L11	$\overline{RESETOUT}$/$\overline{RUNRSTIN}$	M02	V_{DD_EXT}	U09		
GND	L12	TCK	K15	V_{DD_EXT}	V09		
GND	L14	TDI	L15	V_{DD_EXT}/$\overline{BR1}$[1]	V08		
GND	M05	TDO	M15	V_{DD_EXT}/$\overline{BR2}$[1]	U08		
GND	M07	THD_M	N12	V_{DD_INT}	D12		
GND	M08	THD_P	N11	V_{DD_INT}	E06		

[1] This pin can be used for shared DDR2 memory between two processors. If shared memory functionality is not used then $\overline{BRx}$ pins should be tied to V_{DD_EXT} and IDx pins should be tied to GND. Table 10 on Page 14 for appropriate connections.

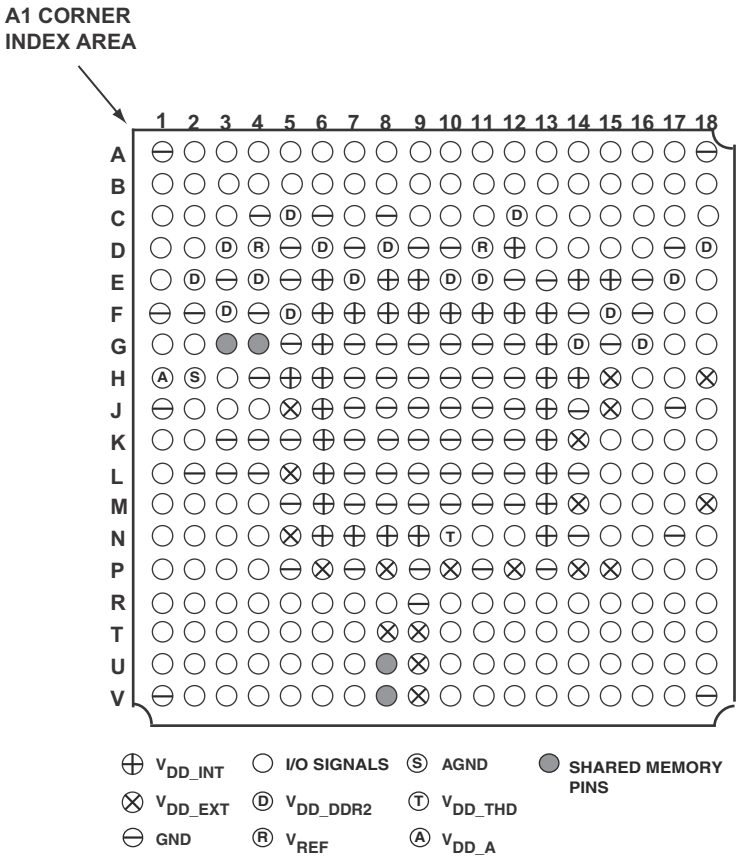

Figure 61. Ball Configuration, Standard Model

AUTOMOTIVE PRODUCTS

The ADSP-21467W and ADSP-21469W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that automotive models may have specifications that differ from commercial models and designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown in Table 63 are available for use in automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Table 63. Automotive Product Models

Model [1, 2, 3]	Temperature Range[4]	On-Chip SRAM	Package Description	Package Option
AD21467WBBCZ3Axx	–40°C to +85°C	5 Mbits	324-Ball CSP_BGA	BC-324-1
AD21469WBBCZ3xx	–40°C to +85°C	5 Mbits	324-Ball CSP_BGA	BC-324-1

[1] Z = RoHS compliant part.
[2] xx denotes silicon revision.
[3] Axx = ROM version A.
[4] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 19 for junction temperature (T_J) specification, which is the only temperature specification.

ORDERING GUIDE

Model	Notes	Temperature Range[1]	On-Chip SRAM	Processor Instruction Rate (Max)	Package Description	Package Option
ADSP-21469KBCZ-3	[2]	0°C to +70°C	5 Mbits	400 MHz	324-Ball CSP_BGA	BC-324-1
ADSP-21469BBC-3		–40°C to +85°C	5 Mbits	400 MHz	324-Ball CSP_BGA	BC-324-1
ADSP-21469BBCZ-3	[2]	–40°C to +85°C	5 Mbits	400 MHz	324-Ball CSP_BGA	BC-324-1
ADSP-21469KBCZ-4	[2]	0°C to +70°C	5 Mbits	450 MHz	324-Ball CSP_BGA	BC-324-1

[1] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 19 for junction temperature (T_J) specification, which is the only temperature specification.
[2] Z = RoHS compliant part.