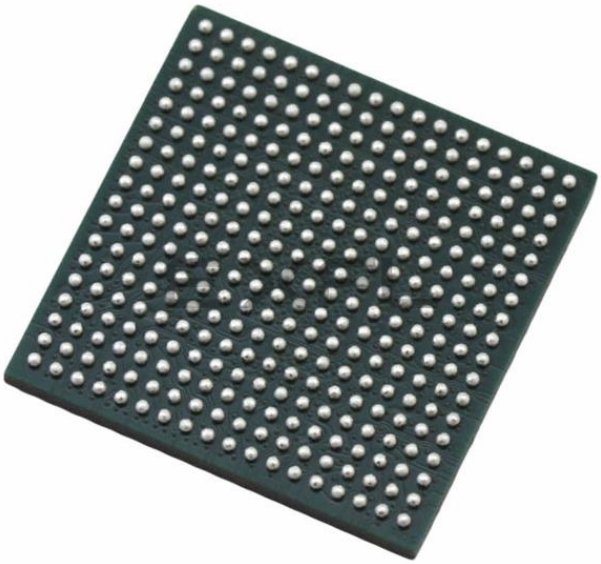

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## Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

## Applications of Embedded - DSP (Digital Signal Processors)

| Details | |
|---|---|
| Product Status | Obsolete |
| Type | Floating Point |
| Interface | DAI, DPI, EBI/EMI, I²C, SCI, SPI, SSP, UART/USART |
| Clock Rate | 400MHz |
| Non-Volatile Memory | External |
| On-Chip RAM | 5Mbit |
| Voltage - I/O | 3.30V |
| Voltage - Core | 1.05V |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 324-BGA, CSPBGA |
| Supplier Device Package | 324-CSPBGA (19x19) |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/adsp-21469bbc-3 |

As shown in Figure 1 on Page 1, the processor uses two computational units to deliver a significant performance increase over the previous SHARC processors on a range of DSP algorithms. With its SIMD computational hardware, the processors can perform 2.7 GFLOPS running at 450 MHz and 2.4 GFLOPS running at 400 MHz.

## FAMILY CORE ARCHITECTURE

The processors are code compatible at the assembly level with the ADSP-2137x, ADSP-2136x, ADSP-2126x, ADSP-21160, and ADSP-21161, and with the first generation ADSP-2106x SHARC processors. The ADSP-21467/ADSP-21469 processors share architectural features with the ADSP-2126x, ADSP-2136x, ADSP-2137x, and ADSP-2116x SIMD SHARC processors, as shown in Figure 2 and detailed in the following sections.

### *SIMD Computational Engine*

The processor contains two computational processing elements that operate as a single-instruction, multiple-data (SIMD) engine. The processing elements are referred to as PEX and PEY and each contains an ALU, multiplier, shifter, and register file. PEX is always active, and PEY may be enabled by setting the PEYEN mode bit in the MODE1 register. When this mode is enabled, the same instruction is executed in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math intensive DSP algorithms.

Entering SIMD mode also has an effect on the way data is transferred between memory and the processing elements. When in SIMD mode, twice the data bandwidth is required to sustain computational operation in the processing elements. Because of this requirement, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each access of memory or the register file.

### *Independent, Parallel Computation Units*

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform all operations in a single cycle. The three units within each processing element are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single-precision floating-point, 40-bit extended precision floating-point, and 32-bit fixed-point data formats.

### *Timer*

A core timer that can generate periodic software interrupts. The core timer can be configured to use FLAG3 as a timer expired signal.

### *Data Register File*

A general-purpose data register file is contained in each processing element. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the processor's enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0-R15 and in PEY as S0-S15.

### *Context Switch*

Many of the processor's registers have secondary registers that can be activated during interrupt servicing for a fast context switch. The data registers in the register file, the DAG registers, and the multiplier result registers all have secondary registers. The primary registers are active at reset, while the secondary registers are activated by control bits in a mode control register.

### *Universal Registers*

These registers can be used for general-purpose tasks. The USTAT (4) registers allow easy bit manipulations (Set, Clear, Toggle, Test, XOR) for all system registers (control/status) of the core.

The data bus exchange register (PX) permits data to be passed between the 64-bit PM data bus and the 64-bit DM data bus, or between the 40-bit register file and the PM/DM data buses. These registers contain hardware to handle the data width difference.

### *Single-Cycle Fetch of Instruction and Four Operands*

The processors feature an enhanced Harvard Architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 2). With the its separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction (from the cache), all in a single cycle.

### *Instruction Cache*

The processors contain an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache allows full speed execution of core, looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

### *Data Address Generators With Zero-Overhead Hardware Circular Buffer Support*

The two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the processors contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

### *Designing an Emulator-Compatible DSP Board (Target)*

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

## ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21467/ADSP-21469 architecture and functionality. For detailed information on the core architecture and instruction set, refer to the *SHARC Processor Programming Reference*.

## RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in Wikipedia or the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (http://www.analog.com/signal chains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

# SPECIFICATIONS

## OPERATING CONDITIONS

| Parameter[1] | Description | 450 MHz | | | 400 MHz | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Nom | Max | Min | Nom | Max | |
| $V_{DD\_INT}$ | Internal (Core) Supply Voltage | 1.05 | 1.1 | 1.15 | 1.0 | 1.05 | 1.1 | V |
| $V_{DD\_EXT}$ | External (I/O) Supply Voltage | 3.13 | 3.3 | 3.47 | 3.13 | 3.3 | 3.47 | V |
| $V_{DD\_A}$[2] | Analog Power Supply Voltage | 1.05 | 1.1 | 1.15 | 1.0 | 1.05 | 1.1 | V |
| $V_{DD\_DDR2}$[3, 4] | DDR2 Controller Supply Voltage | 1.7 | 1.8 | 1.9 | 1.7 | 1.8 | 1.9 | V |
| $V_{DD\_THD}$ | Thermal Diode Supply Voltage | 3.13 | 3.3 | 3.47 | 3.13 | 3.3 | 3.47 | V |
| $V_{REF}$ | DDR2 Reference Voltage | 0.84 | 0.9 | 0.96 | 0.84 | 0.9 | 0.96 | V |
| $V_{IH}$[5] | High Level Input Voltage @ $V_{DD\_EXT}$ = Max | 2.0 | | | 2.0 | | | V |
| $V_{IL}$[5] | Low Level Input Voltage @ $V_{DD\_EXT}$ = Min | | | 0.8 | | | 0.8 | V |
| $V_{IH\_CLKIN}$[6] | High Level Input Voltage @ $V_{DD\_EXT}$ = Max | 2.0 | | | 2.0 | | | V |
| $V_{IL\_CLKIN}$[6] | Low Level Input Voltage @ $V_{DD\_EXT}$ = Min | | | 1.32 | | | 1.32 | V |
| $V_{IL\_DDR2}$ (DC) | DC Low Level Input Voltage | | | $V_{REF}$ – 0.125 | | | $V_{REF}$ – 0.125 | V |
| $V_{IH\_DDR2}$ (DC) | DC High Level Input Voltage | $V_{REF}$ + 0.125 | | | $V_{REF}$ + 0.125 | | | V |
| $V_{IL\_DDR2}$ (AC) | AC Low Level Input Voltage | | | $V_{REF}$ – 0.25 | | | $V_{REF}$ – 0.25 | V |
| $V_{IH\_DDR2}$ (AC) | AC High Level Input Voltage | $V_{REF}$ + 0.25 | | | $V_{REF}$ + 0.25 | | | V |
| $T_J$ | Junction Temperature 324-Lead CSP_BGA @ $T_{AMBIENT}$ 0°C to +70°C | 0 | | 115 | 0 | | 110 | °C |
| $T_J$ | Junction Temperature 324-Lead CSP_BGA @ $T_{AMBIENT}$ –40°C to +85°C | N/A | | N/A | –40 | | 125 | °C |

[1] Specifications subject to change without notice.
[2] See Figure 3 on Page 11 for an example filter circuit.
[3] Applies to DDR2 signals.
[4] If unused, see Table 9 on Page 13.
[5] Applies to input and bidirectional pins: AMI_ADDR23–0, AMI_DATA7–0, FLAG3–0, DAI_Px, DPI_Px, BOOTCFGx, CLKCFGx, ($\overline{\text{RUNRSTIN}}$), $\overline{\text{RESET}}$, TCK, TMS, TDI, $\overline{\text{TRST}}$.
[6] Applies to input pin CLKIN.

**Table 14. Dynamic Current in CCLK Domain—$I_{DD\_INT\_DYNAMIC}$ (mA, with ASF = 1.0)[1]**

| $f_{CCLK}$ (MHz)[2] | $V_{DD\_INT}$(V)[2] | | | | |
|---|---|---|---|---|---|
| | **0.95 V** | **1.0 V** | **1.05 V** | **1.10 V** | **1.15 V** |
| 100 | 78 | 82 | 86 | 91 | 98 |
| 150 | 115 | 121 | 130 | 136 | 142 |
| 200 | 150 | 159 | 169 | 177 | 188 |
| 250 | 186 | 197 | 208 | 219 | 231 |
| 300 | 222 | 236 | 249 | 261 | 276 |
| 350 | 259 | 275 | 288 | 304 | 319 |
| 400 | 293 | 309 | 328 | 344 | 361 |
| 450 | N/A | N/A | 366 | 385 | 406 |

[1] The values are not guaranteed as standalone maximum specifications. They must be combined with static current per the equations of Electrical Characteristics on Page 20.
[2] Valid frequency and voltage ranges are model-specific. See Operating Conditions on Page 19.

## ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 15 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 15. Absolute Maximum Ratings**

| Parameter | Rating |
|---|---|
| Internal (Core) Supply Voltage ($V_{DD\_INT}$) | –0.3 V to +1.32 V |
| Analog (PLL) Supply Voltage ($V_{DD\_A}$) | –0.3 V to +1.15 V |
| External (I/O) Supply Voltage ($V_{DD\_EXT}$) | –0.3 V to +3.6 V |
| Thermal Diode Supply Voltage ($V_{DD\_THD}$) | –0.3 V to +3.6 V |
| DDR2 Controller Supply Voltage ($V_{DD\_DDR2}$) | –0.3 V to +1.9 V |
| DDR2 Input Voltage | –0.3 V to +1.9 V |
| Input Voltage | –0.3 V to +3.6 V |
| Output Voltage Swing | –0.3 V to $V_{DD\_EXT}$ +0.5 V |
| Storage Temperature Range | –65°C to +150°C |
| Junction Temperature While Biased | 125°C |

## PACKAGE INFORMATION

The information presented in Figure 4 and Table 16 provides details about the package branding for the processor. For a complete listing of product availability, see Ordering Guide on Page 74.


*Figure 4. Typical Package Brand*

**Table 16. Package Brand Information[1]**

| Brand Key | Field Description |
|---|---|
| t | Temperature Range |
| pp | Package Type |
| Z | RoHS Compliant Option |
| cc | See Ordering Guide |
| vvvvvv.x | Assembly Lot Code |
| n.n | Silicon Revision |
| # | RoHS Compliant Designation |
| yyww | Date Code |

[1] Non-automotive only. For branding information specific to automotive products, contact Analog Devices, Inc.

### Power-Up Sequencing

The timing requirements for processor startup are given in Table 18. While no specific power-up sequencing is required between $V_{DD\_EXT}$, $V_{DD\_DDR2}$, and $V_{DD\_INT}$, there are some considerations that system designs should take into account.

- No power supply should be powered up for an extended period of time (> 200 ms) before another supply starts to ramp up.
- If $V_{DD\_INT}$ power supply comes up after $V_{DD\_EXT}$, any pin, such as $\overline{\text{RESETOUT}}$ and $\overline{\text{RESET}}$, may actually drive momentarily until the $V_{DD\_INT}$ rail has powered up. Systems sharing these signals on the board must determine if there are any issues that need to be addressed based on this behavior.

Note that during power-up, when the $V_{DD\_INT}$ power supply comes up after $V_{DD\_EXT}$, a leakage current of the order of three-state leakage current pull-up, pull-down may be observed on any pin, even if that pin is an input only (for example the $\overline{\text{RESET}}$ pin) until the $V_{DD\_INT}$ rail has powered up.

**Table 18. Power-Up Sequencing Timing Requirements (Processor Startup)**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{RSTVDD}$ | $\overline{\text{RESET}}$ Low Before $V_{DD\_INT}$ or $V_{DD\_EXT}$ or $V_{DD\_DDR2}$ On | 0 | | ms |
| $t_{IVDD-EVDD}$ | $V_{DD\_INT}$ On Before $V_{DD\_EXT}$ | –200 | +200 | ms |
| $t_{EVDD\_DDR2VDD}$ | $V_{DD\_EXT}$ On Before $V_{DD\_DDR2}$ | –200 | +200 | ms |
| $t_{CLKVDD}$[1] | CLKIN Valid After $V_{DD\_INT}$ or $V_{DD\_EXT}$ or $V_{DD\_DDR2}$ Valid | 0 | 200 | ms |
| $t_{CLKRST}$ | CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted | 10[2] | | µs |
| $t_{PLLRST}$ | PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted | 20[3] | | µs |
| *Switching Characteristic* | | | | |
| $t_{CORERST}$ | Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted | $4096 \times t_{CK} + 2 \times t_{CCLK}$ [4, 5] | | |

[1] Valid $V_{DD\_INT}$ assumes that the supply is fully ramped to its nominal value. Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.
[2] Assumes a stable CLKIN signal, after meeting worst-case startup timing of crystal oscillators. Refer to your crystal oscillator manufacturer's data sheet for startup time. Assume a 25 ms maximum oscillator startup time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.
[3] Based on CLKIN cycles.
[4] Applies after the power-up sequence is complete. Subsequent resets require a minimum of four CLKIN cycles for $\overline{\text{RESET}}$ to be held low in order to properly initialize and propagate default states at all I/O pins.
[5] The 4096 cycle count depends on $t_{SRST}$ specification in Table 20. If setup time is not met, one additional CLKIN cycle may be added to the core reset time, resulting in 4097 cycles maximum.

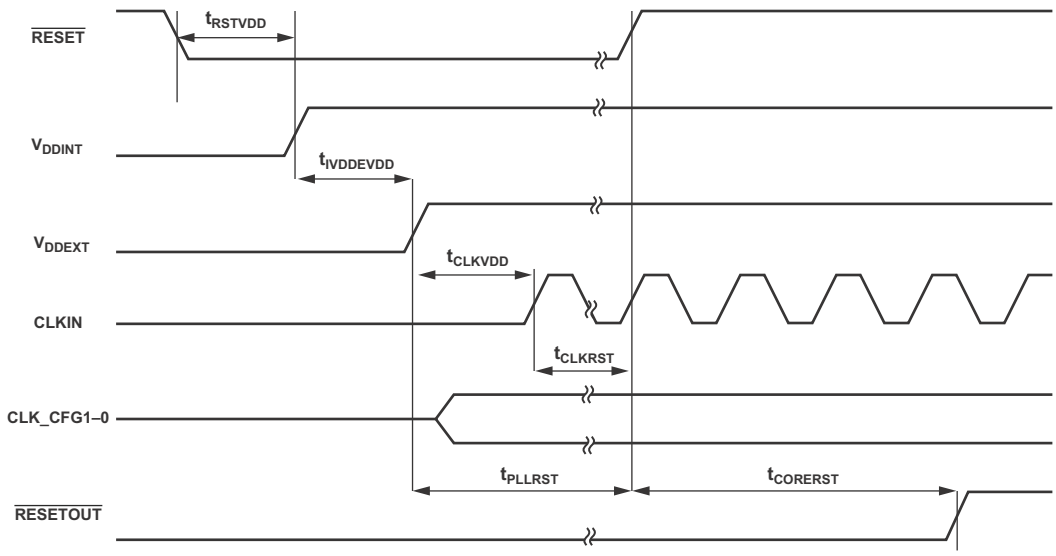



*Figure 6. Power-Up Sequencing*

### Clock Input

**Table 19. Clock Input**

| Parameter | | 400 MHz[1] Min | 400 MHz[1] Max | 450 MHz[2] Min | 450 MHz[2] Max | Unit |
|---|---|---|---|---|---|---|
| *Timing Requirements* | | | | | | |
| $t_{CK}$ | CLKIN Period | 15[3] | 100 | 13.26 | 100 | ns |
| $t_{CKL}$ | CLKIN Width Low | 7.5 | 45 | 6.63 | 45 | ns |
| $t_{CKH}$ | CLKIN Width High | 7.5 | 45 | 6.63 | 45 | ns |
| $t_{CKRF}$ | CLKIN Rise/Fall (0.4 V to 2.0 V) | | 3[4] | | 3[4] | ns |
| $t_{CCLK}$[5] | CCLK Period | 2.5 | 10 | 2.22 | 10 | ns |
| $f_{VCO}$[6] | VCO Frequency | 200 | 900 | 200 | 900 | MHz |
| $t_{CKJ}$[7, 8] | CLKIN Jitter Tolerance | –250 | +250 | –250 | +250 | ps |

[1] Applies to all 400 MHz models. See Ordering Guide on Page 74.
[2] Applies to all 450 MHz models. See Ordering Guide on Page 74.
[3] Applies only for CLK_CFG1–0 = 00 and default values for PLL control bits in PMCTL.
[4] Guaranteed by simulation but not tested on silicon.
[5] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification $t_{CCLK}$.
[6] See Figure 5 on Page 24 for VCO diagram.
[7] Actual input jitter should be combined with ac specifications for accurate timing analysis.
[8] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

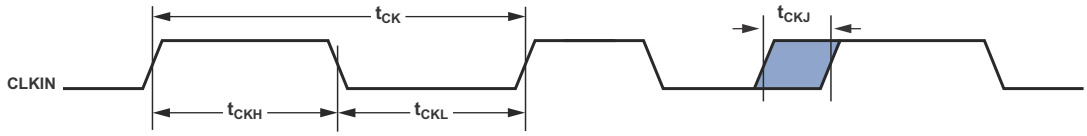



*Figure 7. Clock Input*

### Clock Signals

The processor can use an external clock or a crystal. See the CLKIN pin description in Table 10. Programs can configure the processor to use its internal clock generator by connecting the necessary components to CLKIN and XTAL. Figure 8 shows the component connections used for a crystal operating in fundamental mode. Note that the clock rate is achieved using a 25 MHz crystal and a PLL multiplier ratio 16:1 (CCLK:CLKIN achieves a clock speed of 400 MHz).

To achieve the full core clock rate, programs need to configure the multiplier bits in the PMCTL register.

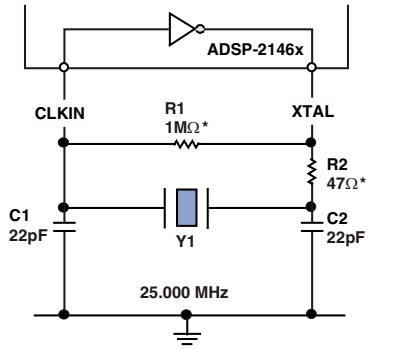



*Figure 8. Recommended Circuit for Fundamental Mode Crystal Operation*

### *Timer PWM_OUT Cycle Timing*

The following timing specification applies to Timer0 and Timer1 in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DPI_P14–1 pins through the DPI SRU. Therefore, the timing specifications provided below are valid at the DPI_P14–1 pins.

**Table 24. Timer PWM_OUT Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Switching Characteristic* | | | | |
| $t_{PWMO}$ | Timer Pulse Width Output | $2 \times t_{PCLK} - 1.2$ | $2 \times (2^{31} - 1) \times t_{PCLK}$ | ns |

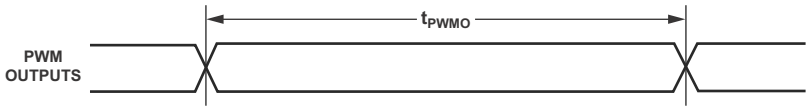



*Figure 13. Timer PWM_OUT Timing*

### *Timer WDTH_CAP Timing*

The following timing specification applies to Timer0 and Timer1 in WDTH_CAP (pulse width count and capture) mode. Timer signals are routed to the DPI_P14–1 pins through the SRU. Therefore, the timing specifications provided below are valid at the DPI_P14–1 pins.

**Table 25. Timer Width Capture Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirement* | | | | |
| $t_{PWI}$ | Timer Pulse Width | $2 \times t_{PCLK}$ | $2 \times (2^{31} - 1) \times t_{PCLK}$ | ns |

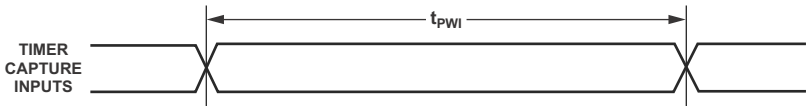



*Figure 14. Timer Width Capture Timing*

### *Flags*

The timing specifications provided below apply to AMI_ADDR23–0 and AMI_DATA7–0 when configured as FLAGS. See Table 10 on Page 14 for more information on flag use.

**Table 28. Flags**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirement* | | | | |
| $t_{FIPW}$ | DPI_P14–1, AMI_ADDR23–0, AMI_DATA7–0, FLAG3–0 IN Pulse Width | $2 \times t_{PCLK} + 3$ | | ns |
| *Switching Characteristic* | | | | |
| $t_{FOPW}$ | DPI_P14–1, AMI_ADDR23–0, AMI_DATA7–0, FLAG3–0 OUT Pulse Width | $2 \times t_{PCLK} - 3$ | | ns |

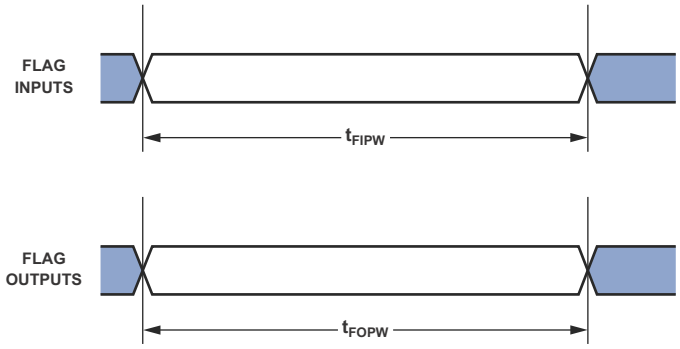
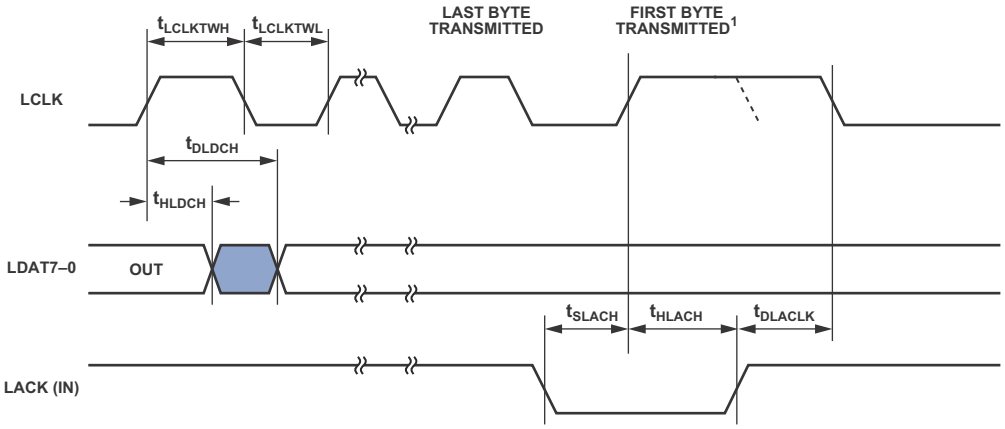



*Figure 17. Flags*




**NOTES**
The $t_{SLACH}$ and $t_{HLACH}$ specifications apply only to the LACK falling edge. If these specifications are met, LCLK would extend and the dotted LCLK falling edge would not occur as shown. The $t_{SLACH}$ and $t_{HLACH}$ requirement apply to the falling edge of LCLK only for the first byte transmitted.

*Figure 25. Link Ports—Transmit (Bit 6 Set)*

### *Serial Ports*

In slave transmitter mode and master receiver mode the maximum serial port frequency is $f_{PCLK}/8$. To determine whether communication is possible between two devices at clock speed *n*, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) serial clock (SCLK) width.

Serial port signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins. In Figure 26 either the rising edge or the falling edge of SCLK (external or internal) can be used as the active sampling edge.

**Table 37. Serial Ports—External Clock**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SFSE}$[1] | Frame Sync Setup Before SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode) | 2.5 | | ns |
| $t_{HFSE}$[1] | Frame Sync Hold After SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode) | 2.5 | | ns |
| $t_{SDRE}$[1] | Receive Data Setup Before Receive SCLK | 1.9 | | ns |
| $t_{HDRE}$[1] | Receive Data Hold After SCLK | 2.5 | | ns |
| $t_{SCLKW}$ | SCLK Width | $(t_{PCLK} \times 4) \div 2 - 1.2$ | | ns |
| $t_{SCLK}$ | SCLK Period | $t_{PCLK} \times 4$ | | ns |
| *Switching Characteristics* | | | | |
| $t_{DFSE}$[2] | Frame Sync Delay After SCLK (Internally Generated Frame Sync in either Transmit or Receive Mode) | | 10.25 | ns |
| $t_{HOFSE}$[2] | Frame Sync Hold After SCLK (Internally Generated Frame Sync in either Transmit or Receive Mode) | 2 | | ns |
| $t_{DDTE}$[2] | Transmit Data Delay After Transmit SCLK | | 8.5 | ns |
| $t_{HDTE}$[2] | Transmit Data Hold After Transmit SCLK | 2 | | ns |

[1] Referenced to sample edge.
[2] Referenced to drive edge.

**Table 38. Serial Ports—Internal Clock**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SFSI}$[1] | Frame Sync Setup Before SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode) | 7 | | ns |
| $t_{HFSI}$[1] | Frame Sync Hold After SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode) | 2.5 | | ns |
| $t_{SDRI}$[1] | Receive Data Setup Before SCLK | 7 | | ns |
| $t_{HDRI}$[1] | Receive Data Hold After SCLK | 2.5 | | ns |
| *Switching Characteristics* | | | | |
| $t_{DFSI}$[2] | Frame Sync Delay After SCLK (Internally Generated Frame Sync in Transmit Mode) | | 4 | ns |
| $t_{HOFSI}$[2] | Frame Sync Hold After SCLK (Internally Generated Frame Sync in Transmit Mode) | –1.0 | | ns |
| $t_{DFSIR}$[2] | Frame Sync Delay After SCLK (Internally Generated Frame Sync in Receive Mode) | | 9.75 | ns |
| $t_{HOFSIR}$[2] | Frame Sync Hold After SCLK (Internally Generated Frame Sync in Receive Mode) | –1.0 | | ns |
| $t_{DDTI}$[2] | Transmit Data Delay After SCLK | | 3.25 | ns |
| $t_{HDTI}$[2] | Transmit Data Hold After SCLK | –1.25 | | ns |
| $t_{SCLKIW}$ | Transmit or Receive SCLK Width | $2 \times t_{PCLK} - 1.2$ | $2 \times t_{PCLK} + 1.5$ | ns |

[1] Referenced to the sample edge.
[2] Referenced to drive edge.

**Table 39. Serial Ports—Enable and Three-State**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Switching Characteristics* | | | | |
| $t_{DDTEN}$[1] | Data Enable from External Transmit SCLK | 2 | | ns |
| $t_{DDTTE}$[1] | Data Disable from External Transmit SCLK | | 11.5 | ns |
| $t_{DDTIN}$[1] | Data Enable from Internal Transmit SCLK | –1 | | ns |

[1] Referenced to drive edge.

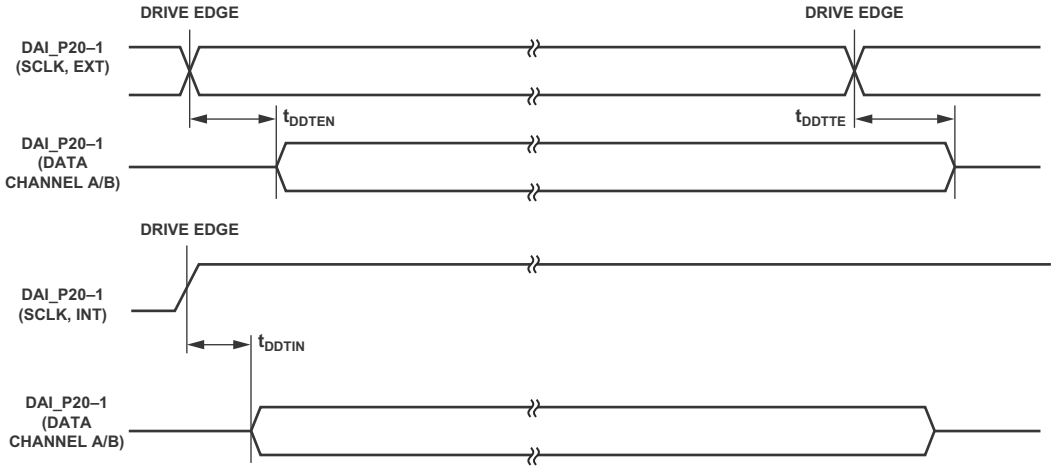



*Figure 27. Serial Ports—Enable and Three-State*

### *Input Data Port (IDP)*

The timing requirements for the IDP are given in Table 42. IDP signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

**Table 42. Input Data Port (IDP)**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SISFS}$[1] | Frame Sync Setup Before Serial Clock Rising Edge | 3.8 | | ns |
| $t_{SIHFS}$[1] | Frame Sync Hold After Serial Clock Rising Edge | 2.5 | | ns |
| $t_{SISD}$[1] | Data Setup Before Serial Clock Rising Edge | 2.5 | | ns |
| $t_{SIHD}$[1] | Data Hold After Serial Clock Rising Edge | 2.5 | | ns |
| $t_{IDPCLKW}$ | Clock Width | $(t_{PCLK} \times 4) \div 2 - 1$ | | ns |
| $t_{IDPCLK}$ | Clock Period | $t_{PCLK} \times 4$ | | ns |

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. The PCG's input can be either CLKIN or any of the DAI pins.

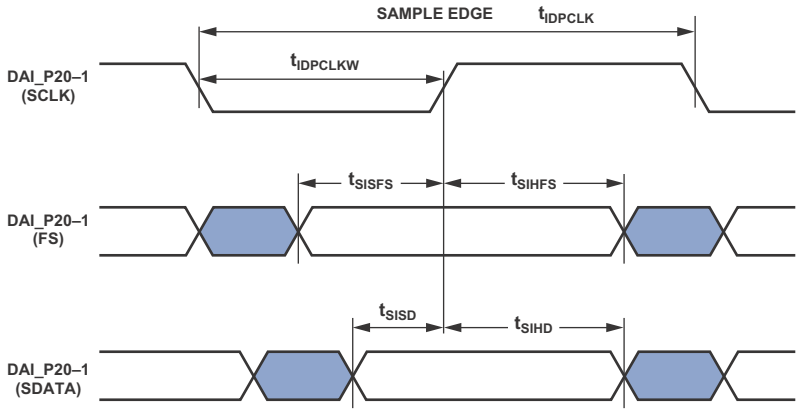



*Figure 30. IDP Master Timing*

### *Parallel Data Acquisition Port (PDAP)*

The timing requirements for the PDAP are provided in Table 43. PDAP is the parallel mode operation of channel 0 of the IDP. For details on the operation of the PDAP, see the PDAP chapter of the *ADSP-214xx SHARC Processor Hardware Reference*.

**Table 43. Parallel Data Acquisition Port (PDAP)**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SPHOLD}$[1] | PDAP_HOLD Setup Before PDAP_CLK Sample Edge | 2.5 | | ns |
| $t_{HPHOLD}$[1] | PDAP_HOLD Hold After PDAP_CLK Sample Edge | 2.5 | | ns |
| $t_{PDSD}$[1] | PDAP_DAT Setup Before Serial Clock PDAP_CLK Sample Edge | 3.85 | | ns |
| $t_{PDHD}$[1] | PDAP_DAT Hold After Serial Clock PDAP_CLK Sample Edge | 2.5 | | ns |
| $t_{PDCLKW}$ | Clock Width | $(t_{PCLK} \times 4) \div 2 - 3$ | | ns |
| $t_{PDCLK}$ | Clock Period | $t_{PCLK} \times 4$ | | ns |
| *Switching Characteristics* | | | | |
| $t_{PDHLDD}$ | Delay of PDAP Strobe After Last PDAP_CLK Capture Edge for a Word | $2 \times t_{PCLK} + 3$ | | ns |
| $t_{PDSTRB}$ | PDAP Strobe Pulse Width | $2 \times t_{PCLK} - 1$ | | ns |

[1] The 20 bits of external PDAP data can be provided through the AMI_ADDR23–4 or DAI pins. Source pins for serial clock and frame sync are 1) AMI_ADDR3–2 pins, 2) DAI pins.

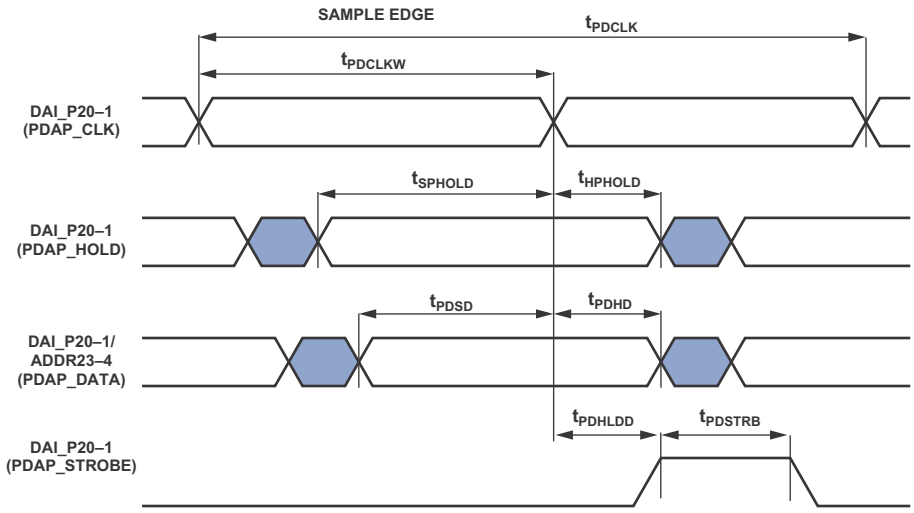



*Figure 31. PDAP Timing*

**Table 49. S/PDIF Transmitter Left-Justified Mode**

| Parameter | | Nominal | Unit |
|---|---|---|---|
| *Timing Requirement* | | | |
| $t_{LJD}$ | LRCLK to MSB Delay in Left-Justified Mode | 0 | SCLK |

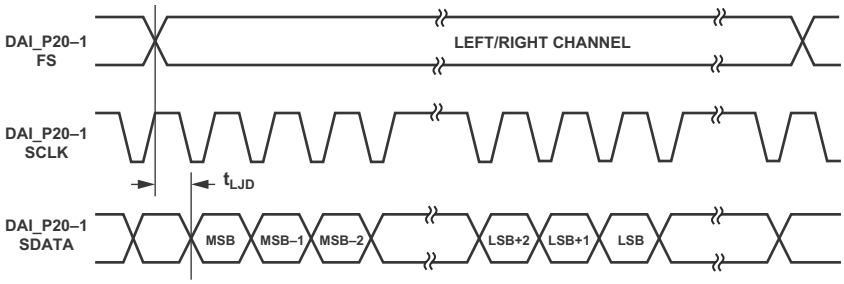



*Figure 37. Left-Justified Mode*

### S/PDIF Transmitter Input Data Timing

The timing requirements for the S/PDIF transmitter are given in Table 50. Input signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

**Table 50. S/PDIF Transmitter Input Data Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SISFS}$[1] | Frame Sync Setup Before Serial Clock Rising Edge | 3 | | ns |
| $t_{SIHFS}$[1] | Frame Sync Hold After Serial Clock Rising Edge | 3 | | ns |
| $t_{SISD}$[1] | Data Setup Before Serial Clock Rising Edge | 3 | | ns |
| $t_{SIHD}$[1] | Data Hold After Serial Clock Rising Edge | 3 | | ns |
| $t_{SITXCLKW}$ | Transmit Clock Width | 9 | | ns |
| $t_{SITXCLK}$ | Transmit Clock Period | 20 | | ns |
| $t_{SISCLKW}$ | Clock Width | 36 | | ns |
| $t_{SISCLK}$ | Clock Period | 80 | | ns |

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. The PCG's input can be either CLKIN or any of the DAI pins.

### *Media Local Bus*

All the numbers given are applicable for all speed modes (1024 FS, 512 FS, and 256 FS for 3-pin; 512 FS and 256 FS for 5-pin) unless otherwise specified. Please refer to MediaLB specification document rev 3.0 for more details.

**Table 55. MLB Interface, 3-Pin Specifications**

| Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| *3-Pin Characteristics* | | | | | |
| $t_{MLBCLK}$ | MLB Clock Period | | | | |
| | 1024 FS | | 20.3 | | ns |
| | 512 FS | | 40 | | ns |
| | 256 FS | | 81 | | ns |
| $t_{MCKL}$ | MLBCLK Low Time | | | | |
| | 1024 FS | 6.1 | | | ns |
| | 512 FS | 14 | | | ns |
| | 256 FS | 30 | | | ns |
| $t_{MCKH}$ | MLBCLK High Time | | | | |
| | 1024 FS | 9.3 | | | ns |
| | 512 FS | 14 | | | ns |
| | 256 FS | 30 | | | ns |
| $t_{MCKR}$ | MLBCLK Rise Time ($V_{IL}$ to $V_{IH}$) | | | | |
| | 1024 FS | | | 1 | ns |
| | 512 FS/256 FS | | | 3 | ns |
| $t_{MCKF}$ | MLBCLK Fall Time ($V_{IH}$ to $V_{IL}$) | | | | |
| | 1024 FS | | | 1 | ns |
| | 512 FS/256 FS | | | 3 | ns |
| $T_{MPWV}$[1] | MLBCLK Pulse Width Variation | | | | |
| | 1024 FS | | | 0.7 | ns p-p |
| | 512 FS/256 FS | | | 2.0 | ns p-p |
| $t_{DSMCF}$ | DAT/SIG Input Setup Time | 1 | | | ns |
| $t_{DHMCF}$ | DAT/SIG Input Hold Time | 1 | | | ns |
| $t_{MCFDZ}$ | DAT/SIG Output Time to Three-state | 0 | | 15 | ns |
| $t_{MCDRV}$ | DAT/SIG Output Data Delay From MLBCLK Rising Edge | | | 8 | ns |
| $t_{MDZH}$[2] | Bus Hold Time | | | | |
| | 1024 FS | 2 | | | ns |
| | 512 FS/256 FS | 4 | | | ns |
| $C_{MLB}$ | DAT/SIG Pin Load | | | | |
| | 1024 FS | | | 40 | pf |
| | 512 FS/256 FS | | | 60 | pf |

[1] Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in nanoseconds peak-to-peak (ns p-p).
[2] The board must be designed to ensure that the high impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

### *JTAG Test Access Port and Emulation*

**Table 57. JTAG Test Access Port and Emulation**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{TCK}$ | TCK Period | 20 | | ns |
| $t_{STAP}$ | TDI, TMS Setup Before TCK High | 5 | | ns |
| $t_{HTAP}$ | TDI, TMS Hold After TCK High | 6 | | ns |
| $t_{SSYS}$[1] | System Inputs Setup Before TCK High | 7 | | ns |
| $t_{HSYS}$[1] | System Inputs Hold After TCK High | 18 | | ns |
| $t_{TRSTW}$ | $\overline{\text{TRST}}$ Pulse Width | $4 \times t_{CK}$ | | ns |
| *Switching Characteristics* | | | | |
| $t_{DTDO}$ | TDO Delay from TCK Low | | 10 | ns |
| $t_{DSYS}$[2] | System Outputs Delay After TCK Low | | $t_{CK} \div 2 + 7$ | ns |

[1] System Inputs = AMI_DATA, DDR2_DATA, CLKCFG1–0, BOOTCFG2–0 RESET, DAI, DPI, FLAG3–0.
[2] System Outputs = AMI_ADDR/DATA, DDR2_ADDR/DATA, AMI_CTRL, DDR2_CTRL, DAI, DPI, FLAG3–0, $\overline{\text{EMU}}$.

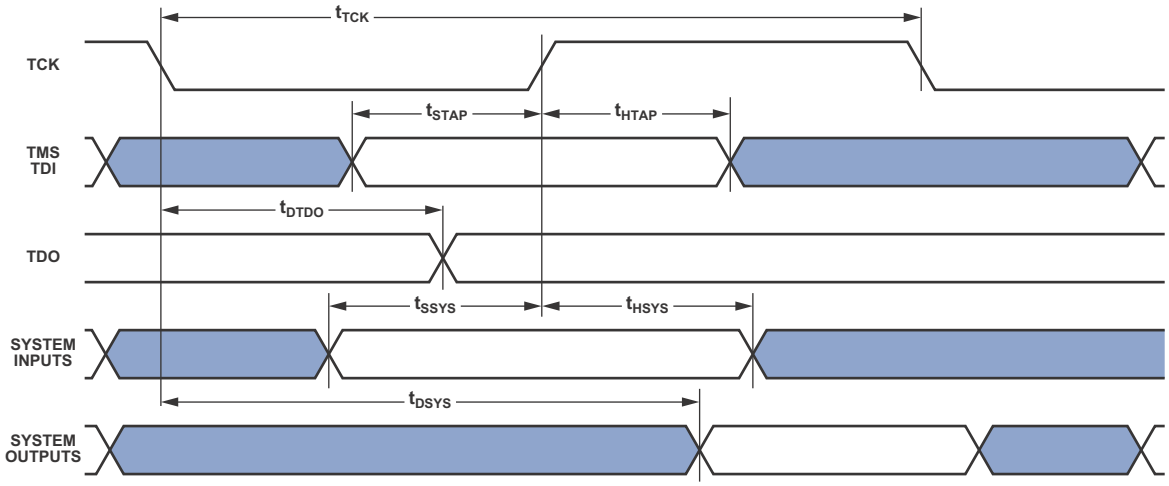



*Figure 45. IEEE 1149.1 JTAG Test Access Port*

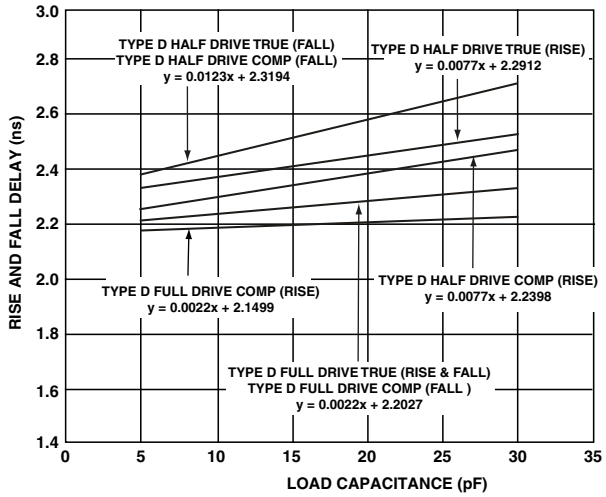



*Figure 57. Typical Output Rise/Fall Delay DDR Pad D ($V_{DD\_EXT}$ = Min)*

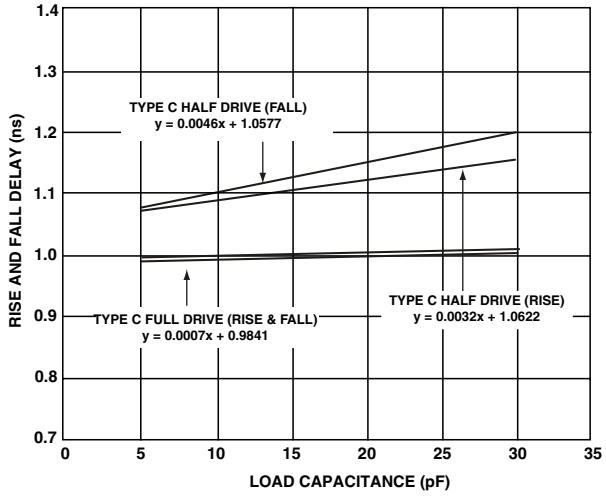



*Figure 58. Typical Output Rise/Fall Delay DDR Pad C ($V_{DD\_EXT}$ = Max)*

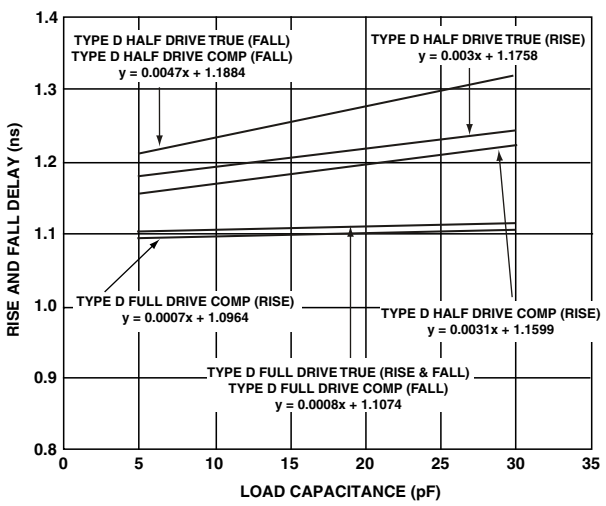



*Figure 59. Typical Output Rise/Fall Delay DDR Pad D ($V_{DD\_EXT}$ = Max)*

## THERMAL CHARACTERISTICS

The processors are rated for performance over the temperature range specified in Operating Conditions on Page 19.

Table 59 airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6, and the junction-to-board measurement complies with JESD51-8. Test board design complies with JEDEC standards JESD51-7 (CSP_BGA). The junction-to-case measurement complies with MIL- STD-883. All measurements use a 2S2P JEDEC test board.

To determine the junction temperature of the device while on the application PCB use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

$T_J$ = junction temperature (°C)

$T_{CASE}$ = case temperature (°C) measured at the top center of the package

$\Psi_{JT}$ = junction-to-top (of package) characterization parameter is the typical value from Table 59.

$P_D$ = power dissipation

Values of $\theta_{JA}$ are provided for package comparison and PCB design considerations. $\theta_{JA}$ can be used for a first order approximation of $T_J$ by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

$T_A$ = ambient temperature °C

Values of $\theta_{JC}$ are provided for package comparison and PCB design considerations when an external heat sink is required.

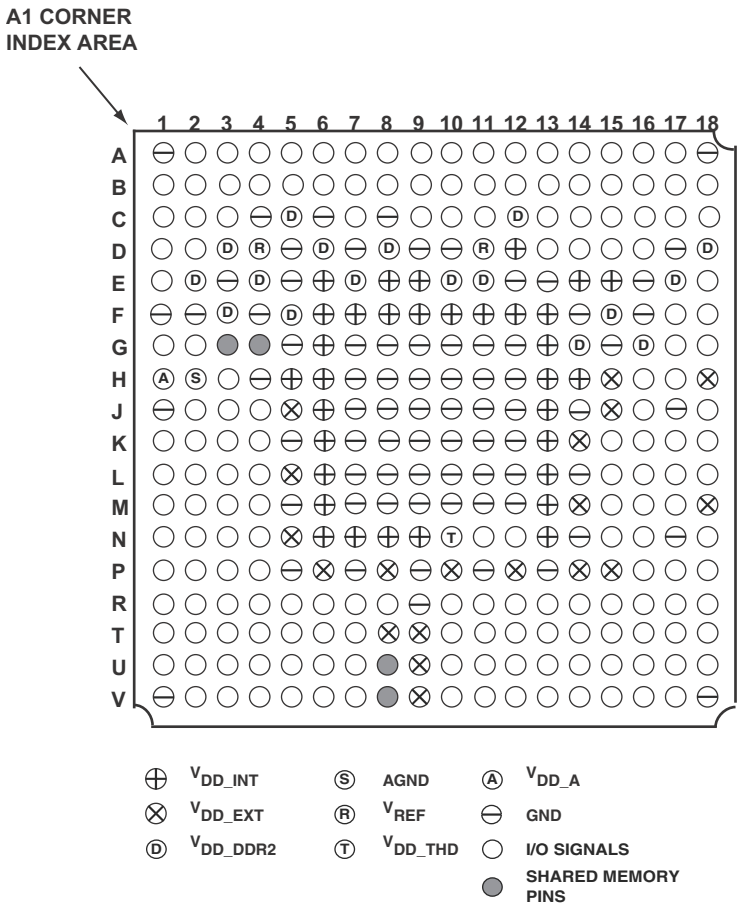



*Figure 60. Ball Configuration, Automotive Model*

# CSP_BGA BALL ASSIGNMENT—STANDARD MODELS

Table 62 lists the standard model CSP_BGA ball assignments by signal.

**Table 62. CSP_BGA Ball Assignment (Alphabetical by Signal)**

| Signal | Ball No. | Signal | Ball No. | Signal | Ball No. | Signal | Ball No. |
|---|---|---|---|---|---|---|---|
| AGND | H02 | BOOT_CFG2 | H03 | DDR2_BA0 | C18 | DPI_P03 | T01 |
| AMI_ACK | R10 | CLK_CFG0 | G01 | DDR2_BA1 | C17 | DPI_P04 | R01 |
| AMI_ADDR0 | V16 | CLK_CFG1 | G02 | DDR2_BA2 | B18 | DPI_P05 | P01 |
| AMI_ADDR01 | U16 | CLKIN | L01 | $\overline{\text{DDR2\_CAS}}$ | C07 | DPI_P06 | P02 |
| AMI_ADDR02 | T16 | DAI_P01 | R06 | DDR2_CKE | E01 | DPI_P07 | P03 |
| AMI_ADDR03 | R16 | DAI_P02 | V05 | $\overline{\text{DDR2\_CLK0}}$ | A07 | DPI_P08 | P04 |
| AMI_ADDR04 | V15 | DAI_P03 | R07 | DDR2_CLK0 | B07 | DPI_P09 | N01 |
| AMI_ADDR05 | U15 | DAI_P04 | R03 | $\overline{\text{DDR2\_CLK1}}$ | A13 | DPI_P10 | N02 |
| AMI_ADDR06 | T15 | DAI_P05 | U05 | DDR2_CLK1 | B13 | DPI_P11 | N03 |
| AMI_ADDR07 | R15 | DAI_P06 | T05 | $\overline{\text{DDR2\_CS0}}$ | C01 | DPI_P12 | N04 |
| AMI_ADDR08 | V14 | DAI_P07 | V06 | $\overline{\text{DDR2\_CS1}}$ | D01 | DPI_P13 | M03 |
| AMI_ADDR09 | U14 | DAI_P08 | V02 | $\overline{\text{DDR2\_CS2}}$ | C02 | DPI_P14 | M04 |
| AMI_ADDR10 | T14 | DAI_P09 | R05 | $\overline{\text{DDR2\_CS3}}$ | D02 | $\overline{\text{EMU}}$ | K02 |
| AMI_ADDR11 | R14 | DAI_P10 | V04 | DDR2_DATA0 | B02 | FLAG0 | R08 |
| AMI_ADDR12 | V13 | DAI_P11 | U04 | DDR2_DATA01 | A02 | FLAG1 | V07 |
| AMI_ADDR13 | U13 | DAI_P12 | T04 | DDR2_DATA02 | B03 | FLAG2 | U07 |
| AMI_ADDR14 | T13 | DAI_P13 | U06 | DDR2_DATA03 | A03 | FLAG3 | T07 |
| AMI_ADDR15 | R13 | DAI_P14 | U02 | DDR2_DATA04 | B05 | GND | A01 |
| AMI_ADDR16 | V12 | DAI_P15 | R04 | DDR2_DATA05 | A05 | GND | A18 |
| AMI_ADDR17 | U12 | DAI_P16 | V03 | DDR2_DATA06 | B06 | GND | C04 |
| AMI_ADDR18 | T12 | DAI_P17 | U03 | DDR2_DATA07 | A06 | GND | C06 |
| AMI_ADDR19 | R12 | DAI_P18 | T03 | DDR2_DATA08 | B08 | GND | C08 |
| AMI_ADDR20 | V11 | DAI_P19 | T06 | DDR2_DATA09 | A08 | GND | D05 |
| AMI_ADDR21 | U11 | DAI_P20 | T02 | DDR2_DATA10 | B09 | GND | D07 |
| AMI_ADDR22 | T11 | DDR2_ADDR0 | D13 | DDR2_DATA11 | A09 | GND | D09 |
| AMI_ADDR23 | R11 | DDR2_ADDR01 | C13 | DDR2_DATA12 | A11 | GND | D10 |
| AMI_DATA0 | U18 | DDR2_ADDR02 | D14 | DDR2_DATA13 | B11 | GND | D17 |
| AMI_DATA1 | T18 | DDR2_ADDR03 | C14 | DDR2_DATA14 | A12 | GND | E03 |
| AMI_DATA2 | R18 | DDR2_ADDR04 | B14 | DDR2_DATA15 | B12 | GND | E05 |
| AMI_DATA3 | P18 | DDR2_ADDR05 | A14 | DDR2_DM0 | C03 | GND | E12 |
| AMI_DATA4 | V17 | DDR2_ADDR06 | D15 | DDR2_DM1 | C11 | GND | E13 |
| AMI_DATA5 | U17 | DDR2_ADDR07 | C15 | DDR2_DQS0 | A04 | GND | E16 |
| AMI_DATA6 | T17 | DDR2_ADDR08 | B15 | $\overline{\text{DDR2\_DQS0}}$ | B04 | GND | F01 |
| AMI_DATA7 | R17 | DDR2_ADDR09 | A15 | DDR2_DQS1 | A10 | GND | F02 |
| $\overline{\text{AMI\_MS0}}$ | T10 | DDR2_ADDR10 | D16 | $\overline{\text{DDR2\_DQS1}}$ | B10 | GND | F04 |
| $\overline{\text{AMI\_MS1}}$ | U10 | DDR2_ADDR11 | C16 | DDR2_ODT | B01 | GND | F14 |
| $\overline{\text{AMI\_RD}}$ | J04 | DDR2_ADDR12 | B16 | $\overline{\text{DDR2\_RAS}}$ | C09 | GND | F16 |
| $\overline{\text{AMI\_WR}}$ | V10 | DDR2_ADDR13 | A16 | $\overline{\text{DDR2\_WE}}$ | C10 | GND | G05 |
| BOOT_CFG0 | J02 | DDR2_ADDR14 | B17 | DPI_P01 | R02 | GND | G07 |
| BOOT_CFG1 | J03 | DDR2_ADDR15 | A17 | DPI_P02 | U01 | GND | G08 |