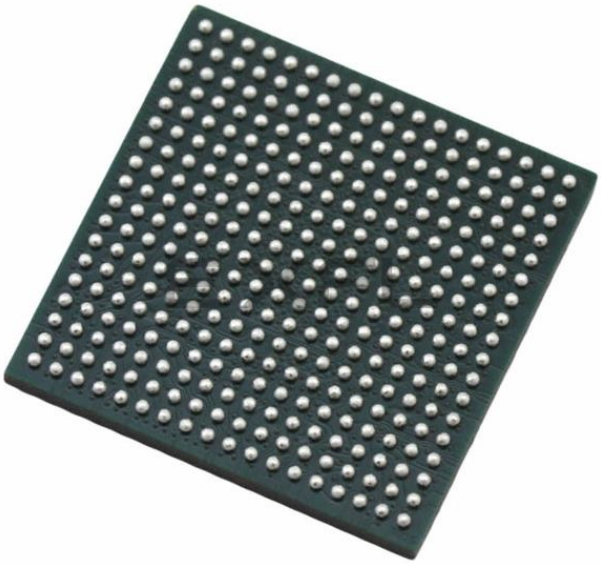

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	DAI, DPI, EBI/EMI, I²C, SCI, SPI, SSP, UART/USART
Clock Rate	400MHz
Non-Volatile Memory	External
On-Chip RAM	5Mbit
Voltage - I/O	3.30V
Voltage - Core	1.05V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	324-BGA, CSPBGA
Supplier Device Package	324-CSPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21469bbcz-3

Using the DM bus and PM buses, with one bus dedicated to a memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

The memory map in Table 3 displays the internal memory address space of the processors. The 48-bit space section describes what this address range looks like to an instruction that retrieves 48-bit memory. The 32-bit section describes what this address range looks like to an instruction that retrieves 32-bit memory.

On-Chip Memory Bandwidth

The internal memory architecture allows programs to have four accesses at the same time to any of the four blocks (assuming there are no block conflicts). The total bandwidth is realized using the DMD and PMD buses (2 × 64-bits, CCLK speed) and the IOD0/1 buses (2 × 32-bit, PCLK speed).

Nonsecured ROM

For nonsecured ROM, booting modes are selected using the BOOTCFG pins as shown in Table 8 on Page 10. In this mode, emulation is always enabled, and the IVT is placed on the internal RAM except for the case where BOOTCFGx = 011.

ROM-Based Security

The ROM security feature provides hardware support for securing user software code by preventing unauthorized reading from the internal code when enabled. When using this feature, the processors do not boot-load any external code, executing exclusively from internal ROM. Additionally, the processors are not freely accessible via the JTAG port. Instead, a unique 64-bit key, which must be scanned in through the JTAG or Test Access Port will be assigned to each customer.

Digital Transmission Content Protection

The DTCP specification defines a cryptographic protocol for protecting audio entertainment content from illegal copying, intercepting, and tampering as it traverses high performance digital buses, such as the IEEE 1394 standard. Only legitimate entertainment content delivered to a source device via another approved copy protection system (such as the DVD content scrambling system) is protected by this copy protection system.

Table 3. Internal Memory Space[1]

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 Bits)	**Extended Precision Normal or Instruction Word (48 Bits)**	**Normal Word (32 Bits)**	**Short Word (16 Bits)**
Block 0 ROM (Reserved) 0x0004 0000–0x0004 7FFF	Block 0 ROM (Reserved) 0x0008 0000–0x0008 AAA9	Block 0 ROM (Reserved) 0x0008 0000–0x0008 FFFF	Block 0 ROM (Reserved) 0x0010 0000–0x0011 FFFF
Reserved 0x0004 8000–0x0004 8FFF	Reserved 0x0008 AAAA–0x0008 BFFF	Reserved 0x0009 0000–0x0009 1FFF	Reserved 0x0012 0000–0x0012 3FFF
Block 0 SRAM 0x0004 9000–0x0004 EFFF	Block 0 SRAM 0x0008 C000–0x0009 3FFF	Block 0 SRAM 0x0009 2000–0x0009 DFFF	Block 0 SRAM 0x0012 4000–0x0013 BFFF
Reserved 0x0004 F000–0x0004 FFFF	Reserved 0x0009 4000–0x0009 FFFF	Reserved 0x0009 E000–0x0009 FFFF	Reserved 0x0013 C000–0x0013 FFFF
Block 1 ROM (Reserved) 0x0005 0000–0x0005 7FFF	Block 1 ROM (Reserved) 0x000A 0000–0x000A AAA9	Block 1 ROM (Reserved) 0x000A 0000–0x000A FFFF	Block 1 ROM (Reserved) 0x0014 0000–0x0015 FFFF
Reserved 0x0005 8000–0x0005 8FFF	Reserved 0x000A AAAA–0x000A BFFF	Reserved 0x000B 0000–0x000B 1FFF	Reserved 0x0016 0000–0x0016 3FFF
Block 1 SRAM 0x0005 9000–0x0005 EFFF	Block 1 SRAM 0x000A C000–0x000B 3FFF	Block 1 SRAM 0x000B 2000–0x000B DFFF	Block 1 SRAM 0x0016 4000–0x0017 BFFF
Reserved 0x0005 F000–0x0005 FFFF	Reserved 0x000B 4000–0x000B FFFF	Reserved 0x000B E000–0x000B FFFF	Reserved 0x0017 C000–0x0017 FFFF
Block 2 SRAM 0x0006 0000–0x0006 3FFF	Block 2 SRAM 0x000C 0000–0x000C 5554	Block 2 SRAM 0x000C 0000–0x000C 7FFF	Block 2 SRAM 0x0018 0000–0x0018 FFFF
Reserved 0x0006 4000– 0x0006 FFFF	Reserved 0x000C 5555–0x000D FFFF	Reserved 0x000C 8000–0x000D FFFF	Reserved 0x0019 0000–0x001B FFFF
Block 3 SRAM 0x0007 0000–0x0007 3FFF	Block 3 SRAM 0x000E 0000–0x000E 5554	Block 3 SRAM 0x000E 0000–0x000E 7FFF	Block 3 SRAM 0x001C 0000–0x001C FFFF
Reserved 0x0007 4000–0x0007 FFFF	Reserved 0x000E 5555–0x0000F FFFF	Reserved 0x000E 8000–0x000F FFFF	Reserved 0x001D 0000–0x001F FFFF

[1] Some processors include a customer-definable ROM block. ROM addresses on these models are not reserved as shown in this table. Please contact your Analog Devices sales representative for additional details.

Table 10. Pin Descriptions (Continued)

Name	Type	State During/ After Reset	Description
$DDR2\_ADDR_{15-0}$	O/T	High-Z/ driven low	**DDR2 Address.** DDR2 address pins.
$DDR2\_BA_{2-0}$	O/T	High-Z/ driven low	**DDR2 Bank Address Input.** Defines which internal bank an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied to. BA_{2-0}define which mode registers, including MR, EMR, EMR(2), and EMR(3) are loaded during the LOAD MODE REGISTER command.
$\overline{DDR2\_CAS}$	O/T	High-Z/ driven high	**DDR2 Column Address Strobe.** Connect to $\overline{DDR2\_CAS}$ pin; in conjunction with other DDR2 command pins, defines the operation for the DDR2 to perform.
DDR2_CKE	O/T	High-Z/ driven low	**DDR2 Clock Enable Output to DDR2.** Active high signal. Connect to DDR2 CKE signal.
$\overline{DDR2\_CS_{3-0}}$	O/T	High-Z/ driven high	**DDR2 Chip Select.** All commands are masked when $\overline{DDR2\_CS_{3-0}}$ is driven high. $\overline{DDR2\_CS_{3-0}}$ are decoded memory address lines. Each $\overline{DDR2\_CS_{3-0}}$ line selects the corresponding external bank.
$DDR2\_DATA_{15-0}$	I/O/T	High-Z	**DDR2 Data In/Out.** Connect to corresponding DDR2_DATA pins.
$DDR2\_DM_{1-0}$	O/T	High-Z/ driven high	**DDR2 Input Data Mask.** Mask for the DDR2 write data if driven high. Sampled on both edges of DDR2_DQS at DDR2 side. DM0 corresponds to DDR2_DATA 7–0 and DM1 corresponds to DDR2_DATA15–8.
$DDR2\_DQS_{1-0}$ $\overline{DDR2\_DQS_{1-0}}$	I/O/T (Differential)	High-Z	**Data Strobe.** Output with Write Data. Input with Read Data. DQS0 corresponds to DDR2_DATA 7–0 and DQS1 corresponds to DDR2_DATA 15–8. Based on software control via the DDR2CTL3 register, this pin can be single-ended or differential.
$\overline{DDR2\_RAS}$	O/T	High-Z/ driven high	**DDR2 Row Address Strobe.** Connect to $\overline{DDR2\_RAS}$ pin; in conjunction with other DDR2 command pins, defines the operation for the DDR2 to perform.
$\overline{DDR2\_WE}$	O/T	High-Z/ driven high	**DDR2 Write Enable.** Connect to $\overline{DDR2\_WE}$ pin; in conjunction with other DDR2 command pins, defines the operation for the DDR2 to perform.
DDR2_CLK0, $\overline{DDR2\_CLK0}$, DDR2_CLK1, $\overline{DDR2\_CLK1}$	O/T (Differential)	High-Z/ driven low	**DDR2 Memory Clocks.** Two differential outputs available via software control (DDR2CTL0 register). Free running, minimum frequency not guaranteed during reset.
DDR2_ODT	O/T	High-Z/ driven low	**DDR2 On Die Termination.** ODT pin when driven high (along with other requirements) enables the DDR2 termination resistances. ODT is enabled/disabled regardless of read or write commands.

The following symbols appear in the Type column of Table 10: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open-drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26 kΩ–63 kΩ. The range of an ipd resistor can be between 31 kΩ–85 kΩ. The three-state voltage of ipu pads will not reach to full the V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.
In this table, the DDR2 pins are SSTL18 compliant. All other pins are LVTTL compliant.

Table 10. Pin Descriptions (Continued)

Name	Type	State During/ After Reset	Description
$\overline{\text{RESET}}$	I		**Processor Reset.** Resets the processor to a known state. Upon deassertion, there is a 4096 CLKIN cycle latency for the PLL to lock. After this time, the core begins program execution from the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
$\overline{\text{RESETOUT}}$/ $\overline{\text{RUNRSTIN}}$	I/O (ipu)		**Reset Out/Running Reset In.** The default setting on this pin is reset out. This pin also has a second function as RUNRSTIN which is enabled by setting bit 0 of the RUNRSTCTL register. For more information, see the *ADSP-214xx SHARC Processor Hardware Reference*.
BOOT_CFG_{2-0}	I		**Boot Configuration Select.** These pins select the boot mode for the processor. The BOOT_CFG pins must be valid before $\overline{\text{RESET}}$ (hardware and software) is de-asserted.

The following symbols appear in the Type column of Table 10: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open-drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26 kΩ–63 kΩ. The range of an ipd resistor can be between 31 kΩ–85 kΩ. The three-state voltage of ipu pads will not reach to full the V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.
In this table, the DDR2 pins are SSTL18 compliant. All other pins are LVTTL compliant.

Table 11. Pin List, Power and Ground

Name	Type	Description
V_{DD_INT}	P	Internal Power
V_{DD_EXT}	P	External Power
V_{DD_A}	P	Analog Power for PLL
V_{DD_THD}	P	Thermal Diode Power; if thermal diode is not used then this pin can be left floating
V_{DD_DDR2}[1]	P	DDR2 Interface Power
V_{REF}	P	DDR2 Input Voltage Reference
GND	G	Ground
AGND	G	Analog Ground

[1] Applies to DDR2 signals.

ELECTRICAL CHARACTERISTICS

Parameter[1]	Description	Test Conditions	450 MHz Min	450 MHz Max	400 MHz Min	400 MHz Max	Unit
V_{OH}[2]	High Level Output Voltage	@ V_{DD_EXT} = Min, I_{OH} = –1.0 mA[3]	2.4		2.4		V
V_{OL}[2]	Low Level Output Voltage	@ V_{DD_EXT} = Min, I_{OL} = 1.0 mA[3]		0.4		0.4	V
V_{OH_DDR2}	High Level Output Voltage for DDR2	@ V_{DD_DDR} = Min, I_{OH} = –13.4 mA	1.4		1.4		V
V_{OL_DDR2}	Low Level Output Voltage for DDR2	@ V_{DD_DDR} = Min, IOL = 13.4 mA		0.29		0.29	V
I_{IH}[4, 5]	High Level Input Current	@ V_{DD_EXT} = Max, V_{IN} = V_{DD_EXT} Max		10		10	µA
I_{IL}[4, 6]	Low Level Input Current	@ V_{DD_EXT} = Max, V_{IN} = 0 V		10		10	µA
I_{ILPU}[5]	Low Level Input Current Pull-up	@ V_{DD_EXT} = Max, V_{IN} = 0 V		200		200	µA
I_{IHPD}[6]	High Level Input Current Pull-down	@ V_{DD_EXT} = Max, V_{IN} = V_{DD_EXT} Max		200		200	µA
I_{OZH}[7, 8]	Three-State Leakage Current	@ V_{DD_EXT}/V_{DD_DDR} = Max, V_{IN} = V_{DD_EXT}/V_{DD_DDR} Max		10		10	µA
I_{OZL}[7, 9]	Three-State Leakage Current	@ V_{DD_EXT}/V_{DD_DDR} = Max, V_{IN} = 0 V		10		10	µA
I_{OZLPU}[8]	Three-State Leakage Current Pull-up	@ V_{DD_EXT} = Max, V_{IN} = 0 V		200		200	µA
I_{OZHPD}[9]	Three-State Leakage Current Pull-down	@ V_{DD_EXT} = Max, V_{IN} = V_{DD_EXT} Max		200		200	µA
I_{DD_INT}[10]	Supply Current (Internal)	f_{CCLK} > 0 MHz		Table 13 + Table 14 × ASF		Table 13 + Table 14 × ASF	mA
I_{DD_A}[11]	Supply Current (Analog)	V_{DD_A} = Max		10		10	mA
C_{IN}[12, 13]	Input Capacitance	T_{CASE} = 25°C		5		5	pF

[1] Specifications subject to change without notice.
[2] Applies to output and bidirectional pins: AMI_ADDR23-0, AMI_DATA7-0, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, FLAG3–0, DAI_Px, DPI_Px, $\overline{\text{EMU}}$, TDO.
[3] See Output Drive Currents on Page 62 for typical drive current capabilities.
[4] Applies to input pins: BOOTCFGx, CLKCFGx, TCK, $\overline{\text{RESET}}$, CLKIN.
[5] Applies to input pins with internal pull-ups: $\overline{\text{TRST}}$, TMS, TDI.
[6] Applies to input pins with internal pull-downs: MLBCLK
[7] Applies to three-statable pins: all DDR2 pins.
[8] Applies to three-statable pins with pull-ups: DAI_Px, DPI_Px, $\overline{\text{EMU}}$.
[9] Applies to three-statable pins with pull-downs: MLBDAT, MLBSIG, MLBDO, MLBSO, LDAT07-0, LDAT17-0, LCLK0, LCLK1, LACK0, LACK1.
[10] See Engineer-to-Engineer Note EE-348 “Estimating Power Dissipation for ADSP-214xx SHARC Processors” for further information.
[11] Characterized but not tested.
[12] Applies to all signal pins.
[13] Guaranteed, but not tested.

Table 14. Dynamic Current in CCLK Domain—$I_{DD\_INT\_DYNAMIC}$ (mA, with ASF = 1.0)[1]

f_{CCLK} (MHz)[2]	V_{DD_INT}(V)[2]				
	0.95 V	**1.0 V**	**1.05 V**	**1.10 V**	**1.15 V**
100	78	82	86	91	98
150	115	121	130	136	142
200	150	159	169	177	188
250	186	197	208	219	231
300	222	236	249	261	276
350	259	275	288	304	319
400	293	309	328	344	361
450	N/A	N/A	366	385	406

[1] The values are not guaranteed as standalone maximum specifications. They must be combined with static current per the equations of Electrical Characteristics on Page 20.
[2] Valid frequency and voltage ranges are model-specific. See Operating Conditions on Page 19.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 15 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 15. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DD_INT})	–0.3 V to +1.32 V
Analog (PLL) Supply Voltage (V_{DD_A})	–0.3 V to +1.15 V
External (I/O) Supply Voltage (V_{DD_EXT})	–0.3 V to +3.6 V
Thermal Diode Supply Voltage (V_{DD_THD})	–0.3 V to +3.6 V
DDR2 Controller Supply Voltage (V_{DD_DDR2})	–0.3 V to +1.9 V
DDR2 Input Voltage	–0.3 V to +1.9 V
Input Voltage	–0.3 V to +3.6 V
Output Voltage Swing	–0.3 V to V_{DD_EXT} +0.5 V
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased	125°C

PACKAGE INFORMATION

The information presented in Figure 4 and Table 16 provides details about the package branding for the processor. For a complete listing of product availability, see Ordering Guide on Page 74.

Figure 4. Typical Package Brand

Table 16. Package Brand Information[1]

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Option
cc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

[1] Non-automotive only. For branding information specific to automotive products, contact Analog Devices, Inc.

Clock Input

Table 19. Clock Input

Parameter		400 MHz[1] Min	400 MHz[1] Max	450 MHz[2] Min	450 MHz[2] Max	Unit
Timing Requirements						
t_{CK}	CLKIN Period	15[3]	100	13.26	100	ns
t_{CKL}	CLKIN Width Low	7.5	45	6.63	45	ns
t_{CKH}	CLKIN Width High	7.5	45	6.63	45	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		3[4]		3[4]	ns
t_{CCLK}[5]	CCLK Period	2.5	10	2.22	10	ns
f_{VCO}[6]	VCO Frequency	200	900	200	900	MHz
t_{CKJ}[7, 8]	CLKIN Jitter Tolerance	–250	+250	–250	+250	ps

[1] Applies to all 400 MHz models. See Ordering Guide on Page 74.
[2] Applies to all 450 MHz models. See Ordering Guide on Page 74.
[3] Applies only for CLK_CFG1–0 = 00 and default values for PLL control bits in PMCTL.
[4] Guaranteed by simulation but not tested on silicon.
[5] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{CCLK}.
[6] See Figure 5 on Page 24 for VCO diagram.
[7] Actual input jitter should be combined with ac specifications for accurate timing analysis.
[8] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

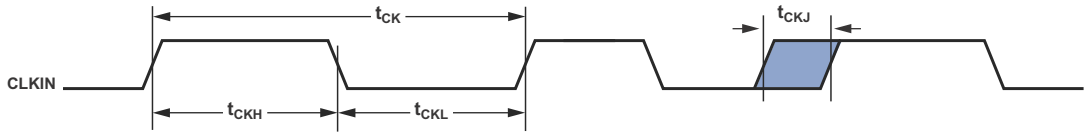


Figure 7. Clock Input

Clock Signals

The processor can use an external clock or a crystal. See the CLKIN pin description in Table 10. Programs can configure the processor to use its internal clock generator by connecting the necessary components to CLKIN and XTAL. Figure 8 shows the component connections used for a crystal operating in fundamental mode. Note that the clock rate is achieved using a 25 MHz crystal and a PLL multiplier ratio 16:1 (CCLK:CLKIN achieves a clock speed of 400 MHz).

To achieve the full core clock rate, programs need to configure the multiplier bits in the PMCTL register.

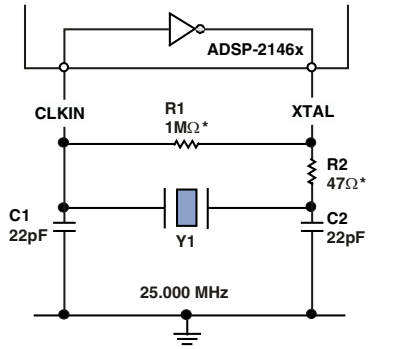


Figure 8. Recommended Circuit for Fundamental Mode Crystal Operation

Precision Clock Generator (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's inputs and outputs are not directly routed to/from DAI pins (via pin buffers) there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P01 – DAI_P20).

Table 27. Precision Clock Generator (Direct Pin Routing)

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCGIW}	Input Clock Period	$t_{PCLK} \times 4$		ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	4.5		ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	3		ns
Switching Characteristics				
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	2.5	10	ns
$t_{DTRIGCLK}$	PCG Output Clock Delay After PCG Trigger	$2.5 + (2.5 \times t_{PCGIP})$	$10 + (2.5 \times t_{PCGIP})$	ns
$t_{DTRIGFS}$	PCG Frame Sync Delay After PCG Trigger	$2.5 + ((2.5 + D - PH) \times t_{PCGIP})$	$10 + ((2.5 + D - PH) \times t_{PCGIP})$	ns
t_{PCGOW}[1]	Output Clock Period	$2 \times t_{PCGIP} - 1$		ns

D = FSxDIV, PH = FSxPHASE. For more information, see the ADSP-214xx SHARC Processor Hardware Reference, "Precision Clock Generators" chapter.

[1] Normal mode of operation.

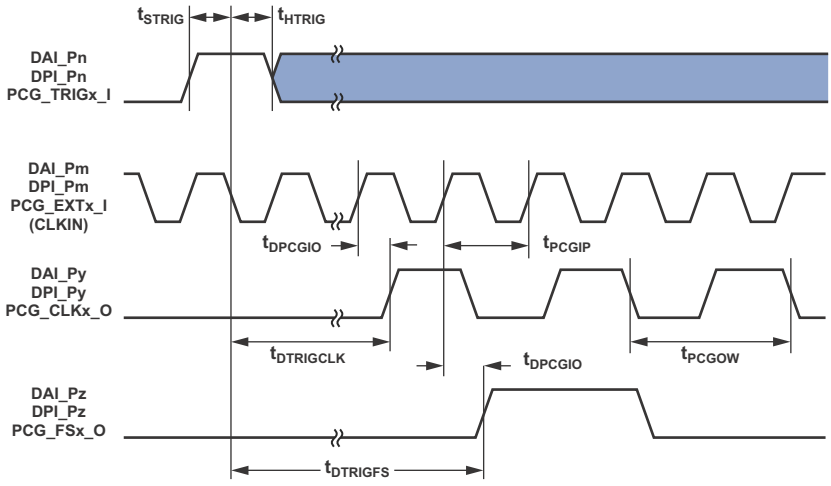


Figure 16. Precision Clock Generator (Direct Pin Routing)

DDR2 SDRAM Read Cycle Timing

Table 29. DDR2 SDRAM Read Cycle Timing, V_{DD_DDR2} Nominal 1.8 V

Parameter		200 MHz[1] Min	200 MHz[1] Max	225 MHz[1] Min	225 MHz[1] Max	Unit
Timing Requirements						
t_{AC}	Access Window of DDR2_DATA to DDR2_CLKx/$\overline{\text{DDR2\_CLKx}}$	–1.0	1.5	–1.0	1.5	ns
t_{DQSCK}	Access Window of DDR2_DQSx/$\overline{\text{DDR2\_DQSx}}$ to DDR2_CLKx/$\overline{\text{DDR2\_CLKx}}$	–1.0	1.5	–1.0	1.5	ns
t_{DQSQ}	DQS-DATA skew for DDR2_DQSx and Associated DDR2_DATA signals		0.450		0.450	ns
t_{QH}	DDR2_DATA Hold Time From DDR2_DQSx/$\overline{\text{DDR2\_DQSx}}$	1.9		1.71		ns
t_{RPRE}	Read Preamble	0.6		0.6		t_{CK}
t_{RPST}	Read Postamble	0.25		0.25		t_{CK}
Switching Characteristics						
t_{CK}	DDR2_CLKx/$\overline{\text{DDR2\_CLKx}}$ Period	4.8		4.22		ns
t_{CH}	DDR2_CLKx High Pulse Width	2.35	2.75	2.05	2.45	ns
t_{CL}	DDR2_CLKx Low Pulse Width	2.35	2.75	2.05	2.45	ns
t_{AS}	DDR2_ADDR and Control Setup Time Relative to DDR2_CLKx Rising	1.85		1.65		ns
t_{AH}	DDR2_ADDR and Control Hold Time Relative to DDR2_CLKx Rising	1.0		0.9		ns

[1] In order to ensure proper operation of the DDR2, all the DDR2 guidelines have to be strictly followed (see Engineer-to-Engineer Note EE-349).

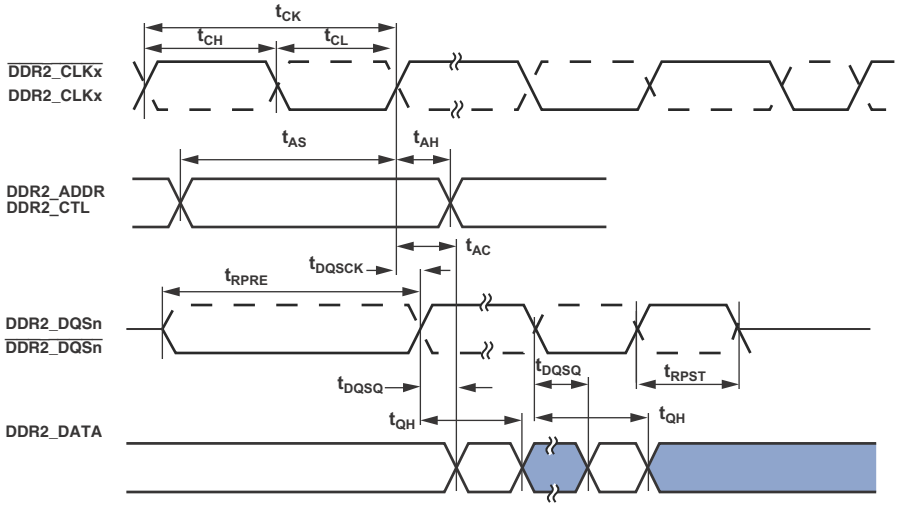


Figure 18. DDR2 SDRAM Controller Input AC Timing

AMI Write

Use these specifications for asynchronous interfacing to memories. Note that timing for AMI_ACK, AMI_DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.

Table 32. Memory Write

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAAK}	AMI_ACK Delay from Address, Selects[1, 2]		t_{DDR2_CLK} – 9.7 + W	ns
t_{DSAK}	AMI_ACK Delay from $\overline{\text{AMI\_WR}}$ Low [1, 3]		W – 6	ns
Switching Characteristics				
t_{DAWH}	Address, Selects to $\overline{\text{AMI\_WR}}$ Deasserted[2]	t_{DDR2_CLK} – 3.1 + W		ns
t_{DAWL}	Address, Selects to $\overline{\text{AMI\_WR}}$ Low[2]	t_{DDR2_CLK} – 3		ns
t_{WW}	$\overline{\text{AMI\_WR}}$ Pulse Width	W – 1.3		ns
t_{DDWH}	Data Setup Before $\overline{\text{AMI\_WR}}$ High	t_{DDR2_CLK} – 3.0 + W		ns
t_{DWHA}	Address Hold After $\overline{\text{AMI\_WR}}$ Deasserted	H + 0.15		ns
t_{DWHD}	Data Hold After $\overline{\text{AMI\_WR}}$ Deasserted	H		ns
t_{DATRWH}	Data Disable After $\overline{\text{AMI\_WR}}$ Deasserted[4]	t_{DDR2_CLK} – 1.37 + H	t_{DDR2_CLK} + 4.9 + H	ns
t_{WWR}	$\overline{\text{AMI\_WR}}$ High to $\overline{\text{AMI\_WR}}$ Low[5]	t_{DDR2_CLK} – 1.5 + H		ns
t_{DDWR}	Data Disable Before $\overline{\text{AMI\_RD}}$ Low	$2t_{DDR2\_CLK}$ – 6		ns
t_{WDE}	$\overline{\text{AMI\_WR}}$ Low to Data Enabled	t_{DDR2_CLK} – 3.5		ns
W = (number of wait states specified in AMICTLx register) × t_{DDR2_CLK}, H = (number of hold cycles specified in AMICTLx register) × t_{DDR2_CLK}				

[1] AMI_ACK delay/setup: System must meet t_{DAAK}, or t_{DSAK}, for deassertion of AMI_ACK (low).
[2] The falling edge of $\overline{\text{AMI\_MSx}}$ is referenced.
[3] Note that timing for AMI_ACK, AMI_DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only applies to asynchronous access mode.
[4] See Test Conditions on Page 62 for calculation of hold times given capacitive and dc loads.
[5] For Write to Write: t_{DDR2_CLK} + H, for both same bank and different bank. For Write to Read: (3 × t_{DDR2_CLK}) + H, for the same bank and different banks.

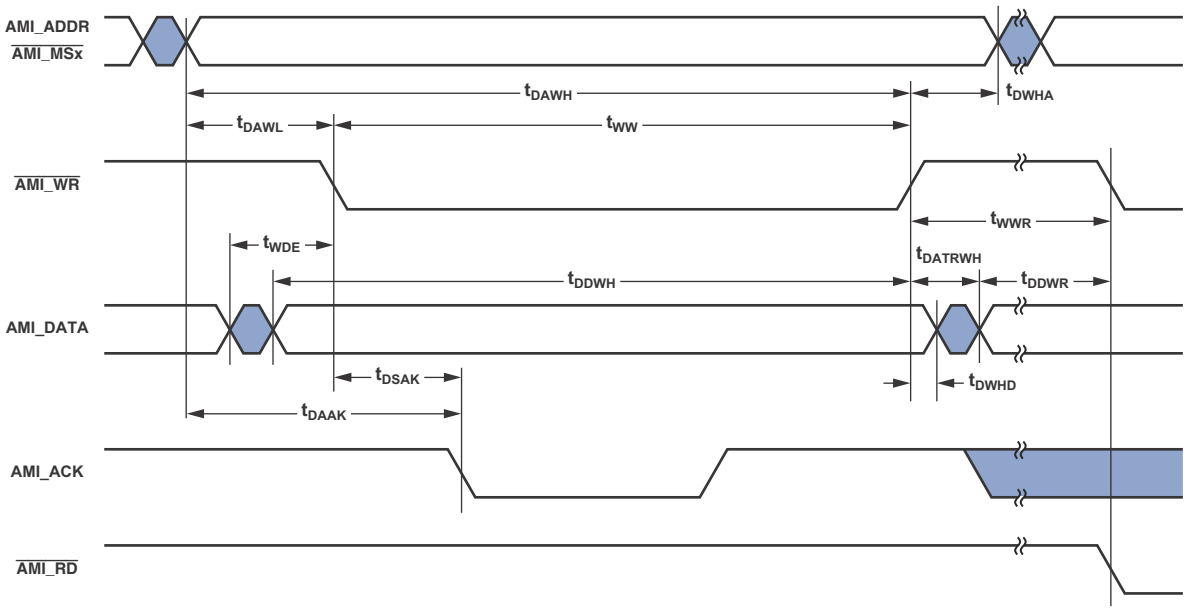


Figure 21. AMI Write

Shared Memory Bus Request

Use these specifications for passing bus mastership between processors ($\overline{BRx}$).

Table 33. Shared Memory Bus Request

Parameter		Min	Max	Unit
Timing Requirements				
t_{SBRI}	$\overline{BRx}$, Setup Before CLKIN High	$2 \times t_{PCLK} + 4$		ns
t_{HBRI}	$\overline{BRx}$, Hold After CLKIN High	5		ns
Switching Characteristics				
t_{DBRO}	$\overline{BRx}$ Delay After CLKIN High		20	ns
t_{HBRO}	$\overline{BRx}$ Hold After CLKIN High	$1 - t_{PCLK}$		ns

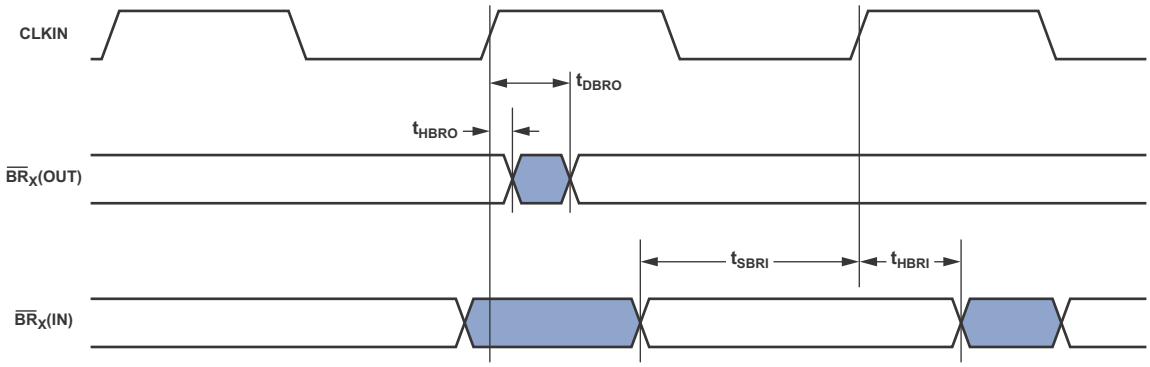


Figure 22. Shared Memory Bus Request

Link Ports

Calculation of link receiver data setup and hold relative to link clock is required to determine the maximum allowable skew that can be introduced in the transmission path length difference between LDATA and LCLK. Setup skew is the maximum delay that can be introduced in LDATA relative to LCLK: (setup skew = $t_{LCLKTWH}$ min – t_{DLDCH} – t_{SLDCL}). Hold skew is the maximum delay that can be introduced in LCLK relative to LDATA: (hold skew = $t_{LCLKTWL}$ min – t_{HLDCH} – t_{HLDCL}).

Table 34. Link Ports—Receive

Parameter		Min	Max	Unit
Timing Requirements				
t_{SLDCL}	Data Setup Before LCLK Low	0.5		ns
t_{HLDCL}	Data Hold After LCLK Low	1.5		ns
t_{LCLKIW}	LCLK Period	t_{LCLK} (6 ns)		ns
$t_{LCLKRWL}$	LCLK Width Low	2.6		ns
$t_{LCLKRWH}$	LCLK Width High	2.6		ns
Switching Characteristics				
t_{DLALC}	LACK Low Delay After LCLK Low[1]	5	12	ns

[1] LACK goes low with t_{DLALC} relative to the fall of LCLK after first byte, but does not go low if the receiver's link buffer is not about to fill.

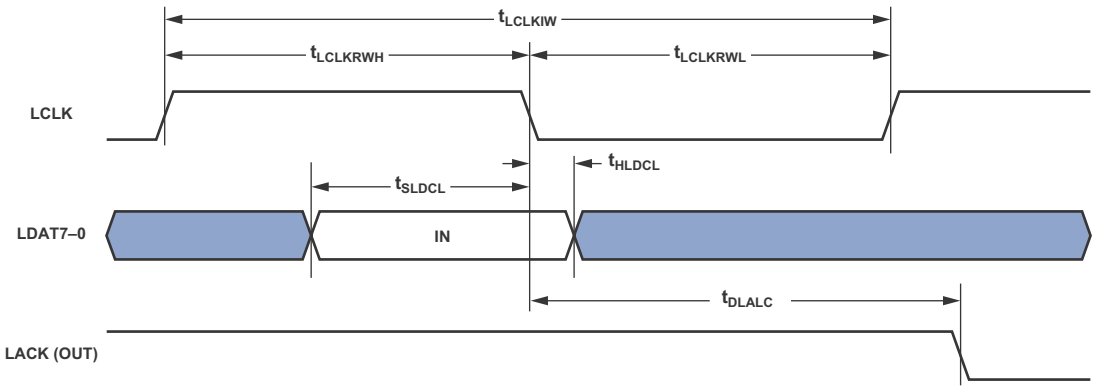


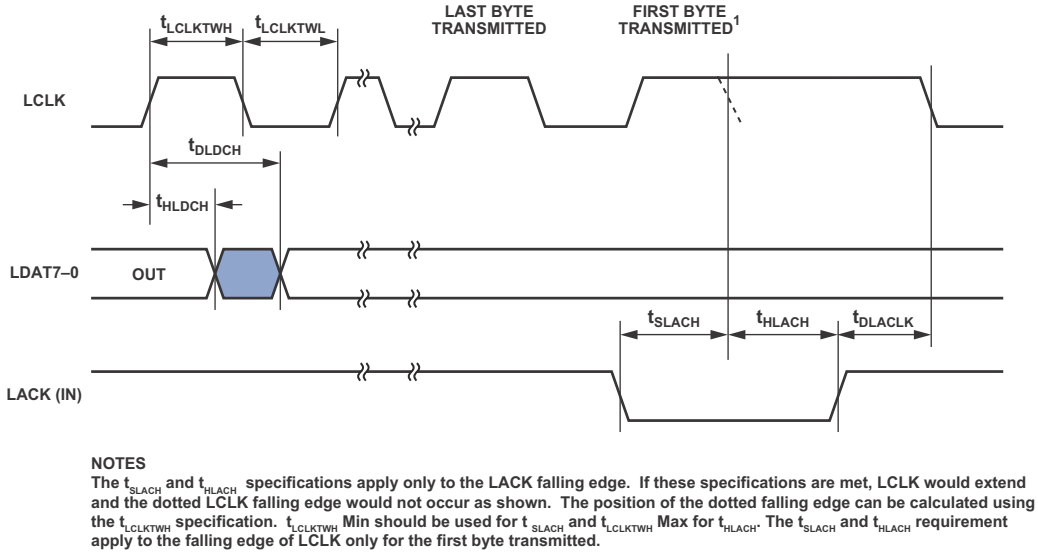
Figure 23. Link Ports—Receive

The data in Table 35 and timing information in Figure 24 apply when the LSYNC_EN bit (bit 6 in the LCTLx register) is cleared.

Table 35. Link Ports—Transmit (Bit 6 Cleared)

Parameter		Min	Max	Unit
Timing Requirements				
t_{SLACH}	LACK Setup Before LCLK Low	8.5		ns
t_{HLACH}	LACK Hold After LCLK Low	0		ns
Switching Characteristics				
t_{DLDCH}	Data Delay After LCLK High		1	ns
t_{HLDCH}	Data Hold After LCLK High	–1		ns
$t_{LCLKTWL}$	LCLK Width Low	$0.5 \times t_{LCLK} - 0.4$	$0.6 \times t_{LCLK} + 0.4$[1]	ns
$t_{LCLKTWH}$	LCLK Width High	$0.4 \times t_{LCLK} - 0.4$[1]	$0.5 \times t_{LCLK} + 0.4$	ns
t_{DLACLK}	LCLK Low Delay After LACK High	4	$t_{LCLK} + 8$	ns

[1] For 1:2.5 ratio. For other ratios this specification is $0.5 \times t_{LCLK} - 1$.



NOTES
The t_{SLACH} and t_{HLACH} specifications apply only to the LACK falling edge. If these specifications are met, LCLK would extend and the dotted LCLK falling edge would not occur as shown. The position of the dotted falling edge can be calculated using the $t_{LCLKTWH}$ specification. $t_{LCLKTWH}$ Min should be used for t_{SLACH} and $t_{LCLKTWH}$ Max for t_{HLACH}. The t_{SLACH} and t_{HLACH} requirement apply to the falling edge of LCLK only for the first byte transmitted.

Figure 24. Link Ports—Transmit (Bit 6 Cleared)

The data in Table 36 and timing information in Figure 25 apply when the LSYNC_EN bit (bit 6 in the LCTLx register) is set.

Table 36. Link Ports—Transmit (Bit 6 Set)

Parameter		Min	Max	Unit
Timing Requirements				
t_{SLACH}	LACK Setup Before LCLK High	8.5		ns
t_{HLACH}	LACK Hold After LCLK High	0		ns
Switching Characteristics				
t_{DLDCH}	Data Delay After LCLK High		1	ns
t_{HLDCH}	Data Hold After LCLK High	–1		ns
$t_{LCLKTWL}$	LCLK Width Low	$0.5 \times t_{LCLK} - 0.4$	$0.6 \times t_{LCLK} + 0.4$[1]	ns
$t_{LCLKTWH}$	LCLK Width High	$0.4 \times t_{LCLK} - 0.4$[1]	$0.5 \times t_{LCLK} + 0.4$	ns
t_{DLACLK}	LCLK Low Delay After LACK High	$0.5 \times t_{LCLK} + 4$	$1.5 \times t_{LCLK} + 4$	ns

[1] For 1:2.5 ratio. For other ratios this specification is $0.5 \times t_{LCLK} - 1$.

Table 39. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DDTEN}[1]	Data Enable from External Transmit SCLK	2		ns
t_{DDTTE}[1]	Data Disable from External Transmit SCLK		11.5	ns
t_{DDTIN}[1]	Data Enable from Internal Transmit SCLK	–1		ns

[1] Referenced to drive edge.

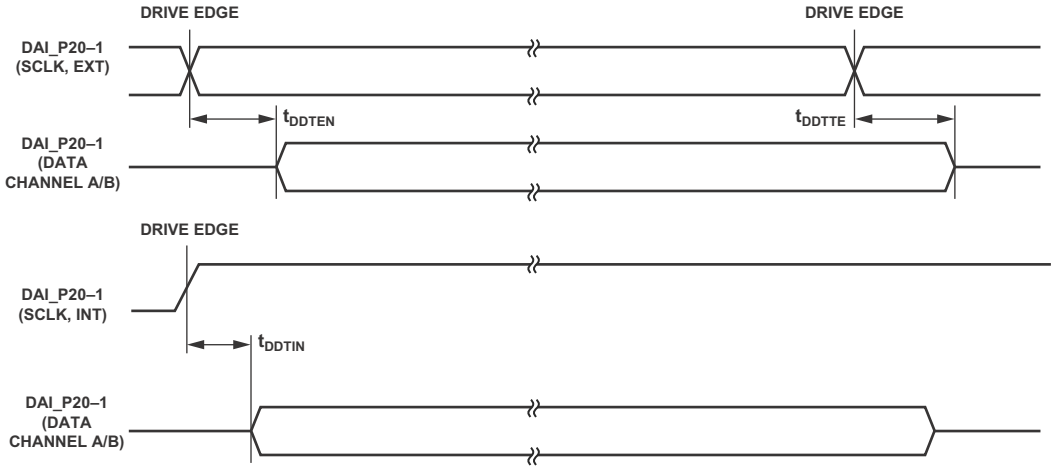


Figure 27. Serial Ports—Enable and Three-State

Parallel Data Acquisition Port (PDAP)

The timing requirements for the PDAP are provided in Table 43. PDAP is the parallel mode operation of channel 0 of the IDP. For details on the operation of the PDAP, see the PDAP chapter of the *ADSP-214xx SHARC Processor Hardware Reference*.

Table 43. Parallel Data Acquisition Port (PDAP)

Parameter		Min	Max	Unit
Timing Requirements				
t_{SPHOLD}[1]	PDAP_HOLD Setup Before PDAP_CLK Sample Edge	2.5		ns
t_{HPHOLD}[1]	PDAP_HOLD Hold After PDAP_CLK Sample Edge	2.5		ns
t_{PDSD}[1]	PDAP_DAT Setup Before Serial Clock PDAP_CLK Sample Edge	3.85		ns
t_{PDHD}[1]	PDAP_DAT Hold After Serial Clock PDAP_CLK Sample Edge	2.5		ns
t_{PDCLKW}	Clock Width	$(t_{PCLK} \times 4) \div 2 - 3$		ns
t_{PDCLK}	Clock Period	$t_{PCLK} \times 4$		ns
Switching Characteristics				
t_{PDHLDD}	Delay of PDAP Strobe After Last PDAP_CLK Capture Edge for a Word	$2 \times t_{PCLK} + 3$		ns
t_{PDSTRB}	PDAP Strobe Pulse Width	$2 \times t_{PCLK} - 1$		ns

[1] The 20 bits of external PDAP data can be provided through the AMI_ADDR23–4 or DAI pins. Source pins for serial clock and frame sync are 1) AMI_ADDR3–2 pins, 2) DAI pins.

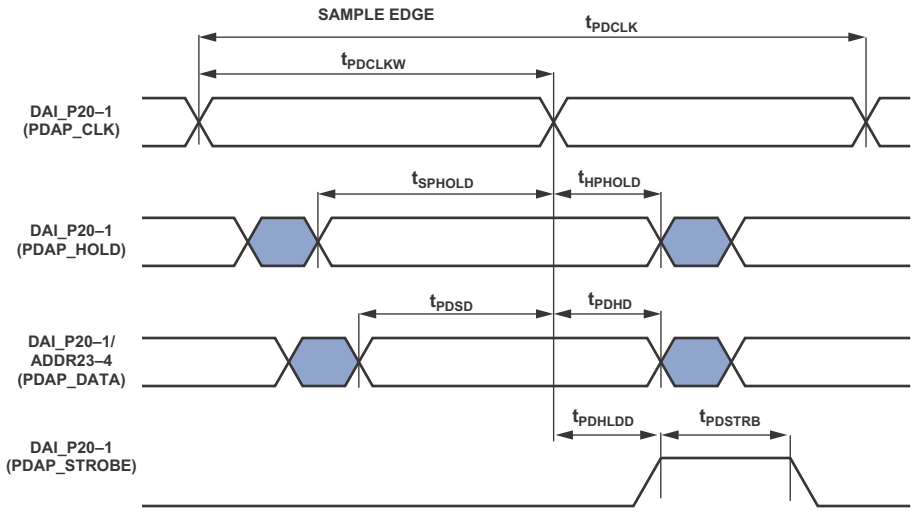


Figure 31. PDAP Timing

JTAG Test Access Port and Emulation

Table 57. JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	7		ns
t_{HSYS}[1]	System Inputs Hold After TCK High	18		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width	$4 \times t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		10	ns
t_{DSYS}[2]	System Outputs Delay After TCK Low		$t_{CK} \div 2 + 7$	ns

[1] System Inputs = AMI_DATA, DDR2_DATA, CLKCFG1–0, BOOTCFG2–0 RESET, DAI, DPI, FLAG3–0.
[2] System Outputs = AMI_ADDR/DATA, DDR2_ADDR/DATA, AMI_CTRL, DDR2_CTRL, DAI, DPI, FLAG3–0, $\overline{\text{EMU}}$.

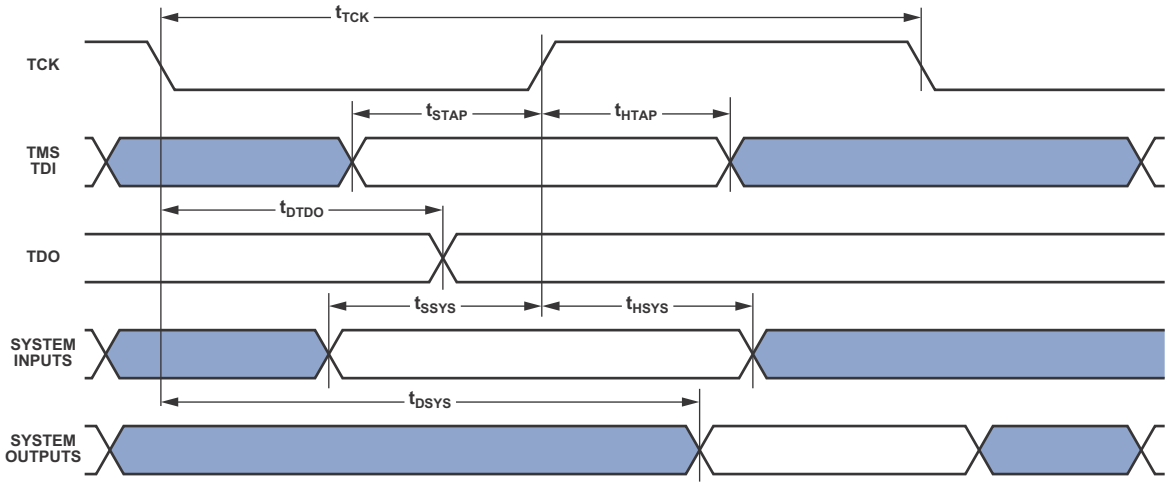
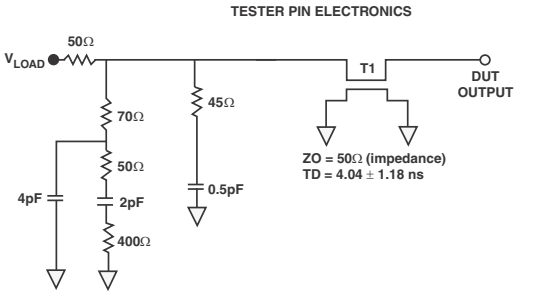


Figure 45. IEEE 1149.1 JTAG Test Access Port

TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 20 on Page 27 through Table 57 on Page 61. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 46.

Timing is measured on signals when they cross the V_{MEAS} level as described in Figure 47. All delays (in nanoseconds) are measured between the point that the first signal reaches V_{MEAS} and the point that the second signal reaches V_{MEAS}. The value of V_{MEAS} is 1.5 V for non-DDR pins and 0.9 V for DDR pins.



NOTES:
THE WORST-CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFLECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 46. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

Figure 47. Voltage Reference Levels for AC Measurements

OUTPUT DRIVE CURRENTS

Figure 48 and Figure 49 shows typical I-V characteristics for the output drivers of the processor, and Table 58 shows the pins associated with each driver. The curves represent the current drive capability of the output drivers as a function of output voltage.

Table 58. Driver Types

Driver Type	Associated Pins
A	LACK1–0, LDAT0[7:0], LDAT1[7:0], MLBCLK, MLBDAT, MLBDO, MLBSIG, MLBSO, AMI_ACK, AMI_ADDR23–0, AMI_DATA7–0, $\overline{\text{AMI\_MS1–0}}$, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, DAI_P, DPI_P, $\overline{\text{EMU}}$, FLAG3–0, RESETOUT, TDO
B	LCLK1–0
C	DDR2_ADDR15–0, DDR2_BA2–0, $\overline{\text{DDR2\_CAS}}$, DDR2_CKE, $\overline{\text{DDR2\_CS3–0}}$, DDR2_DATA15–0, DDR2_DM1–0, DDR2_ODT, $\overline{\text{DDR2\_RAS}}$, $\overline{\text{DDR2\_WE}}$
D (TRUE)	DDR2_CLK1–0, DDR2_DQS1–0
D (COMP)	$\overline{\text{DDR2\_CLK1–0}}$, $\overline{\text{DDR2\_DQS1–0}}$

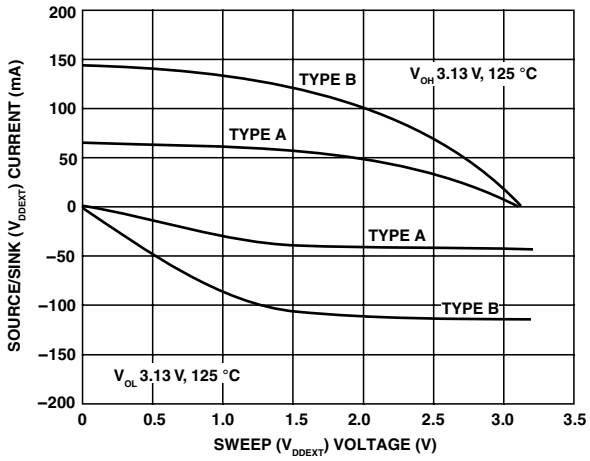


Figure 48. Output Buffer Characteristics (Worst-Case Non-DDR2)

Table 61. CSP_BGA Ball Assignment (Alphabetical by Signal) (Continued)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
GND	G09	GND	N17	TMS	K16	V_{DD_INT}	E08
GND	G10	GND	P05	$\overline{TRST}$	N15	V_{DD_INT}	E09
GND	G11	GND	P07	VDD_A	H01	V_{DD_INT}	E14
GND	G12	GND	P09	V_{DD_DDR2}	C05	V_{DD_INT}	E15
GND	G15	GND	P11	V_{DD_DDR2}	C12	V_{DD_INT}	F06
GND	H04	GND	P13	V_{DD_DDR2}	D03	V_{DD_INT}	F07
GND	H07	GND	V01	V_{DD_DDR2}	D06	V_{DD_INT}	F08
GND	H08	GND	V18	V_{DD_DDR2}	D08	V_{DD_INT}	F09
GND	H09	GND	R09	V_{DD_DDR2}	D18	V_{DD_INT}	F10
GND	H10	GND/ID0[1]	G03	V_{DD_DDR2}	E02	V_{DD_INT}	F11
GND	H11	GND/ID1[1]	G04	V_{DD_DDR2}	E04	V_{DD_INT}	F12
GND	H12	LACK_0	K17	V_{DD_DDR2}	E07	V_{DD_INT}	F13
GND	J01	LACK_1	P17	V_{DD_DDR2}	E10	V_{DD_INT}	G06
GND	J07	LCLK_0	J18	V_{DD_DDR2}	E11	V_{DD_INT}	G13
GND	J08	LCLK_1	N18	V_{DD_DDR2}	E17	V_{DD_INT}	H05
GND	J09	LDAT0_0	E18	V_{DD_DDR2}	F03	V_{DD_INT}	H06
GND	J10	LDAT0_1	F17	V_{DD_DDR2}	F05	V_{DD_INT}	H13
GND	J11	LDAT0_2	F18	V_{DD_DDR2}	F15	V_{DD_INT}	H14
GND	J12	LDAT0_3	G17	V_{DD_DDR2}	G14	V_{DD_INT}	J06
GND	J14	LDAT0_4	G18	V_{DD_DDR2}	G16	V_{DD_INT}	J13
GND	J17	LDAT0_5	H16	V_{DD_EXT}	H15	V_{DD_INT}	K06
GND	K05	LDAT0_6	H17	V_{DD_EXT}	H18	V_{DD_INT}	K13
GND	K07	LDAT0_7	J16	V_{DD_EXT}	J05	V_{DD_INT}	L06
GND	K08	LDAT1_0	K18	V_{DD_EXT}	J15	V_{DD_INT}	L13
GND	K09	LDAT1_1	L16	V_{DD_EXT}	K14	V_{DD_INT}	M06
GND	K10	LDAT1_2	L17	V_{DD_EXT}	L05	V_{DD_INT}	M13
GND	K11	LDAT1_3	L18	V_{DD_EXT}	M14	V_{DD_INT}	N06
GND	K12	LDAT1_4	M16	V_{DD_EXT}	M18	V_{DD_INT}	N07
GND	L07	LDAT1_5	M17	V_{DD_EXT}	N05	V_{DD_INT}	N08
GND	L08	LDAT1_6	N16	V_{DD_EXT}	P06	V_{DD_INT}	N09
GND	L09	LDAT1_7	P16	V_{DD_EXT}	P08	V_{DD_INT}	N13
GND	L10	MLBCLK	K03	V_{DD_EXT}	P10	V_{DD_THD}	N10
GND	L11	MLBDAT	K04	V_{DD_EXT}	P12	V_{REF}	D04
GND	L12	MLBDO	L04	V_{DD_EXT}	P14	V_{REF}	D11
GND	L14	MLBSIG	L02	V_{DD_EXT}	P15	XTAL	K01
GND	M05	MLBSO	L03	V_{DD_EXT}	T08		
GND	M07	$\overline{RESET}$	M01	V_{DD_EXT}	T09		
GND	M08	$\overline{RESETOUT}$/$\overline{RUNRSTIN}$	M02	V_{DD_EXT}	U09		
GND	M09	TCK	K15	V_{DD_EXT}	V09		
GND	M10	TDI	L15	V_{DD_EXT}/$\overline{BR1}$[1]	V08		
GND	M11	TDO	M15	V_{DD_EXT}/$\overline{BR2}$[1]	U08		
GND	M12	THD_M	N12	V_{DD_INT}	D12		
GND	N14	THD_P	N11	V_{DD_INT}	E06		

[1] This pin can be used for shared DDR2 memory between two processors. If shared memory functionality is not used then $\overline{BRx}$ pins should be tied to V_{DD_EXT} and IDx pins should be tied to GND. Table 10 on Page 14 for appropriate connections.

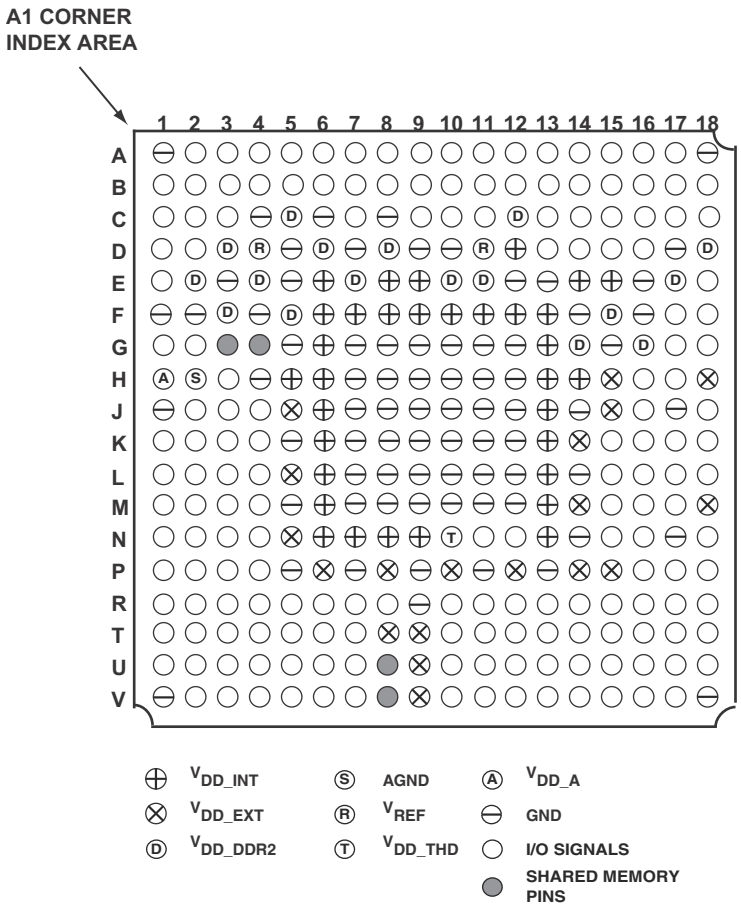


Figure 60. Ball Configuration, Automotive Model

CSP_BGA BALL ASSIGNMENT—STANDARD MODELS

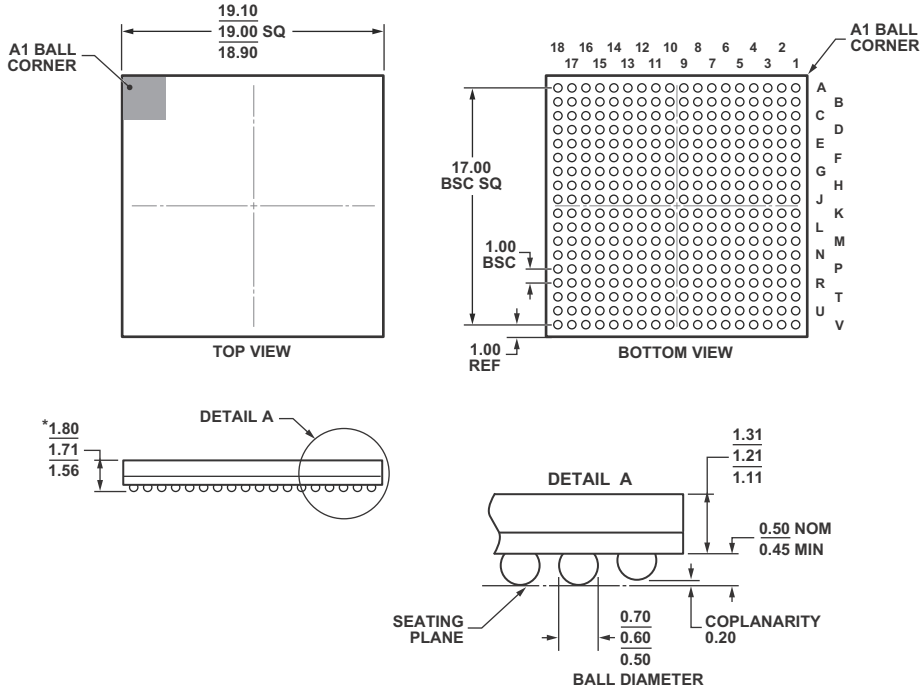
Table 62 lists the standard model CSP_BGA ball assignments by signal.

Table 62. CSP_BGA Ball Assignment (Alphabetical by Signal)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
AGND	H02	BOOT_CFG2	H03	DDR2_BA0	C18	DPI_P03	T01
AMI_ACK	R10	CLK_CFG0	G01	DDR2_BA1	C17	DPI_P04	R01
AMI_ADDR0	V16	CLK_CFG1	G02	DDR2_BA2	B18	DPI_P05	P01
AMI_ADDR01	U16	CLKIN	L01	$\overline{\text{DDR2\_CAS}}$	C07	DPI_P06	P02
AMI_ADDR02	T16	DAI_P01	R06	DDR2_CKE	E01	DPI_P07	P03
AMI_ADDR03	R16	DAI_P02	V05	$\overline{\text{DDR2\_CLK0}}$	A07	DPI_P08	P04
AMI_ADDR04	V15	DAI_P03	R07	DDR2_CLK0	B07	DPI_P09	N01
AMI_ADDR05	U15	DAI_P04	R03	$\overline{\text{DDR2\_CLK1}}$	A13	DPI_P10	N02
AMI_ADDR06	T15	DAI_P05	U05	DDR2_CLK1	B13	DPI_P11	N03
AMI_ADDR07	R15	DAI_P06	T05	$\overline{\text{DDR2\_CS0}}$	C01	DPI_P12	N04
AMI_ADDR08	V14	DAI_P07	V06	$\overline{\text{DDR2\_CS1}}$	D01	DPI_P13	M03
AMI_ADDR09	U14	DAI_P08	V02	$\overline{\text{DDR2\_CS2}}$	C02	DPI_P14	M04
AMI_ADDR10	T14	DAI_P09	R05	$\overline{\text{DDR2\_CS3}}$	D02	$\overline{\text{EMU}}$	K02
AMI_ADDR11	R14	DAI_P10	V04	DDR2_DATA0	B02	FLAG0	R08
AMI_ADDR12	V13	DAI_P11	U04	DDR2_DATA01	A02	FLAG1	V07
AMI_ADDR13	U13	DAI_P12	T04	DDR2_DATA02	B03	FLAG2	U07
AMI_ADDR14	T13	DAI_P13	U06	DDR2_DATA03	A03	FLAG3	T07
AMI_ADDR15	R13	DAI_P14	U02	DDR2_DATA04	B05	GND	A01
AMI_ADDR16	V12	DAI_P15	R04	DDR2_DATA05	A05	GND	A18
AMI_ADDR17	U12	DAI_P16	V03	DDR2_DATA06	B06	GND	C04
AMI_ADDR18	T12	DAI_P17	U03	DDR2_DATA07	A06	GND	C06
AMI_ADDR19	R12	DAI_P18	T03	DDR2_DATA08	B08	GND	C08
AMI_ADDR20	V11	DAI_P19	T06	DDR2_DATA09	A08	GND	D05
AMI_ADDR21	U11	DAI_P20	T02	DDR2_DATA10	B09	GND	D07
AMI_ADDR22	T11	DDR2_ADDR0	D13	DDR2_DATA11	A09	GND	D09
AMI_ADDR23	R11	DDR2_ADDR01	C13	DDR2_DATA12	A11	GND	D10
AMI_DATA0	U18	DDR2_ADDR02	D14	DDR2_DATA13	B11	GND	D17
AMI_DATA1	T18	DDR2_ADDR03	C14	DDR2_DATA14	A12	GND	E03
AMI_DATA2	R18	DDR2_ADDR04	B14	DDR2_DATA15	B12	GND	E05
AMI_DATA3	P18	DDR2_ADDR05	A14	DDR2_DM0	C03	GND	E12
AMI_DATA4	V17	DDR2_ADDR06	D15	DDR2_DM1	C11	GND	E13
AMI_DATA5	U17	DDR2_ADDR07	C15	DDR2_DQS0	A04	GND	E16
AMI_DATA6	T17	DDR2_ADDR08	B15	$\overline{\text{DDR2\_DQS0}}$	B04	GND	F01
AMI_DATA7	R17	DDR2_ADDR09	A15	DDR2_DQS1	A10	GND	F02
$\overline{\text{AMI\_MS0}}$	T10	DDR2_ADDR10	D16	$\overline{\text{DDR2\_DQS1}}$	B10	GND	F04
$\overline{\text{AMI\_MS1}}$	U10	DDR2_ADDR11	C16	DDR2_ODT	B01	GND	F14
$\overline{\text{AMI\_RD}}$	J04	DDR2_ADDR12	B16	$\overline{\text{DDR2\_RAS}}$	C09	GND	F16
$\overline{\text{AMI\_WR}}$	V10	DDR2_ADDR13	A16	$\overline{\text{DDR2\_WE}}$	C10	GND	G05
BOOT_CFG0	J02	DDR2_ADDR14	B17	DPI_P01	R02	GND	G07
BOOT_CFG1	J03	DDR2_ADDR15	A17	DPI_P02	U01	GND	G08

OUTLINE DIMENSIONS

The processors are available in a 19 mm by 19 mm CSP_BGA lead-free package.



*COMPLIANT TO JEDEC STANDARDS MO-192-AAG-1 WITH THE EXCEPTION TO PACKAGE HEIGHT.

Figure 62. 324-Ball Chip Scale Package, Ball Grid Array [CSP_BGA] (BC-324-1)
Dimensions shown in millimeters

SURFACE-MOUNT DESIGN

The following table is provided as an aid to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard.*

Package	Package Ball Attach Type	Package Solder Mask Opening	Package Ball Pad Size
324-Ball CSP_BGA (BC-324-1)	Solder Mask Defined	0.43 mm diameter	0.6 mm diameter